SN75439
QUADRUPLE PERIPHERAL DRIVER

SLRS013A – MAY 1988 – REVISED NOVEMBER 1989

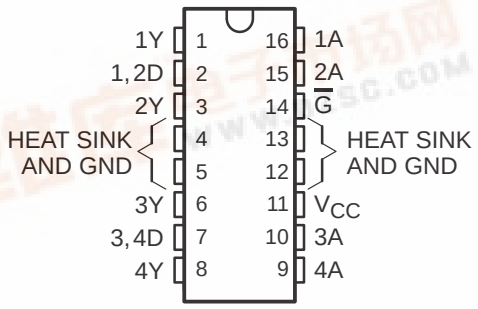
- 1.3-A Current Capability Each Channel
- Saturating Outputs With Low On-State Resistance
- Two Inverting and Two Noninverting Driver Channels With Common Active-Low Enable Input
- Key Application Is as a Complete Full-Step 4-Phase DC Stepper Motor Driver Using Only Three Directly Connected Logic Control Signal Lines From Standard Microprocessors
- High-Impedance Inputs Compatible With TTL or CMOS Levels
- Very Low Standby Power . . . 10 mW Typ
- 50-V Noninductive Switching Voltage Capability
- 40-V Inductive Switching Voltage Capability
- Output Clamp Diodes for Inductive Transient Protection
- 2-W Power Package

description

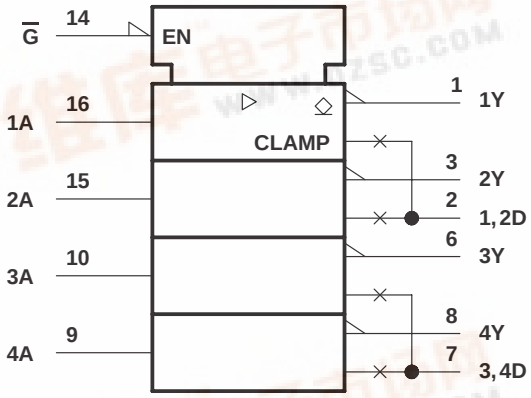
The SN75439 quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. The device features two inverting and two noninverting open-collector outputs with a common-enable input that, when taken high, disables all four outputs. By pairing each inverting channel with a corresponding noninverting channel (such as channel 1 paired with channel 2 and channel 3 paired with channel 4), the device may be used as a complete full-step 4-phase dc stepper-motor driver using only two input logic control signals plus the enable signal, as shown in Figure 3. Other applications include driving relays, lamps, solenoids, motors, LEDs, transmission lines, hammers, and other high-power-demand loads.

The SN75439 is characterized for operation from 0°C to 70°C.

NE PACKAGE
(TOP VIEW)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

Function Tables

EACH CHANNEL 1 OR CHANNEL 4 DRIVER

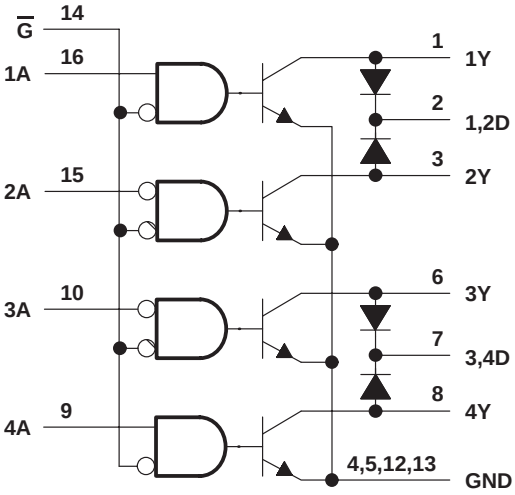
INPUTS		OUTPUT
A	$\overline{G}$	Y
H	L	L
L	X	H
X	H	H

EACH CHANNEL 2 OR CHANNEL 3 DRIVER

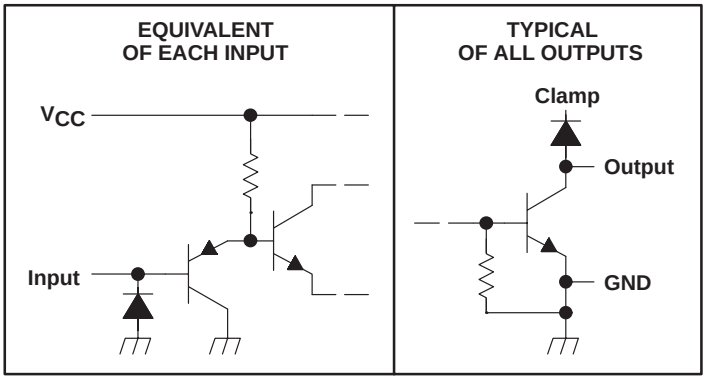
INPUTS		OUTPUT
A	$\overline{G}$	Y
L	L	L
H	X	H
X	H	H

H = high level, L = low level X = irrelevant

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 7 V
Input voltage, V_I	7 V
Output voltage range, V_O	–0.3 V to 52 V
Output voltage, V_O (inductive load)	43 V
Output clamp-diode terminal voltage range, V_{OK}	–0.3 V to 52 V
Input current, I_I	–15 mA
Peak sink output current, I_{OM} (nonrepetitive, $t_w \le 0.1$ ms) (see Note 2)	1.5 A
(repetitive, $t_w \le 10$ ms, duty cycle ≤ 50%)	1.4 A
Continuous sink output current, I_O (see Note 2)	1.3 A
Peak output clamp diode current, I_{OKM} (nonrepetitive, $t_w \le 0.1$ ms) (see Note 2)	1.5 A
(repetitive, $t_w \le 10$ ms, duty cycle ≤ 50%)	1.3 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3)	2075 mW
Continuous total dissipation at (or below) 65°C case temperature (see Note 3)	5000 mW
Operating case or virtual junction temperature range	–55°C to 150°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values are with respect to the network GND (unless otherwise specified).
2. All four channels of this device may conduct rated current simultaneously; however, power dissipation average over a short time interval must fall within the continuous dissipation range.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. For operation above 65°C case temperature, derate linearly at the rate of 59 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Output supply voltage in inductive switching circuit, V_S (see Figure 2)			40	V
High-level input voltage, V_{IH}	2		5.25	V
Low-level input voltage, V_{IL}	–0.3†		0.8	V
Low-level output current, I_{OL}			1.3	A
Operating free-air temperature, T_A	0	25	70	°C

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltages (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –12 mA			–0.9	–1.5	V
V_{OL}	Low-level output voltage	I_{OL} = 0.5 A	See Note 4		0.2	0.35	V
		I_{OL} = 1 A			0.4	0.7	
		I_{OL} = 1.3 A			0.5	0.9	
$V_{F(K)}$	Output clamp-diode forward voltage	I_F = 0.5 A	See Note 4		1.1	1.9	V
		I_F = 1 A			1.3	2.2	
		I_F = 1.3 A			1.4	2.4	
I_{OH}	High-level output current	V_{OH} = 50 V,	V_{OK} = 50 V			100	µA
I_{IH}	High-level input current	$V_I = V_{IH}$				10	µA
I_{IL}	Low-level input current	V_I = 0 to 0.8 V				–10	µA
$I_{R(K)}$	Output clamp-diode reverse current (at Y output)	V_R = 50 V,	V_O = 0			100	µA
I_{CC}	Supply current	All outputs at high level (off)			2	8	mA
		All outputs at low level (on)			140	200	
		Two outputs at high level (off) and two outputs at low level (on)			70	110	

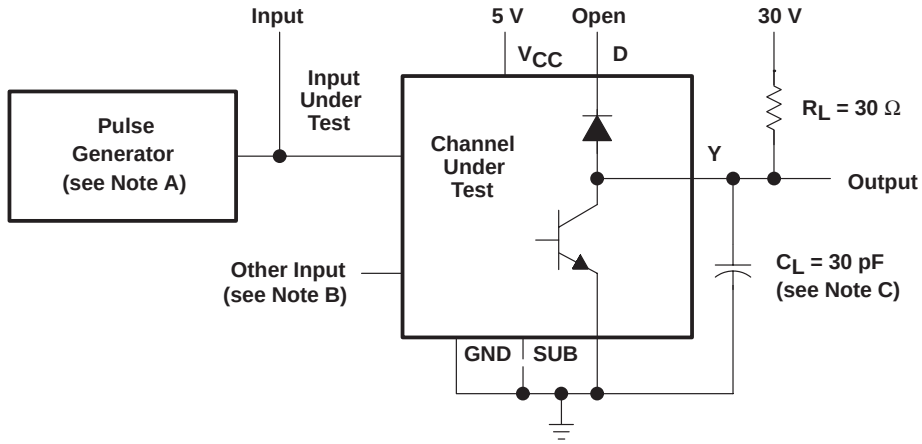
† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 4: These parameters must be measured using pulse techniques, t_w = 1 ms, duty cycle ≤ 10%.

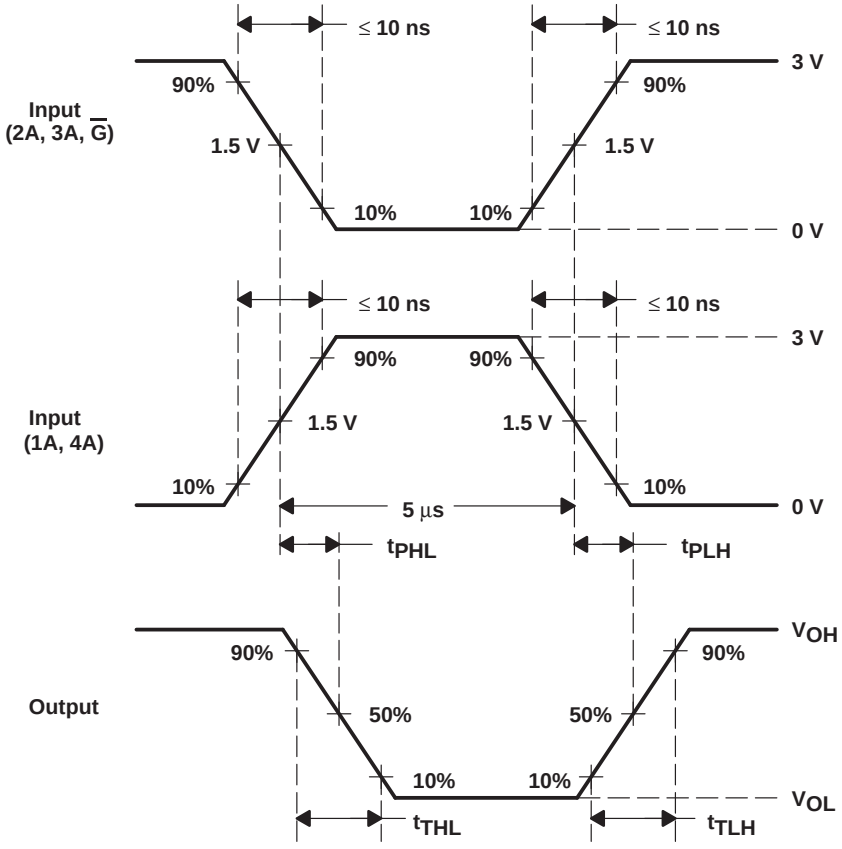
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_{OL} ≈ 1 A, R_L = 30 Ω,	C_L = 30 pF, See Figure 1		1500		ns
t_{PHL}	Propagation delay time, high-to-low-level output				100		ns
t_{TLH}	Transition time, low-to-high-level output				170		ns
t_{THL}	Transition time, high-to-low-level output				50		ns
V_{OH}	High-level output voltage (after switching inductive load)	V_S = 40 V, R_L = 31 Ω,	I_O ≈ 1.3 A, See Figure 2	V_S – 100			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

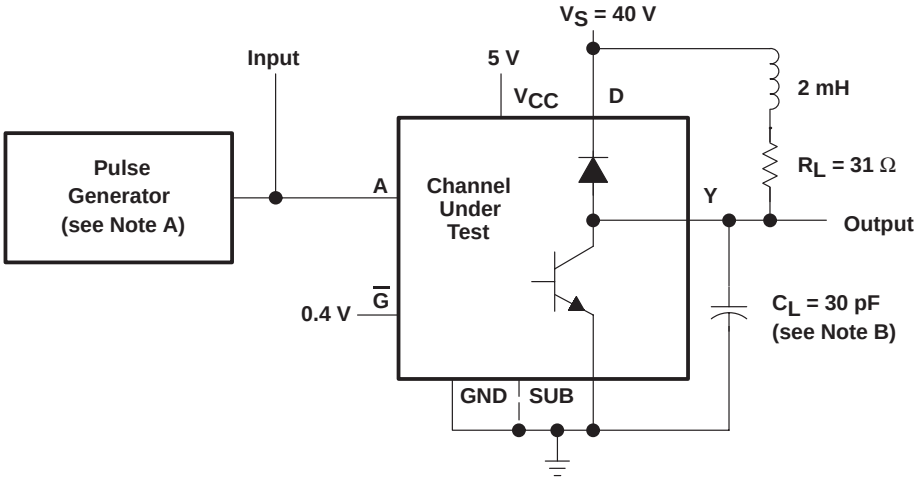


VOLTAGE WAVEFORMS

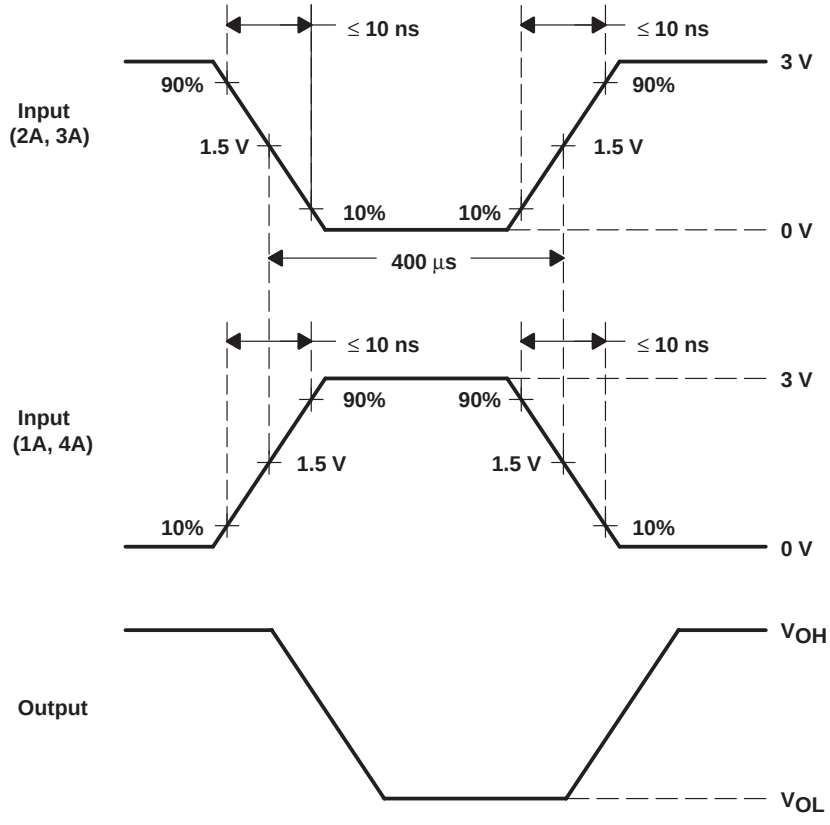
NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1 %, Z_O = 50 Ω.
B. Enable input $\overline{G}$ is at 0 V if input A is used as the switching input. When $\overline{G}$ is used as the switching input, the corresponding A input is at 0 V if testing channel 2 or channel 3 or at 3 V if testing channel 1 or channel 4.
C. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Switching Characteristics

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

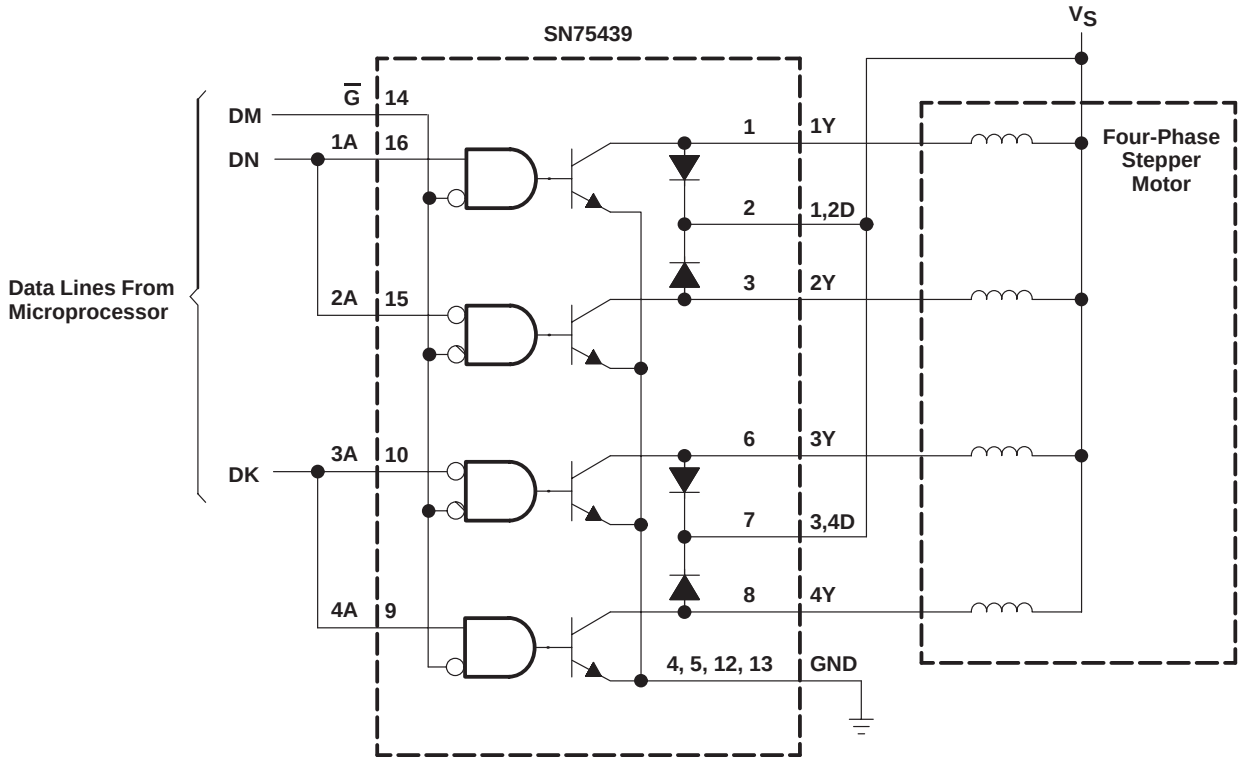


VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1 %, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Output Latch-Up Test Circuit and Voltage Waveforms

APPLICATION INFORMATION



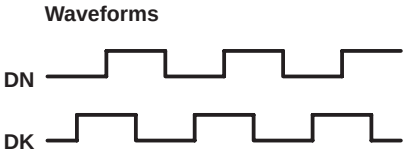


Figure 3. Full-Step Four-Phase Stepper-Motor Driver

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