



UC2909
UC3909

Switchmode Lead-Acid Battery Charger

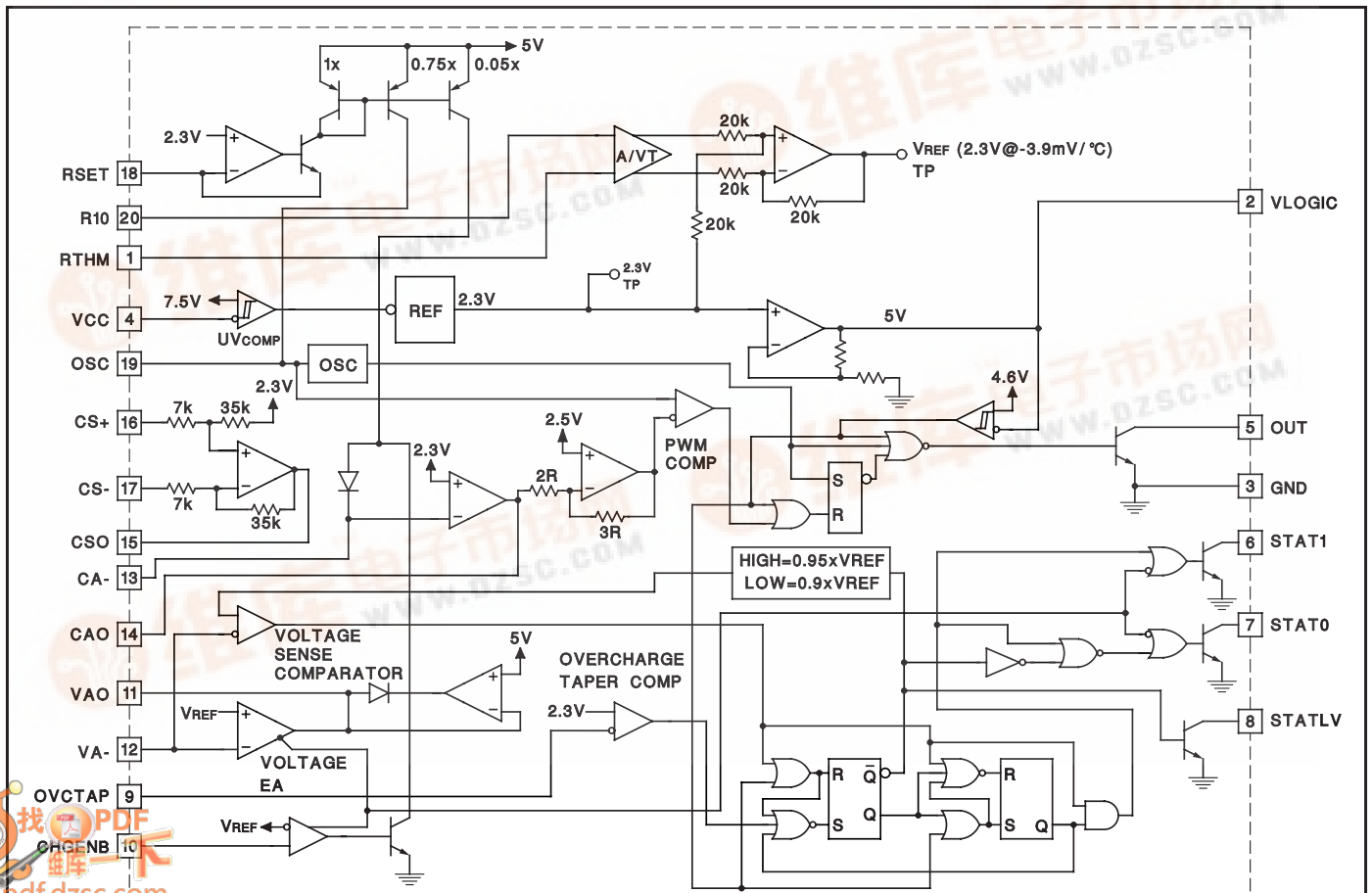
FEATURES

- Accurate and Efficient Control of Battery Charging
- Average Current Mode Control from Trickle to Overcharge
- Resistor Programmable Charge Currents
- Thermistor Interface Tracks Battery Requirements Over Temperature
- Output Status Bits Report on Four Internal Charge States
- Undervoltage Lockout Monitors VCC and VREF

DESCRIPTION

The UC3909 family of Switchmode Lead-Acid Battery Chargers accurately controls lead acid battery charging with a highly efficient average current mode control loop. This chip combines charge state logic with average current PWM control circuitry. Charge state logic commands current or voltage control depending on the charge state. The chip includes undervoltage lockout circuitry to insure sufficient supply voltage is present before output switching starts. Additional circuit blocks include a differential current sense amplifier, a 1.5% voltage reference, a $-3.9\text{mV}/^\circ\text{C}$ thermistor linearization circuit, voltage and current error amplifiers, a PWM oscillator, a PWM comparator, a PWM latch, charge state decode bits, and a 100mA open collector output driver.

BLOCK DIAGRAM



Pin numbers refer to J, N, DW packages.

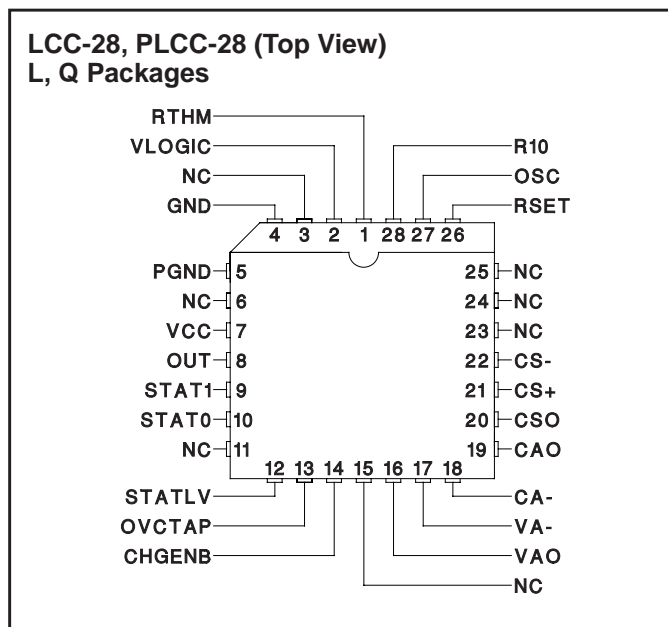
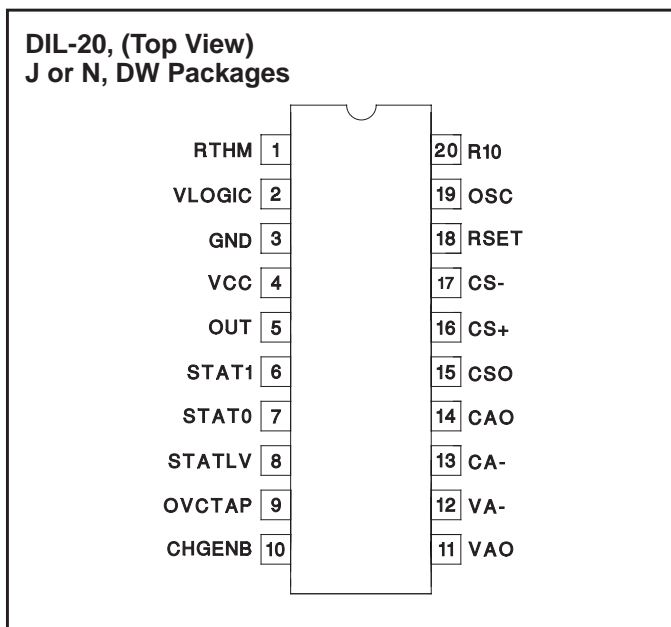
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC), OUT, STAT0, STAT1 40V
 Output Current Sink 0.1A
 CS+, CS- -0.4 to VCC (Note 1)
 Remaining Pin Voltages. -0.3V to 9V
 Storage Temperature -65°C to +150°C
 Junction Temperature -55°C to +150°C
 Lead Temperature (Soldering, 10 sec.) +300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

Note 1: Voltages more negative than -0.4V can be tolerated if current is limited to 50mA.

CONNECTION DIAGRAMS



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for UC2909; 0°C to $+70^\circ\text{C}$ for UC3909; $C_T = 330\text{pF}$, $R_{SET} = 11.5\text{k}$, $R_{10} = 10\text{k}$, $R_{THM} = 10\text{k}$, $V_{CC} = 15\text{V}$, Output no load, $R_{STAT0} = R_{STAT1} = 10\text{k}$, $CHGENB = OVCTAP = VLOGIC$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense AMP (CSA) Section					
DC Gain	$V_{ID} = CS+ - CS-$ $CS- = 0, CS+ = -50\text{mV}; CS+ = -250\text{mV}$	4.90	5	5.10	V/V
	$CS+ = 0, CS- = 50\text{mV}; CS- = 250\text{mV}$	4.90	5	5.10	V/V
$V_{OFFSET} (V_{CSO} - V_{CAO})$	$CS+ = CS- = 2.3\text{V}, CAO = CA-$			15	mV
CMRR	$V_{CM} = -0.25$ to $V_{CC} - 2, 8.8 < V_{CC} < 14$	50			dB
	$V_{CM} = -0.25$ to $V_{CC}, 14 < V_{CC} < 35$	50			dB
V_{OL}	$V_{ID} = -550\text{mV}, -0.25\text{V} < V_{CM} < V_{CC} - 2,$ $I_O = 500\mu\text{A}$		0.3	0.6	V
V_{OH}	$V_{ID} = +700\text{mV}, -0.25\text{V} < V_{CM} < V_{CC} - 2,$ $I_O = -250\mu\text{A}$	5.2	5.7	6.2	V
Output Source Current	$V_{ID} = +700\text{mV}, CSO = 4\text{V}$		-1	-0.5	mA
Output Sink Current	$V_{ID} = -550\text{mV}, CSO = 1\text{V}$	3	4.5		mA
3dB Bandwidth	$V_{ID} = 90\text{mV}, V_{CM} = 0\text{V}$	200			kHz

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Error Amplifier (CEA) Section					
I_B	$8.8\text{V} < V_{CC} < 35\text{V}$, $V_{CHGENB} = V_{LOGIC}$		0.1	0.8	μA
V_{IO} (Note 2)	$8.8\text{V} < V_{CC} < 35\text{V}$, $CAO = CA-$			10	mV
A_{VO}	$1\text{V} < V_{AO} < 4\text{V}$	60	90		dB
GBW	$T_J = 25^\circ\text{C}$, $F = 100\text{kHz}$	1	1.5		MHz
V_{OL}	$I_O = 250\mu\text{A}$		0.4	0.6	V
V_{OH}	$I_O = -5\text{mA}$	4.5	5		V
Output Source Current	$CAO = 4\text{V}$		-25	-12	mA
Output Sink Current	$CAO = 1\text{V}$	2	3		mA
I_{CA-} , $I_{TRCK_CONTROL}$	$V_{CHGENB} = \text{GND}$	8.5	10	11.5	μA
Voltage Amplifier (CEA) Section					
I_B	Total Bias Current; Regulating Level		0.1	1	μA
V_{IO} (Note 2)	$8.8\text{V} < V_{CC} < 35\text{V}$, $V_{CM} = 2.3\text{V}$, $VAO = VA-$		1.2		mV
A_{VO}	$1\text{V} < CAO < 4\text{V}$	60	90		dB
GBW	$T_J = 25^\circ\text{C}$, $F = 100\text{kHz}$	0.25	0.5		MHz
V_{OL}	$I_O = 500\mu\text{A}$		0.4	0.6	V
V_{OH}	$I_O = -500\mu\text{A}$	4.75	5	5.25	V
Output Source Current	$CAO = 4\text{V}$	-2	-1		mA
Output Sink Current	$CAO = 1\text{V}$	2	2.5		mA
VAO Leakage: High Impedance State	$V_{CHGENB} = \text{GND}$, $STAT0 = 0$ & $STAT1 = 0$, $VAO = 2.3\text{V}$	-1		1	μA
Pulse Width Modulator Section					
Maximum Duty Cycle	$CAO = 0.6\text{V}$	90	95	100	%
Modulator Gain	$CAO = 2.5\text{V}, 3.2\text{V}$	63	71	80	%/V
OSC Peak			3		V
OSC Valley			1		V
Oscillator Section					
Frequency	$8.8\text{V} < V_{CC} < 35\text{V}$	198	220	242	kHz
Thermistor Derived Reference Section					
	$V_{ID} = V_{RTHM} - V_{R10}$				
Initial Accuracy, VAO (RTHM = 10k)	$V_{ID} = 0$, $R_{10} = R_{THM} = 10\text{k}$ (Note 3)	2.2655	2.3	2.3345	V
	$V_{ID} = 0$, $R_{10} = R_{THM} = 10\text{k}$, $-40^\circ\text{C} \leq T_A < 0^\circ\text{C}$ (Note 3)	2.254	2.3	2.346	V
Line Regulation	$V_{CC} = 8.8\text{V}$ to 35V		3	10	mV
VAO	$R_{THM} = 138\text{k}$, $R_{10} = 10\text{k}$	2.458	2.495	2.532	V
	$R_{THM} = 138\text{k}$, $R_{10} = 10\text{k}$, $-40^\circ\text{C} \leq T_A < 0^\circ\text{C}$	2.445	2.495	2.545	V
	$R_{THM} = 33.63\text{k}$, $R_{10} = 10\text{k}$	2.362	2.398	2.434	V
	$R_{THM} = 33.63\text{k}$, $R_{10} = 10\text{k}$, $-40^\circ\text{C} \leq T_A < 0^\circ\text{C}$	2.350	2.398	2.446	V
	$R_{THM} = 1.014\text{k}$, $R_{10} = 10\text{k}$	2.035	2.066	2.097	V
	$R_{THM} = 1.014\text{k}$, $R_{10} = 10\text{k}$, $-40^\circ\text{C} \leq T_A < 0^\circ\text{C}$	2.025	2.066	2.107	V
Charge Enable Comparator Section (CEC)					
Threshold Voltage	As a function of $VA-$	0.99	1	1.01	V/V
Input Bias Current	$CHGENB = 2.3\text{V}$	-0.5	-0.1		μA

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Sense Comparator Section (VSC)					
Threshold Voltage	STAT0 = 0, STAT1 = 0, Function of V_{REF}	0.945	0.95	0.955	V/V
	STAT0 = 1, STAT1 = 0, Function of V_{REF}	0.895	0.9	0.905	V/V
Over Charge Taper Current Comparator Section (OCTIC)					
Threshold Voltage	Function of 2.3V REF, CA- = CAO	0.99	1	1.01	V/V
Input Bias Current	OVCTAP = 2.3V	-0.5	-0.1		μA
Logic 5V Reference Section (VLOGIC)					
VLOGIC	$V_{CC} = 15\text{V}$	4.875	5.0	5.125	V
Line Regulation	$8.8\text{V} < V_{CC} < 35\text{V}$		3	15	mV
Load Regulation	$0 < I_O < 10\text{mA}$		3	15	mV
Reference Comparator Turn-on Threshold			4.3	4.8	V
Short Circuit Current	$V_{REF} = 0\text{V}$	30	50	80	mA
Output Stage Section					
I_{SINK} Continuous			50		mA
I_{PEAK}			100		mA
V_{OL}	$I_O = 50\text{mA}$		1	1.3	V
Leakage Current	$V_{OUT} = 35\text{V}$			25	μA
STAT0 & STAT1 Open Collector Outputs Section					
Maximum Sink Current	$V_{OUT} = 8.8\text{V}$	6	10		mA
Saturation Voltage	$I_{OUT} = 5\text{mA}$		0.1	0.45	V
Leakage Current	$V_{OUT} = 35\text{V}$			25	μA
STATLV Open Collector Outputs Section					
Maximum Sink Current	$V_{OUT} = 5\text{V}$	2.5	5		mA
Saturation Voltage	$I_{OUT} = 2\text{mA}$		0.1	0.45	V
Leakage current	$V_{OUT} = 5\text{V}$			3	μA
UVLO Section					
Turn-on Threshold		6.8	7.8	8.8	V
Hysteresis		100	300	500	mV
I_{CC} Section					
I_{CC} (run)	(See Fig. 1)		13	19	mA
I_{CC} (off)	$V_{CC} = 6.5\text{V}$		2		mA

Note 2: V_{IO} is measured prior to packaging with internal probe pad.

Note 3: Thermistor initial accuracy is measured and trimmed with respect to VAO; $VAO = VA-$.

PIN DESCRIPTIONS

CA-: The inverting input to the current error amplifier.

CAO: The output of the current error amplifier which is internally clamped to approximately 4V. It is internally connected to the inverting input of the PWM comparator.

CS-, **CS+**: The inverting and non-inverting inputs to the current sense amplifier. This amplifier has a fixed gain of five and a common-mode voltage range of from -250mV to $+V_{CC}$.

CSO: The output of the current sense amplifier which is internally clamped to approximately 5.7V.

CHGENB: The input to a comparator that detects when battery voltage is low and places the charger in a trickle charge state. The charge enable comparator makes the output of the voltage error amplifier a high impedance while forcing a fixed $10\mu\text{A}$ into CA- to set the trickle charge current.

PIN DESCRIPTIONS (cont.)

GND: The reference point for the internal reference, all thresholds, and the return for the remainder of the device. The output sink transistor is wired directly to this pin.

OVCTAP: The overcharge current taper pin detects when the output current has tapered to the float threshold in the overcharge state.

OSC: The oscillator ramp pin which has a capacitor (C_T) to ground. The ramp oscillates between approximately 1.0V to 3.0V and the frequency is approximated by:

$$frequency = \frac{1}{1.2 \cdot C_T \cdot R_{SET}}$$

OUT: The output of the PWM driver which consists of an open collector output transistor with 100mA sink capability.

R10: Input used to establish a differential voltage corresponding to the temperature of the thermistor. Connect a 10k resistor to ground from this point.

RSET: A resistor to ground programs the oscillator charge current and the trickle control current for the oscillator ramp.

The oscillator charge current is approximately $\frac{1.75}{R_{SET}}$.

The trickle control current ($I_{TRCK_CONTROL}$) is approximately $\frac{0.115}{R_{SET}}$.

RTHM: A 10k thermistor is connected to ground and is thermally connected to the battery. The resistance will vary exponentially over temperature and its change is used to vary the internal 2.3V reference by $-3.9mV/^\circ C$. The recommended thermistor for this function is part number L1005-5744-103-D1, Keystone Carbon Company, St. Marys, PA.

STAT0: This open collector pin is the first decode bit used to decode the charge states.

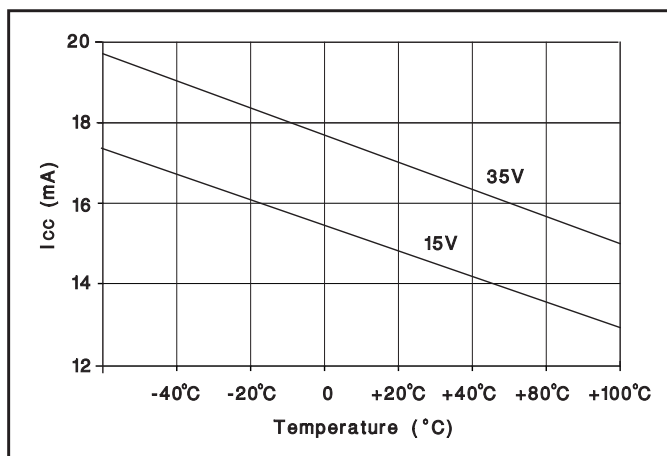


Figure 1. I_{CC} vs. temperature.

STAT1: This open collector pin is the second decode bit used to decode the charge states.

STATLV: This bit is high when the charger is in the float state.

VA- The inverting input to the voltage error amplifier.

VAO: The output of the voltage error amplifier. The upper output clamp voltage of this amplifier is 5V.

VCC: The input voltage to the chip. The chip is operational between 7.5V and 40V and should be bypassed with a $1\mu F$ capacitor. A typical I_{CC} vs. temperature is shown in Figure 1.

VLOGIC: The precision reference voltage. It should be bypassed with a $0.1\mu F$ capacitor.

Charge State Decode Chart

STAT0 and STAT1 are open collector outputs. The output is approximately 0.2V for a logic 0.

	STAT1	STAT0
Trickle Charge	0	0
Bulk Charge	0	1
Over Charge	1	0
Float Charge	1	1

APPLICATION INFORMATION

A Block Diagram of the UC3909 is shown on the first page, while a Typical Application Circuit is shown in Figure 2. The circuit in Figure 2 requires a DC input voltage between 12V and 40V.

The UC3909 uses a voltage control loop with average current limiting to precisely control the charge rate of a lead-acid battery. The small increase in complexity of average current limiting is offset by the relative simplicity of the control loop design.

CONTROL LOOP

Current Sense Amplifier

This amplifier measures the voltage across the sense resistor RS with a fixed gain of five and an offset voltage of 2.3V. This voltage is proportional to the battery current. The most positive voltage end of RS is connected to CS—ensuring the correct polarity going into the PWM comparator.

CSO = 2.3V when there is zero battery current.

RS is chosen by dividing 350mV by the maximum allowable load current. A smaller value for RS can be chosen to reduce power dissipation.

Maximum Charge Current, I_{bulk} , is set by knowing the maximum voltage error amplifier output, $V_{OH} = 5V$, the maximum allowable drop across RS, and setting the resistors RG1 and RG2 such that;

$$\frac{RG1}{RG2} = \frac{5 \cdot V_{RS}}{V_{LOGIC} - CA-} = \frac{5 \cdot V_{RS}}{5V - 2.3V} \quad (1)$$

$$\frac{5 \cdot V_{RS}}{2.7V} = 1.852 \cdot I_{BULK} \cdot RS$$

The maximum allowable drop across RS is specified to limit the maximum swing at CSO to approximately 2.0V to keep the CSO amplifier output from saturating.

No charge/load current: $V_{CSO} = 2.3V$,

Max charge/load current: $V_{max(CSO)} = 2.3V - 2.0V = 0.3V$

Voltage Error Amplifier:

The voltage error amplifier (VEA) senses the battery voltage and compares it to the 2.3V – 3.9mV/°C thermistor generated reference. Its output becomes the current command signal and is summed with the current sense amplifier output. A 5.0V voltage error amplifier upper clamp limits maximum load current. During the trickle charge state, the voltage amplifier output is opened (high impedance output) by the charge enable comparator. A trickle bias current is summed into the CA— input which sets the maximum trickle charge current.

The VEA, $V_{OH} = 5V$ clamp saturates the voltage loop and consequently limits the charge current as stated in Equation 1.

During the trickle bias state the maximum allowable charge current (ITC) is similarly determined:

$$ITC = \frac{I_{TRICK_CONTROL} \cdot RG1}{RS \cdot 5} \quad (2)$$

$I_{TRICK_CONTROL}$ is the fixed control current into CA—. $I_{TRICK_CONTROL}$ is 10µA when $R_{SET} = 11.5k$. See RSET pin description for equation.

Current Error Amplifier

The current error amplifier (CA) compares the output of the current sense amplifier to the output of the voltage error amplifier. The output of the CA forces a PWM duty cycle which results in the correct average battery current. With integral compensation, the CA will have a very high DC current gain, resulting in effectively no average DC current error. For stability purposes, the high frequency gain of the CA must be designed such that the magnitude of the down slope of the CA output signal is less than or equal to the magnitude of the up slope of the PWM ramp.

CHARGE ALGORITHM

Refer to Figure 3 in UC3906 Data Sheet in the data book.

A) Trickle Charge State

STAT0 = STAT1 = STATLV = logic 0

When CHGNB is less than VREF (2.3V – 3.9mV/°C), STATLV is forced low. This decreases the sense voltage divider ratio, forcing the battery to overcharge (VOC).

$$VOC = (VREF) \cdot \frac{(RS1 + RS2 + RS3 || RS4)}{(RS3 || RS4)} \quad (3)$$

During the trickle charge state, the output of the voltage error amplifier is high impedance. The trickle control current is directed into the CA— pin setting the maximum trickle charge current. The trickle charge current is defined in Equation 2.

B) Bulk Charge State

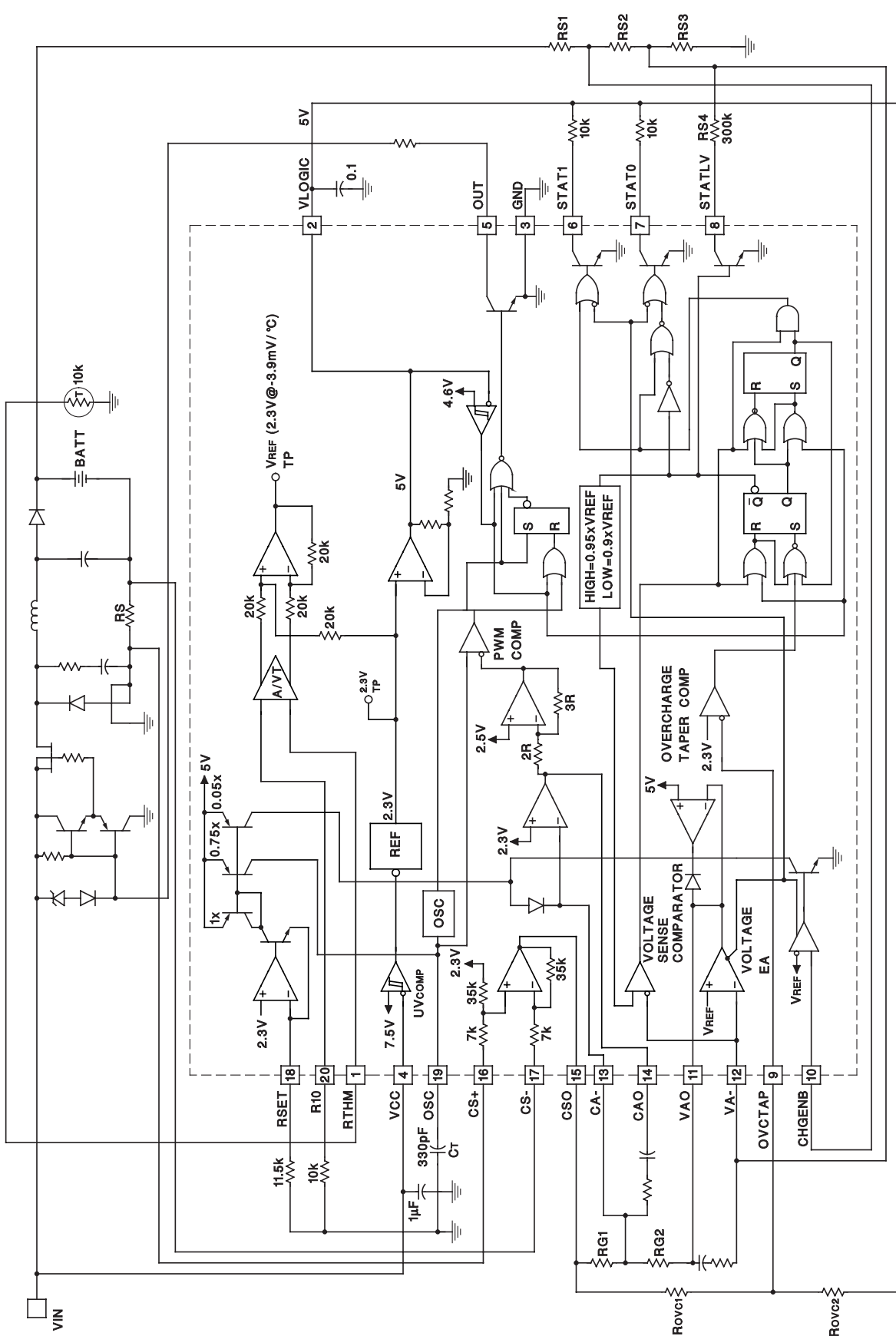
STAT1 = STATLV = logic 0, STAT0 = logic 1

As the battery charges, the UC3909 will transition from trickle to bulk charge when CHGENB becomes greater than 2.3V. The transition equation is

$$VT = VREF \cdot \frac{(RS1 + RS2 + RS3 || RS4)}{(RS2 + RS3 || RS4)} \quad (4)$$

STATLV is still driven low.

APPLICATION INFORMATION (cont.)



Pin numbers refer to J, N, DW packages.

APPLICATION INFORMATION (cont.)

During the bulk charge state, the voltage error amplifier is now operational and is commanding maximum charge current (I_{BULK}) set by Equation 1. The voltage loop attempts to force the battery to VOC.

C) Overcharge State

STAT0 = STATLV = logic 0, STAT1 = logic 1

The battery voltage surpasses 95% of VOC indicating the UC3909 is in its overcharge state.

During the overcharge charge state, the voltage loop becomes stable and the charge current begins to taper off. As the charge current tapers off, the voltage at CSO increases toward its null point of 2.3V. The center connection of the two resistors between CSO and VLOGIC sets the overcurrent taper threshold (OVCTAP). Knowing the desired overcharge terminate current (I_{OCT}), the resistors R_{OVC1} and R_{OVC2} can be calculated by choosing a value of R_{OVC2} and using the following equation:

$$R_{OVC1} = (18518) \cdot I_{OCT} \cdot RS \cdot R_{OVC2} \quad (5)$$

D) Float State

STAT0 = STAT1 = STATLV = logic 1

The battery charge current tapers below its OVCTAP threshold, and forces STATLV high increasing the voltage sense divider ratio. The voltage loop now forces the battery charger to regulate at its float state voltage (V_F).

$$V_F = (V_{REF}) \frac{(RS1 + RS2 + RS3)}{RS3} \quad (6)$$

If the load drains the battery to less than 90% of V_F , the charger goes back to the bulk charge state, STATE 1.

OFF LINE APPLICATIONS

For off line charge applications, either Figure 3 or Figure 4 can be used as a baseline. Figure 3 has the advantage of high frequency operation resulting in a small isolation transformer. Figure 4 is a simpler design, but at the expense of larger magnetics.

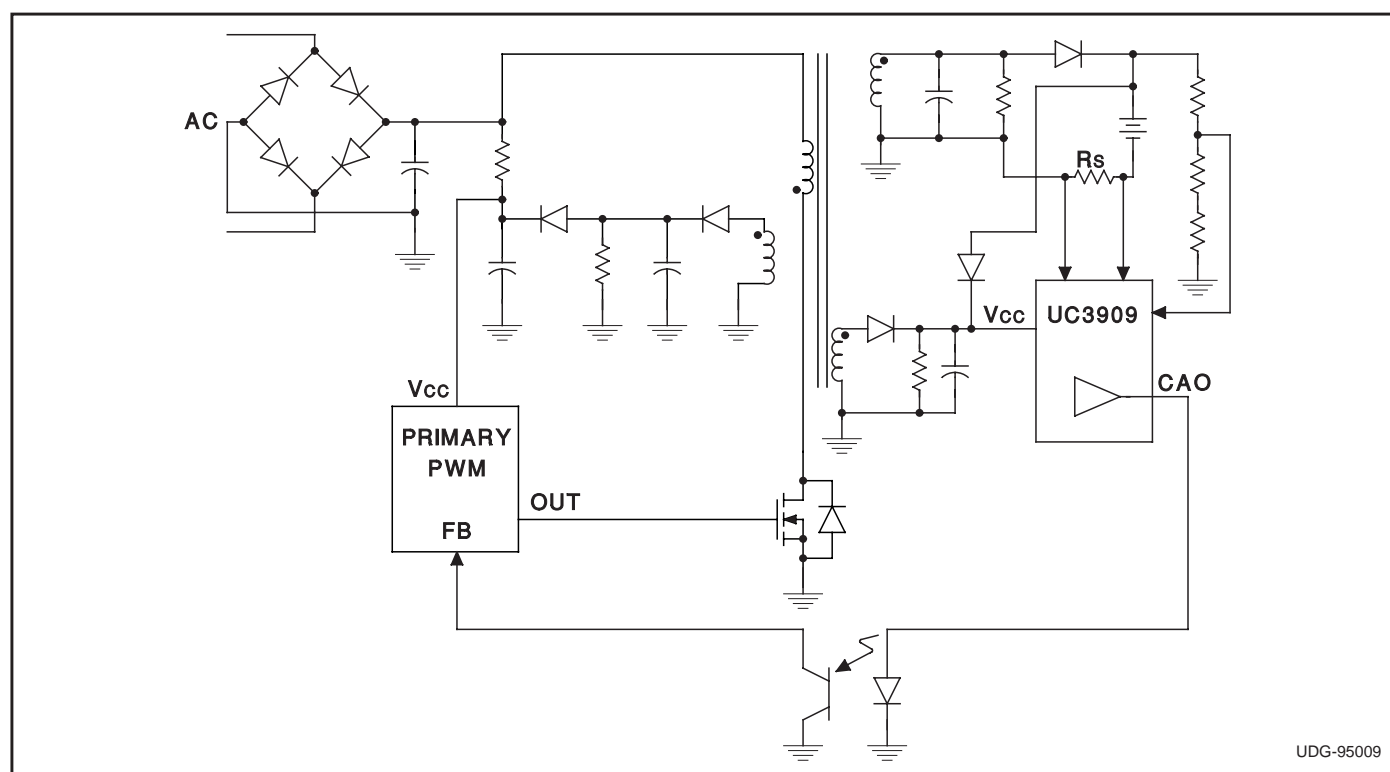
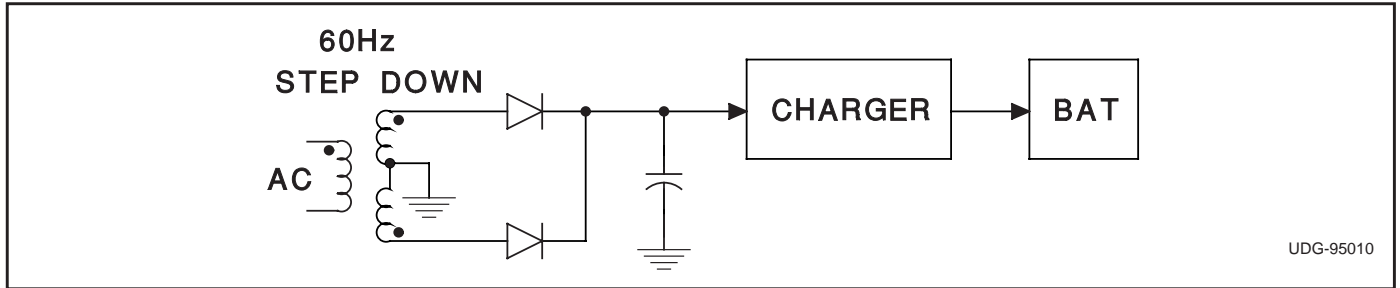


Figure 3. Off line charger with primary side PWM

APPLICATION INFORMATION (cont.)



UDG-95010

Figure 4. Isolated off line charger

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