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UCC3912

# Programmable Hot Swap Power Manager

## FEATURES

- Integrated 0.15Ω Power MOSFET
- 3V to 8V Operation
- Digital Programmable Current Limit from 0 to 3A
- Electronic Circuit Breaker Function
- 1μA I<sub>CC</sub> when Disabled
- Programmable on Time
- Programmable Start Delay
- Fixed 3% Duty Cycle
- Uni-Directional Switch
- Thermal Shutdown
- Fault Output Indicator
- Maximum Output Current can be set to 1A above the Programmed Fault Level or to a full 4A
- Power SOIC, Low Thermal Resistance Packaging

## DESCRIPTION

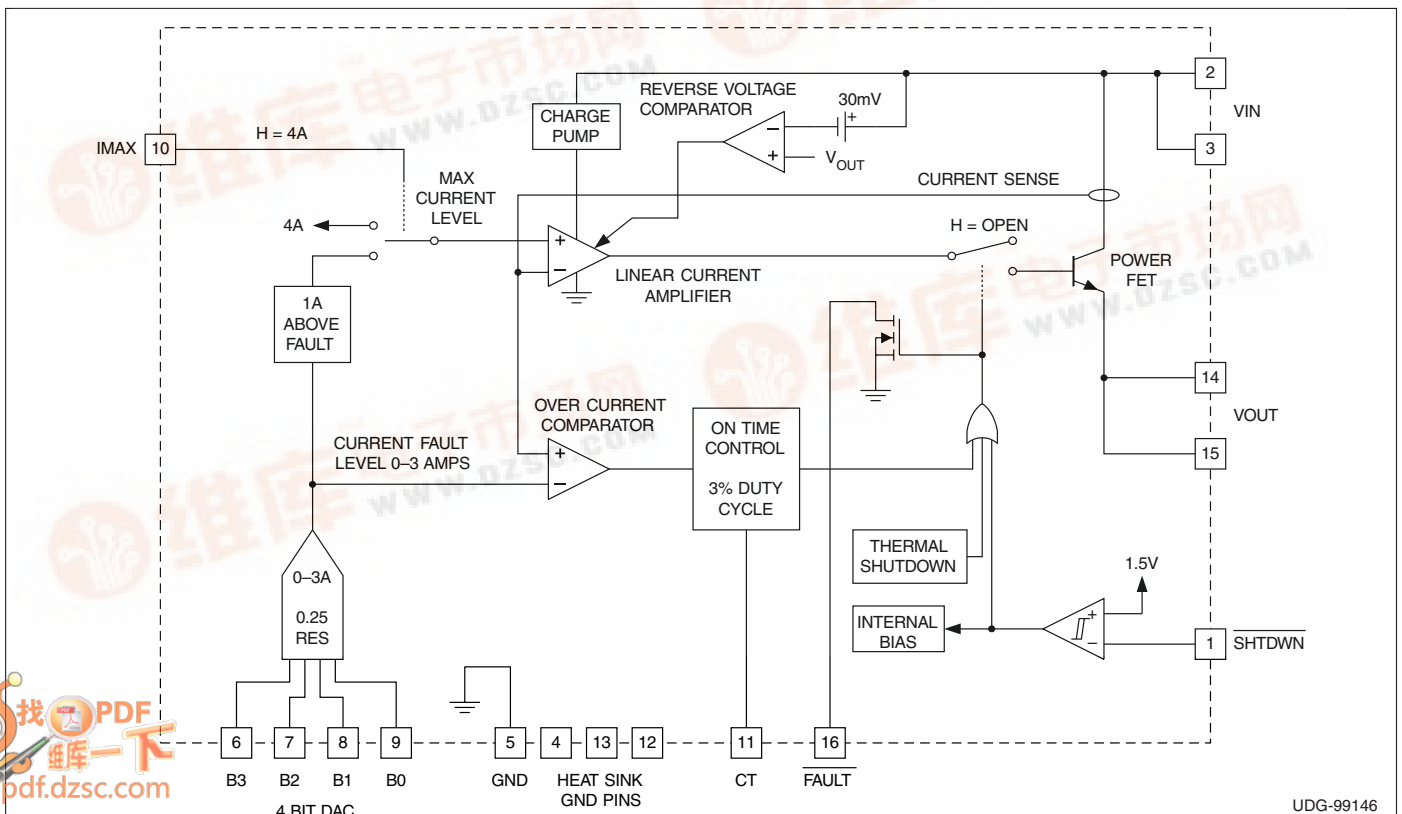
The UCC3912 Hot Swap Power Manager provides complete power management, hot swap capability, and circuit breaker functions. The only component required to operate the device, other than supply bypassing, is the fault timing capacitor, C<sub>T</sub>. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, and start-up delay. In the event of a constant fault, the Internal fixed 3% duty cycle ratio limits average output power.

The internal 4 bit DAC allows programming of the fault level current from 0 to 3A with 0.25A resolution. The IMAX control pin sets the maximum sourcing current to 1A above the fault level when driven low, and to a full 4A when driven high for applications which require fast output capacitor charging.

When the output current is below the fault level, the output MOSFET is switched on with a nominal on resistance of 0.15Ω. When the output current exceeds the fault level, but is less than the maximum sourcing level, the output remains switched on, but the fault timer starts charging C<sub>T</sub>. Once C<sub>T</sub> charges to a preset threshold, the switch is turned off, and remains off for 30 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions from a switch to a constant current source.

(continued)

## BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

V <sub>IN</sub> . . . . .	+8 V
FAULT Sink Current . . . . .	50mA
FAULT Voltage . . . . .	-0.3 to V <sub>IN</sub>
Output Current . . . . .	Self Limiting
Input Voltage (B0, B1, B2, B3, I <sub>MAX</sub> , SHTDWN) . . . . .	-0.3 to V <sub>IN</sub>
Storage Temperature Range . . . . .	-65°C to +150°C
Operating Junction Temperature Range . . . . .	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . .	+300°C

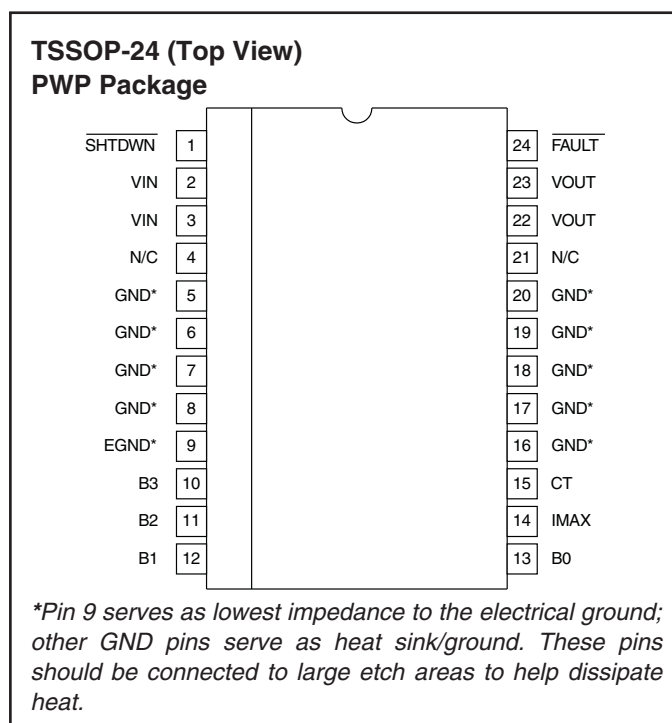
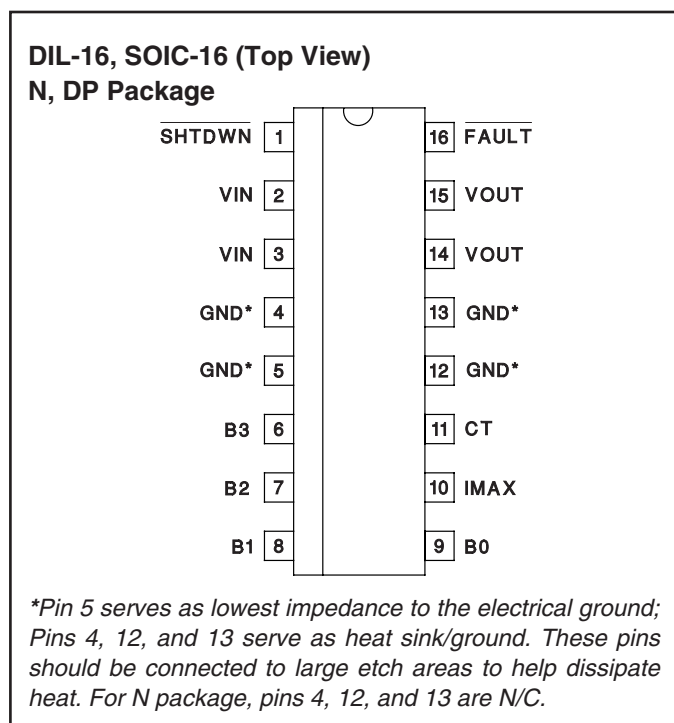
*Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.*

**DESCRIPTION (cont.)**

The UCC3912 is designed for unidirectional current flow, emulating an ideal diode in series with the power switch. This feature is particularly attractive in applications where many devices are powering a common bus, such as with SCSI Termpwr.

The UCC3912 can be put into sleep mode drawing only 1µA of supply current. The SHTDWN pin has a preset threshold hysteresis which allows the user the ability to set a time delay upon start-up to achieve sequencing of power. Other features include an open drain FAULT output indicator, Thermal Shutdown, Under Voltage Lock-out, and a low thermal resistance Small outline package.

**CONNECTION DIAGRAMS**



**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for T<sub>J</sub> = 0°C to 70°C, V<sub>IN</sub> = 5V, I<sub>MAX</sub> = 0.4V, SHTDWN = 2.4V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Supply Section</b>					
Voltage Input Range		3.0		8.0	V
Supply Current			1.0	2.0	mA
Sleep Mode Current	SHTDWN = 0.2V		0.5	5.0	µA
<b>Output Section</b>					
Voltage Drop	I <sub>OUT</sub> = 1A		0.15	0.22	V
	I <sub>OUT</sub> = 2A		0.3	0.45	V
	I <sub>OUT</sub> = 3A		0.45	0.68	V
	I <sub>OUT</sub> = 1A, V <sub>IN</sub> = 3V		0.17	0.27	V
	I <sub>OUT</sub> = 2A, V <sub>IN</sub> = 3V		0.35	0.56	V
	I <sub>OUT</sub> = 3A, V <sub>IN</sub> = 3V		0.5	0.8	V

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_J = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $I_{MAX} = 0.4\text{V}$ ,  $SHTDWN = 2.4\text{V}$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Output Section (cont.)</b>					
Reverse Leakage Current	$V_{IN} < V_{OUT}$ , $\overline{SHTDWN} = 0.2\text{V}$ , $V_{OUT} = 5\text{V}$		5	20	$\mu\text{A}$
Initial Start-up Time	(Note 2)		100		$\mu\text{s}$
Short Circuit Response	(Note 2)		100		ns
Thermal Shutdown	(Note 2)		170		$^\circ\text{C}$
Thermal Hysteresis	(Note 2)		10		$^\circ\text{C}$
<b>DAC Section</b>					
Output Leakage	Code = 0000-0011		0	20	$\mu\text{A}$
Trip Current	Code = 0100	0.1	0.25	0.45	A
	Code = 0101	0.25	0.50	0.75	A
	Code = 0110	0.5	0.75	1.0	A
	Code = 0111	0.75	1.00	1.25	A
	Code = 1000	1.0	1.25	1.5	A
	Code = 1001	1.25	1.50	1.75	A
	Code = 1010	1.5	1.75	2.0	A
	Code = 1011	1.7	2.00	2.3	A
	Code = 1100	1.9	2.25	2.58	A
	Code = 1101	2.1	2.50	2.9	A
	Code = 1110	2.3	2.75	3.2	A
Code = 1111	2.5	3.0	3.5	A	
Max Output Current	Code = 0000 to 0011			0.02	mA
Max Output Current Over Trip (Current Source Mode)	Code = 0100 to 1111, $I_{MAX} = 0\text{V}$	0.5	1.0	1.8	A
Max Output Current (Current Source Mode)	Code = 0100 to 1111, $I_{MAX} = 2.4\text{V}$	3.0	4.0	5.2	A
<b>Timer Section</b>					
CT Charge Current	$V_{CT} = 1.0\text{V}$	-45.0	-36.0	-22.0	$\mu\text{A}$
CT Discharge Current	$V_{CT} = 1.0\text{V}$	0.72	1.2	1.5	$\mu\text{A}$
Output Duty Cycle	$V_{OUT} = 0\text{V}$	2.0	3.0	6.0	%
CT Fault Threshold		1.3	1.5	1.7	V
CT Reset Threshold		0.4	0.5	0.6	V
<b>Shutdown Section</b>					
Shutdown Threshold		1.1	1.5	1.9	V
Shutdown Hysteresis			100		mV
Input Current	$\overline{SHTDWN} = 1\text{V}$		100	500	nA
<b>Fault Output Section</b>					
Output Leakage Current				500	nA
Low Level Output Voltage	$I_{OUT} = 10\text{mA}$		0.4	0.8	V
<b>TTL Input DC Characteristics Section</b>					
TTL Input Voltage High	(can be connected to $V_{IN}$ )	2.0			V
TTL Input Voltage Low				0.8	V
TTL Input High Current	$V_{IH} = 2.4\text{V}$		3	10	$\mu\text{A}$
TTL Input Low Current	$V_{IL} = 0.4\text{V}$			1	$\mu\text{A}$

**Note 1:** All voltages are with respect to Ground. Current is positive into and negative out of the specified terminal.

**Note 2:** Guaranteed by design. Not 100% tested in production.

**PIN DESCRIPTIONS**

**B0 - B3:** These pins provide digital input to the DAC which sets the fault current threshold. They can be used to provide a digital soft-start, adaptive current limiting.

**CT:** A capacitor connected to ground sets the maximum fault time. The maximum fault time must be more than the time to charge the external capacitance in one cycle. The maximum fault time is defined as  $FAULT = 27.8 \cdot 10^3 \cdot CT$ . Once the fault time is reached the output will shut-down for a time given by:  $T_{SD} = 833 \cdot 10^3 \cdot CT$ , this equates to a 3% duty cycle.

**FAULT:** Open drain output which pulls low upon any condition which causes the output to open: Fault, Thermal Shutdown, or Shutdown.

**IMAX:** When this pin is set to logic low the maximum sourcing current will always be 1A above the pro-

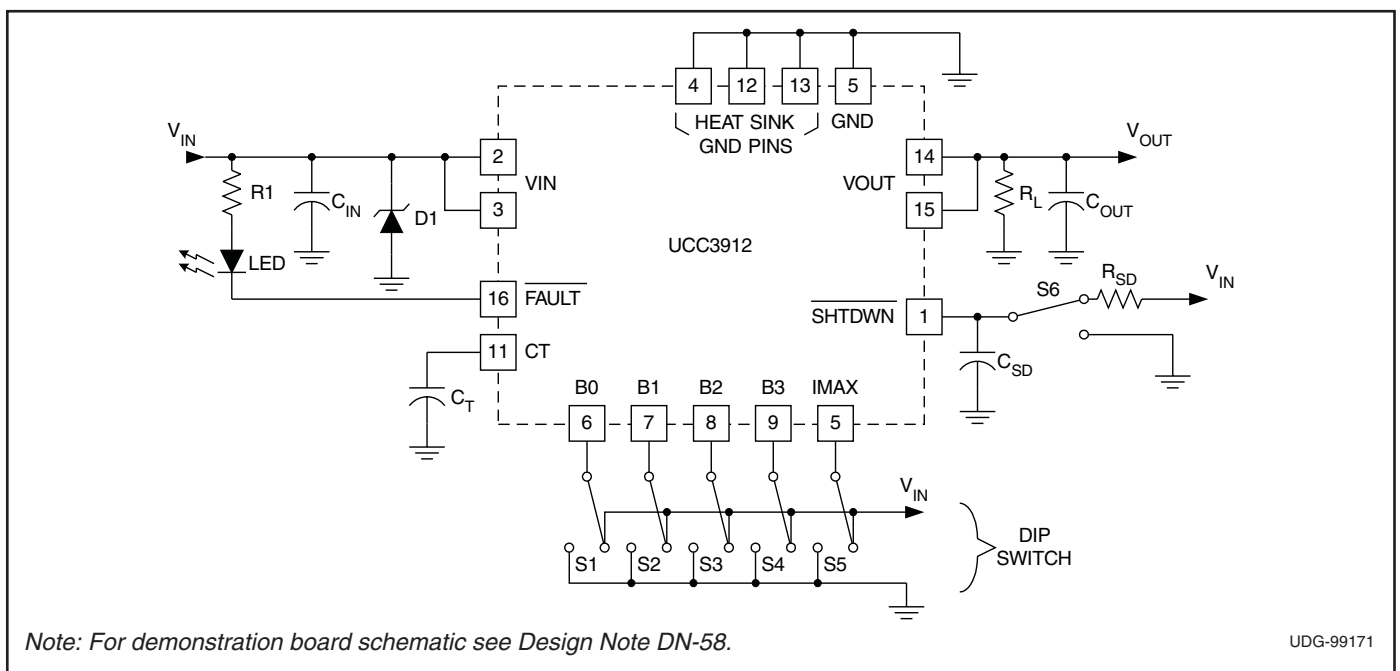
grammed fault level. When set to logic high, the maximum sourcing current will be a constant 4A for applications which require fast charging of load capacitance.

**SHTDWN:** When this pin is brought to a logic low, the IC is put into a sleep mode drawing typically less than  $1\mu A$  of  $I_{CC}$ . The input threshold is hysteretic, allowing the user to program a start-up delay with an external RC circuit.

**VIN:** Input voltage to the UCC3912. The recommended voltage range is 3 to 8 volts. Both VIN pins should be connected together and to the power source.

**VOUT:** Output voltage from the UCC3912. When switched the output voltage will be approximately  $V_{IN} - (0.15\Omega \cdot I_{OUT})$ . Both VOUT pins should be connected together and to the load.

**APPLICATION INFORMATION**



**Figure 1. Evaluation circuit.**

**Protecting The UCC3912 From Voltage Transients**

The parasitic inductance associated with the power distribution can cause a voltage spike at  $V_{IN}$  if the load current is suddenly interrupted by the UCC3912. It is important to limit the peak of this spike to less than 8V to prevent damage to the UCC3912. This voltage spike can be minimized by:

- Reducing the power distribution inductance (e.g., twist the “+” and “-” leads of the power supply feeding  $V_{IN}$ , locate the power supply close to the UCC3912, use a PCB ground plane,...etc.).
- Decoupling  $V_{IN}$  with a capacitor,  $C_{IN}$  (refer to Fig. 1), located close to pins 2 and 3. This capacitor is typically less than  $1\mu F$  to limit the inrush current.
- Clamping the voltage at  $V_{IN}$  below 8V with a Zener diode, D1 (refer to Fig. 1), located close to pins 2 and 3.

APPLICATION INFORMATION (cont.)

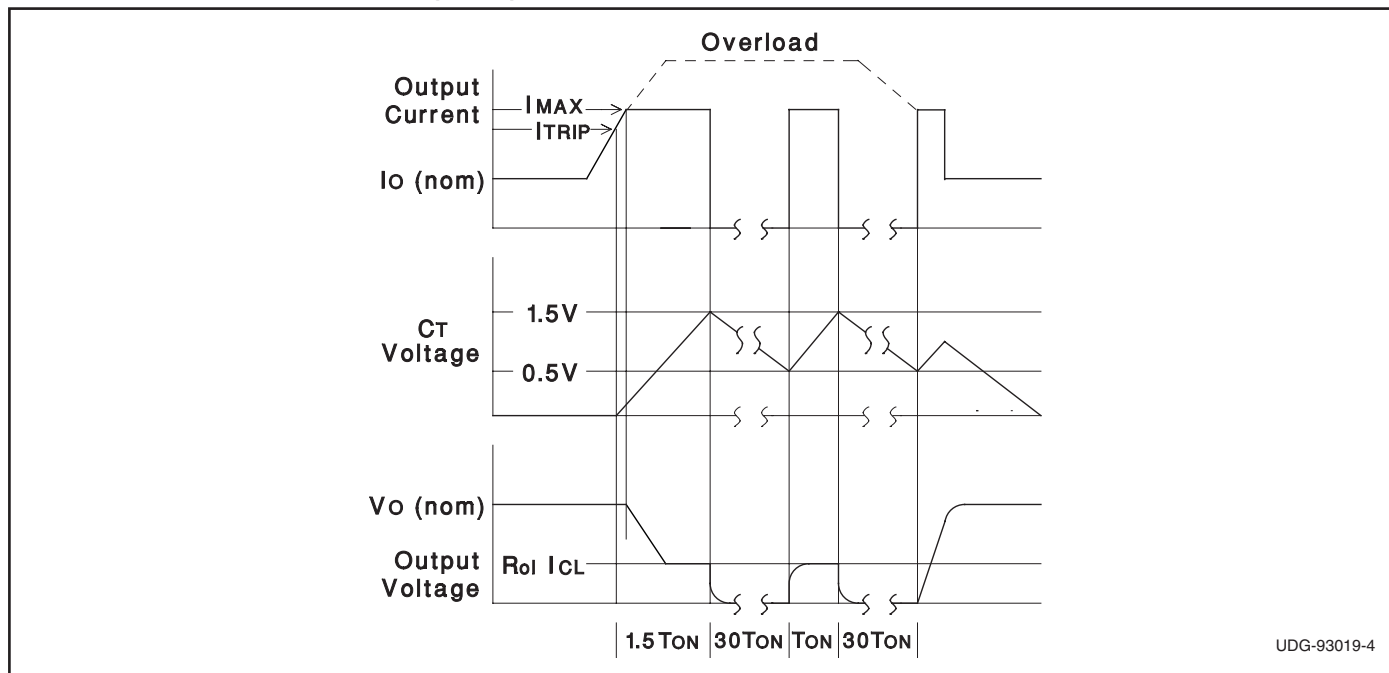


Figure 2. Load current, timing capacitor voltage, and output voltage of the UCC3912 under Fault conditions.

Estimating Maximum Load Capacitance

For hot swap applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current current-limited controller, the output will come up if the load asks for less than the maximum available short-circuit current.

To guarantee recovery of a duty-cycle from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time (Fault time). The design value of ON or Fault time can be adjusted by changing the timing capacitor  $C_T$ .

For worst-case constant-current load of value just less than the trip limit;  $C_{OUT(max)}$  can be estimated from:

$$C_{OUT(max)} \approx (I_{MAX} - I_{LOAD}) \cdot \left( \frac{28 \cdot 10^3 \cdot C_T}{V_{OUT}} \right)$$

where  $V_{OUT}$  is the output voltage.

For a resistive load of value  $R_L$ , the value of  $C_{OUT(max)}$  can be estimated from:

$$C_{OUT(max)} \approx \left( \frac{28 \cdot 10^3 \cdot C_T}{R_L \cdot \ln \left( \frac{1}{1 - \left( \frac{V_{OUT}}{I_{MAX} \cdot R_L} \right)} \right)} \right)$$

**APPLICATION INFORMATION (cont.)**

The overcurrent comparator senses both the DAC output and a representation of the output current. When the output current exceeds the programmed level the timing capacitor  $C_T$  charges with  $36\mu A$  of current. If the fault occurs for the time it takes for  $C_T$  to charge up to  $1.5V$ , the fault latch is set and the output switch is opened. The output remains opened until  $C_T$  discharges to  $0.5V$  with a

$1.2\mu A$  current source. Once the  $0.5V$  is reached the output is enabled and will either appear as a switch, if the fault is removed, or a current source if the fault remains. If the over current condition is still present then  $C_T$  will begin charging, starting the cycle over, resulting in approximately a 3% on time.

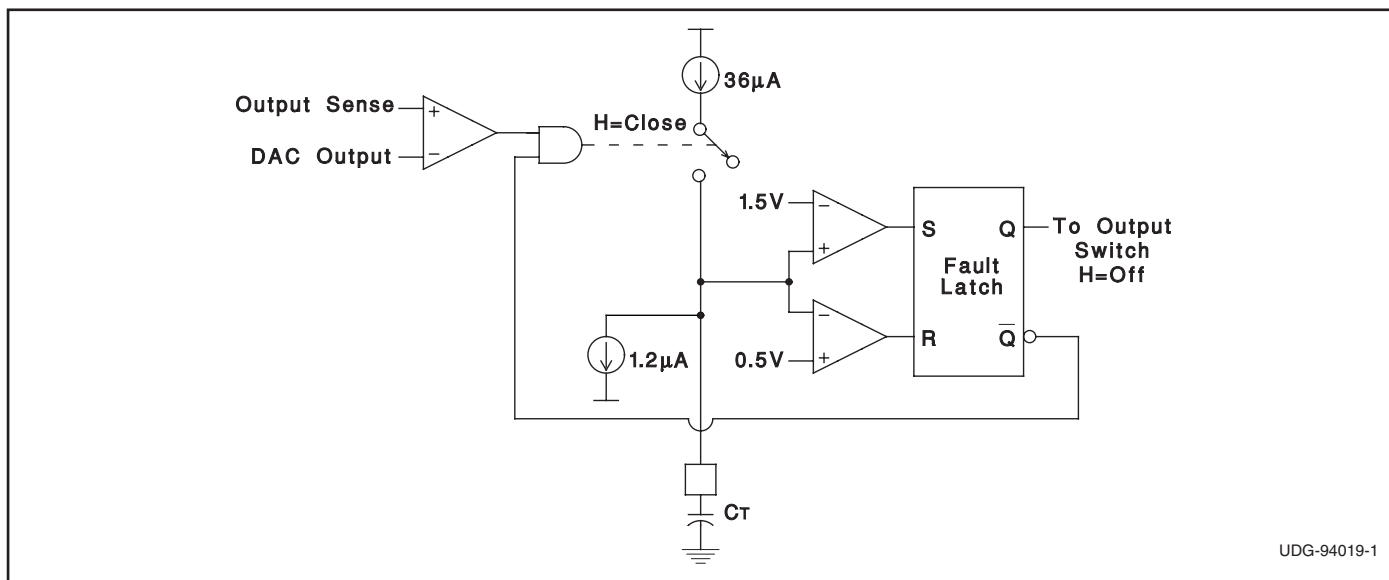


Figure 3. UCC3912 on time control circuitry.

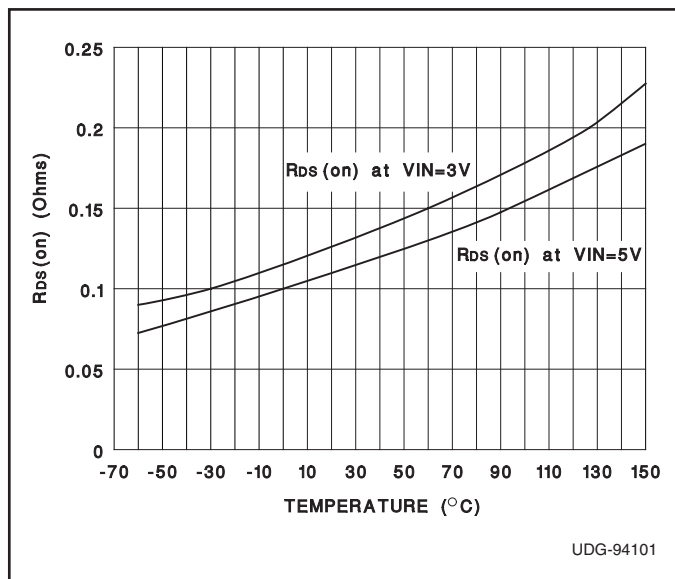


Figure 4. RDS(on) vs temperature at 2A load current.

**SAFETY RECOMMENDATIONS**

Although the UCC3912 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3912 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3912 will prevent the fuse from blowing virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

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