



# Low Voltage Differential (LVD) SCSI 9 Line Terminator

## **FEATURES**

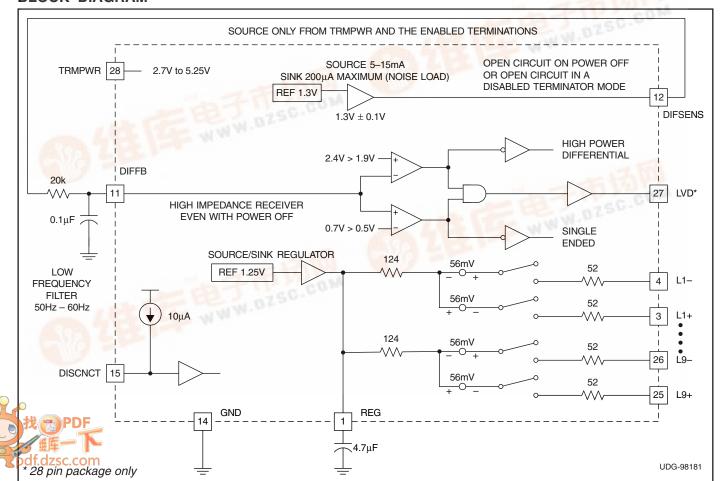
- First LVD only Active Terminator
- Meets SCSI SPI-2 Ultra2 (Fast-40) and Ultra3 / Ultra160 (Fast-80) Standards
- 2.7V to 5.25V Operation
- Differential Failsafe Bias

## **DESCRIPTION**

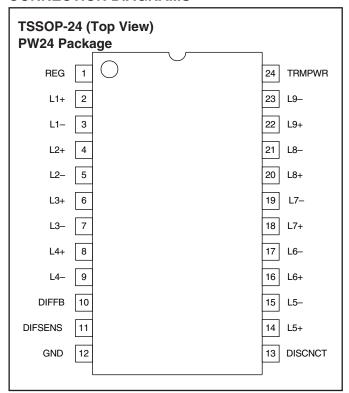
The UCC5640 is an active terminator for Low Voltage Differential (LVD) SCSI networks. This LVD only design allows the user to reach peak bus performance while reducing system cost. The device is designed as an active Y-terminator to improve the frequency response of the LVD Bus. Designed with a 1.5pF channel capacitance, the UCC5640 allows for minimal bus loading for a maximum number of peripherals. With the UCC5640, the designer will be able to comply with the Fast-40 SPI-2 and Fast-80 SPI-3 specifications. The UCC5640 also provides a much-needed system migration path for ever improving SCSI system standards. This device is available in the 24 pin TSSOP and 28 pin TSSOP for ease of layout use.

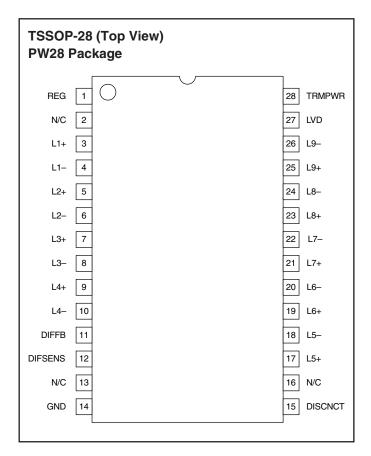
The UCC5640 is not designed for use in single ended or high voltage differential systems.

## **BLOCK DIAGRAM**



#### **CONNECTION DIAGRAMS**





## **ABSOLUTE MAXIMUM RATINGS**

TERMPWR Voltage+6V
Signal Line Voltage
Package Dissipation1W
Storage Temperature65°C to +150°C
Junction Temperature
Lead Temperature (Soldering, 10 sec.) +300°C

Currents are positive into negative out of the specified terminal. consult Packaging Section of Databook for thermal limitations and considerations of package.

# **RECOMMENDED OPERATING CONDITIONS**

TERMPWR Voltage . . . . . . . . . . . . . . . 2.7V to 5.25V

# **ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, specifications apply for $T_A = 0$ °C to 70°C,

TRMPWR = 3.3V.  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS			
TRMPWR Supply Current Section								
TRMPWR Supply Current	No Load			25	mA			
	Disabled Terminator			400	μΑ			
TRMPWR Voltage		2.7		5.25	V			

# **ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, specifications apply for T<sub>A</sub> = 0°C to 70°C,

TRMPWR = 3.3V.  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Section					
1.25V Regulator	DIFSENS connected to DIFFB	1.15	1.25	1.35	V
1.25V Regulator Source Current	DIFSENS connected to DIFFB		-100	-80	mA
1.25V Regulator Sink Current	DIFSENS connected to DIFFB	80	100		mA
1.3V Regulator	DIFFB connected to GND	1.2	1.3	1.4	V
1.3V Regulator Source Current	DIFSENS to GND	-15		-5	mA
1.3V Sink Current	DIFSENS to 3.3V	50		200	μА
Differential Termination Section					
Differential Impedance	-2.5mA to 4.5mA	100	105	110	Ω
Common Mode Impedance	L+ connected to L-	110	150	165	Ω
Differential Bias Voltage	No load, L+ or L-	100		125	mV
Common Mode Bias		1.15	1.25	1.35	V
Output Leakage, Disconnect	DISCNCT, TRMPWR = 0 to 5.25V, $V_{LINE} = 0.2$ to 5.25V		10	400	nA
Output Capacitance	Single ended measurement to ground (Note 1)			3	pF
Low Voltage Differential (LVD) Status Bit So	ection				
Isource	$V_{LOAD} = 2.4V$		-6	-4	mA
ISINK	$V_{LOAD} = 0.4V$	2	5		mA
<b>Disconnect &amp; Differential Sense Input Secti</b>	on				
DISCNCT Threshold		0.8		2	V
Input Current	At 0V and 3.3V	-30	-10		μА
Differential Sense SE to LVD Threshold		0.5		0.7	V
Differential Sense LVD to HPD Threshold		1.9		2.4	V

Note 1: Guaranteed by design. Not 100% tested in production.

#### PIN DESCRIPTION

**DIFFB:** Differential sense filter pin should be connected to a  $0.1\mu F$  capacitor and  $20k\Omega$  resistor to Diff Sense.

**DIFSENS:** The SCSI bus differential sense line to detect what type of devices are connected to the SCSI Bus.

**DISCNCT:** Disconnect pin shuts down the terminator when it is not at the end of the bus.

GND: Ground.

**Ln** -: Negative line in differential applications for the SCSI Bus.

**Ln** +: Positive line for differential applications for the SCSI Bus.

**LVD:** (28 pin package only) Indicates that the bus is in LVD mode.

**REG:** Regulator bypass; must be connected to a  $4.7\mu F$  capacitor to ground.

**TRMPWR:** V<sub>IN</sub> 2.7V to 5.25V power supply.

# **APPLICATION INFORMATION**

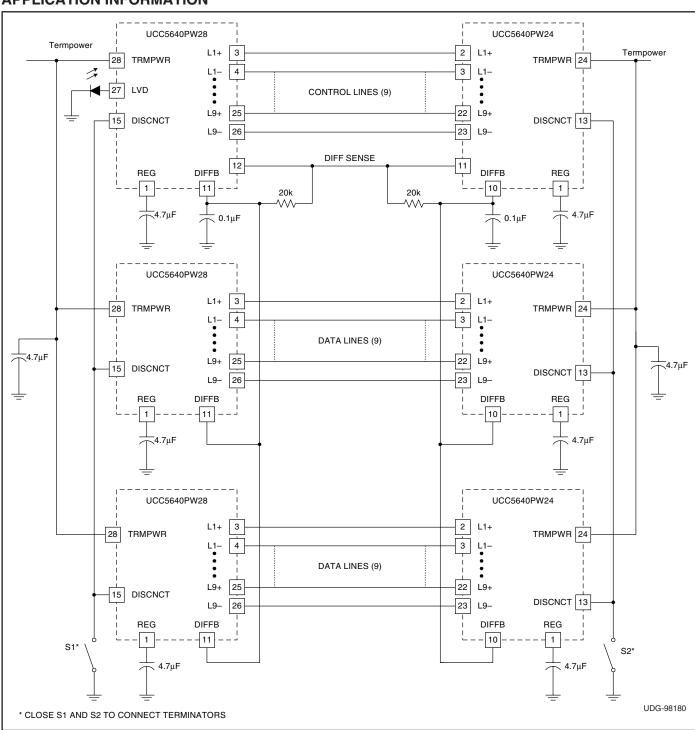


Figure 1. Application diagram.

#### **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 2000, Texas Instruments Incorporated