UCC561

U UNITRODE

Low Voltage Differential SCSI (LVD) 27 Line Regulator Set

FEATURES

- SCSI SPI-2 LVD SCSI 27 Line Low Voltage Differential Regulator

- 2.7V to 5.25V Operation

- Integrated Regulator Set for LVD SCSI

- Differential Failsafe Bias

DESCRIPTION

The UCC561 LVD Regulator set is designed to provide the correct references voltages and bias currents for LVD termination resistor networks (475Ω, 121Ω, and 475Ω). The device also provides a 1.3V output for Diff Sense signaling. With the proper resistor network, the UCC561 solution will meet the common mode bias impedance, differential bias, and termination impedance requirements of SPI-2 (Ultra2) and SPI-3 (Ultra3).

This device incorporates into a single monolith, two sink/source reference voltage regulators, a 1.3V buffered output and protection features. The protection features include thermal shut down and active current limiting circuitry. The UCC561 is offered in 16-pin SOIC(DP) package.
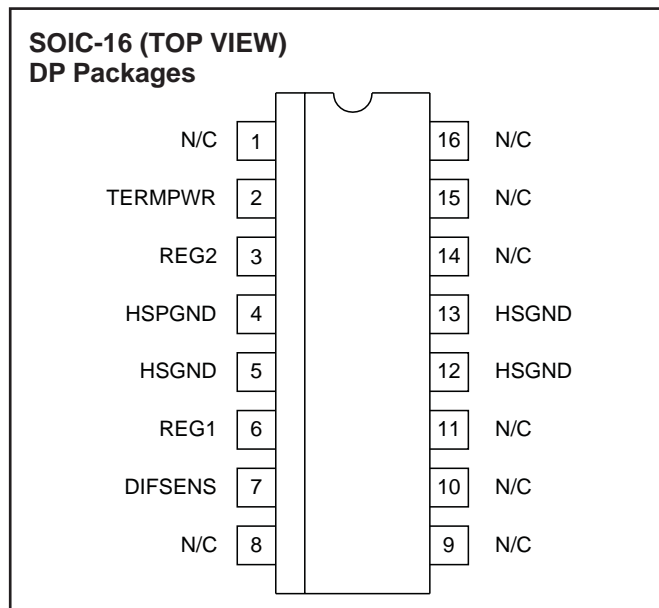
BLOCK DIAGRAM

UDG-98093
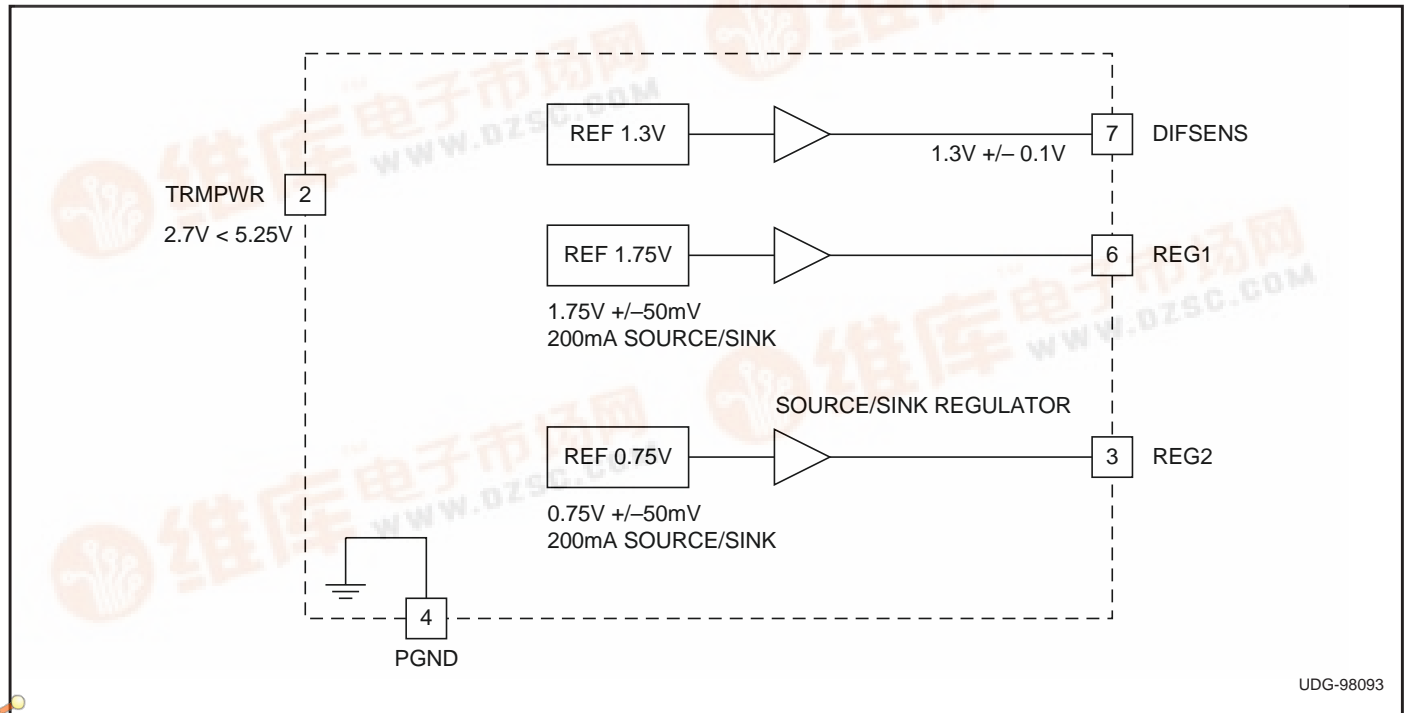
ABSOLUTE MAXIMUM RATINGS

TERMPWR . . . . +6V
Package Dissipation 1.2W
Junction Temperature. . . . . –55°C to +150°C
Storage Temperature . . . . –65°C to +150°C

*Currents are positive into, negative out of the specified termi-
nal. Consult Packaging Section of Databook for thermal limita-
tions and considerations of packages.*

RECOMMENDED OPERATING CONDITIONS

TERMPWR Voltage . . . . 2.7V to 5.25V

CONNECTION DIAGRAMS

SOIC-16 (TOP VIEW)
DP Packages

N/C	1		16	N/C
TERMPWR	2		15	N/C
REG2	3		14	N/C
HSPGND	4		13	HSGND
HSGND	5		12	HSGND
REG1	6		11	N/C
DIFSENS	7		10	N/C
N/C	8		9	N/C

ELECTRICAL CHARACTERISTICS:
Unless otherwise specified these specifications apply for TA = 0°C to 70°C,
TERMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TERMPWR Supply Current Section					
TERMPWR Supply Current	No Load			40.0	mA
TERMPWR Voltage		2.7		5.25	V
Regulator Section					
1.75 Volt Regulator	REG1 (± 125mA)	1.7	1.75	1.8	V
1.3 Volt Regulator	DIFSENS , No Load	1.2	1.3	1.4	V
0.75 Volt Regulator	REG2 (± 125mA)	0.7	0.75	0.8	V
1.75 Volt Regulator Source Current	V_O = 1.25			−200	mA
1.75 Volt Regulator Sink Current	V_O = 2.25	200			mA
1.75 Volt Sink Current Limit				700	mA
1.75 Volt Source Current Limit		−700			mA
1.3 Volt Regulator Source Current	DIFSENS, GND	−5		−15	mA
1.3 Volt Regulator Sink Current	DIFSENS, 2.4V	50		200	μA
0.75 Volt Regulator Source Current	V_O = 0.25			−200	mA
0.75 Volt Regulator Sink Current	V_O = 1.25	200			mA
0.75 Source Current Limit				700	mA
0.75 Sink Current Limit		−700			mA

Note 1: Guaranted by design. Not 100% tested in production.

APPLICATION INFORMATION
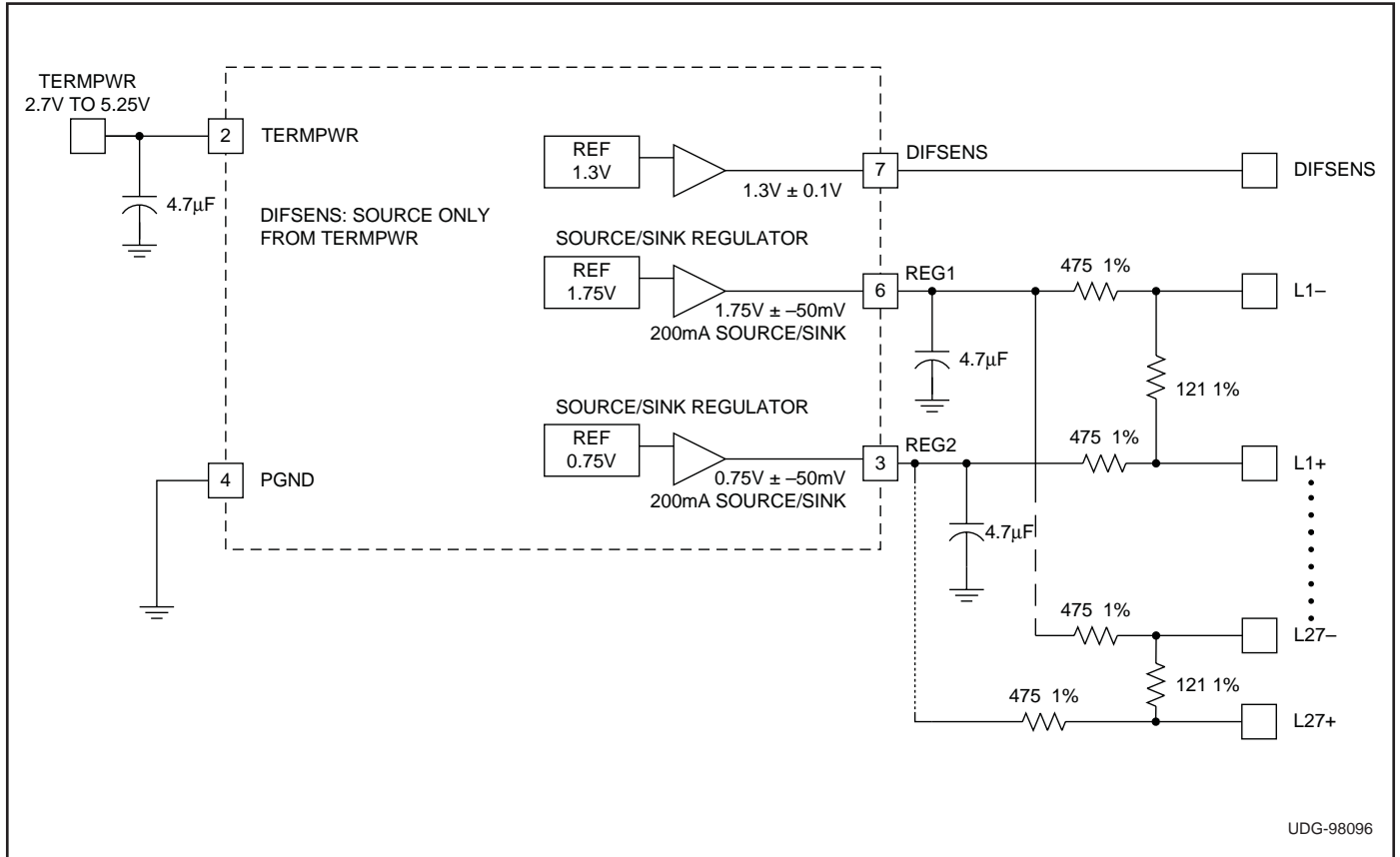
Figure 1. LVD SCSI discrete resistor stack.

Table I. Resistor stack vs. standard.

Outputs	Specification
107.3Ω Diff	100Ω to 110Ω
112.9mV Diff Bias	100mV to 125mV
237Ω Common Mode	100Ω to 300Ω
1.25V Common Mode	1.2V to 1.30V

Application Note: The resistor stack with the 1.75V and 0.75V reference will give the correct differential impedance, bias voltage, common mode differential impedance and common mode voltage as show in Table 1.

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