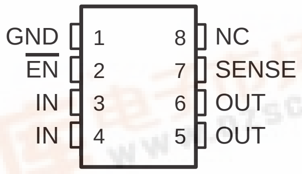
TPS71025
LOW-DROPOUT VOLTAGE REGULATOR

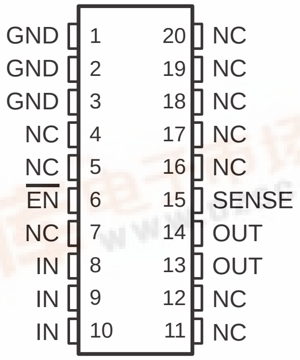
SLVS162A – MAY 1997 – REVISED MAY 1998

- **2.5-V Fixed-Output Regulator**
- **Very Low-Dropout (LDO) Voltage . . . 57 mV Typical at I_O = 100 mA**
- **Very Low Quiescent Current, Independent of Load . . . 292 µA Typ**
- **Extremely Low Sleep-State Current, 0.5 µA Max**
- **2% Tolerance Over Specified Conditions**
- **Output Current Range . . . 0 mA to 500 mA**
- **Available in Space Saving 8-Pin SOIC and 20-Pin TSSOP Packages**
- **0°C to 125°C Operating Junction Temperature Range**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS71025 low-dropout regulator offers an order of magnitude reduction in both dropout voltage and quiescent current over conventional LDO performance. The improvement results from replacing the typical pnp pass transistor with a PMOS device.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (maximum of 95 mV at an output current of 100 mA) and is directly proportional to the output current (see Figure 1). Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and remains independent of output loading (typically 292 µA over the full range of output current, 0 mA to 500 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. The TPS71025 also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to 0.5 µA maximum at T_J = 25°C.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)			PACKAGED DEVICES			CHIP FORM (Y)
	MIN	TYP	MAX	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 125°C	2.45	2.5	2.55	TPS71025D	TPS71025P	TPS71025PWLE	TPS71025Y

The D package is availabe taped and reeled. Add R suffix to device type (e.g., TPS71025DR). The PW package is only available left-end taped and reeled and is indicated by the LE suffix on the device type.

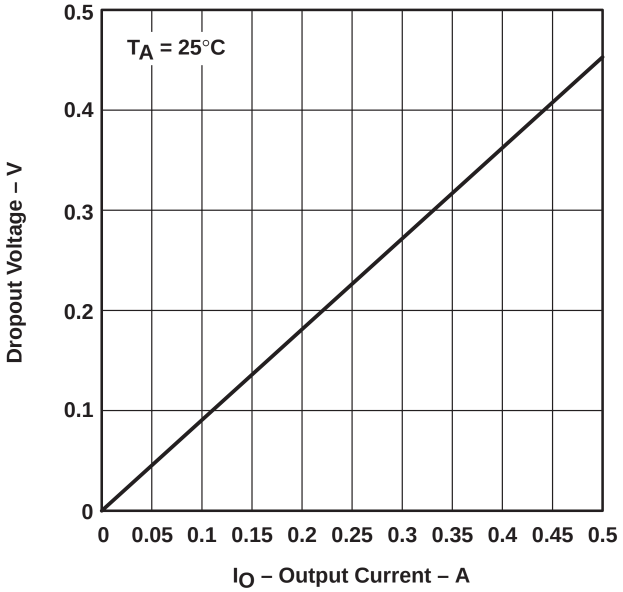
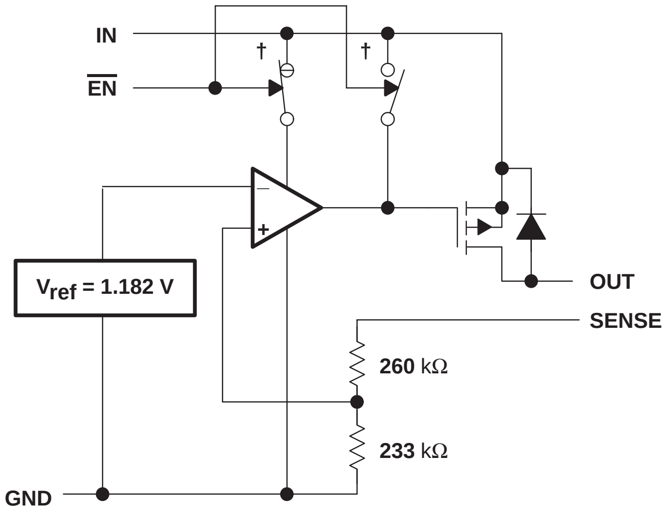


Figure 1. Dropout Voltage Versus Output Current

functional block diagram



[†] Switch positions are shown with EN low (active).

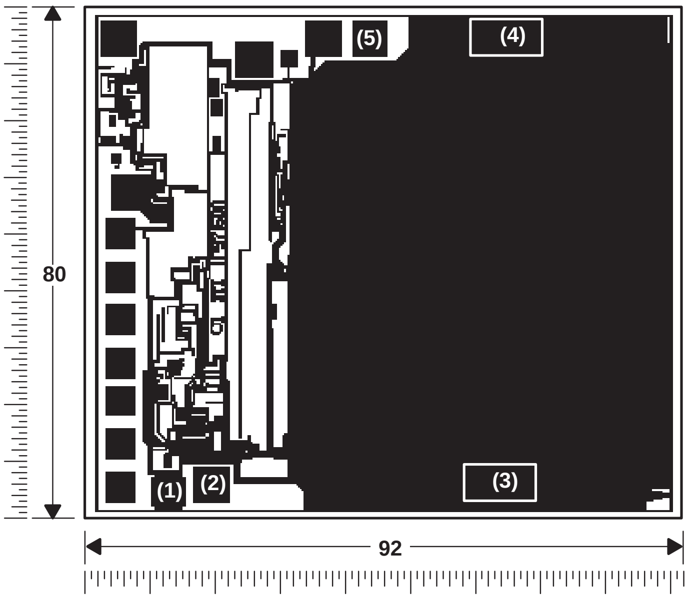
Terminal Functions

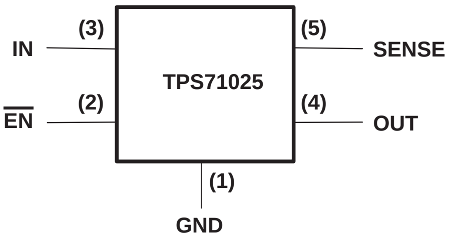
TERMINAL			DESCRIPTION
NAME	NO.		
	D or P	PW	
$\overline{\text{EN}}$	2	6	Enable input. Logic low enables output
GND	1	1–3	Ground
IN	3, 4	8–10	Input supply voltage
OUT	5, 6	13, 14	Output voltage
SENSE	7	15	Output voltage sense input

TPS71025Y chip information

These chips, when properly assembled, display characteristics similar to those of the TPS71025. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

NOTE A: For most applications, OUT and SENSE should be tied together as close as possible to the device; for other implementations, refer to SENSE-pin connection discussion in the Application Information section of this data sheet.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Input voltage range, V_I, $\overline{EN}$ (see Note 1)	–0.3 V to 11 V
Continuous output current, I_O	2 A
Continuous total power dissipation	See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J	–0°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE[‡]

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
P	1175 mW	9.4 mW/°C	752 mW	235 mW
PW	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE[‡]

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 70°C$ POWER RATING	$T_C = 125°C$ POWER RATING
D	2188 mW	17.5 mW/°C	1400 mW	438 mW
P	2738 mW	21.9 mW/°C	1752 mW	548 mW
PW	4025 mW	32.2 mW/°C	2576 mW	805 mW

[‡] Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. For guidelines on maintaining junction temperature within recommended operating range, see the Thermal Information section.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	2.97	10	V
High-level input voltage at $\overline{EN}$, V_{IH}	2		V
Low-level input voltage at $\overline{EN}$, V_{IL}	0	0.5	V
Output current range, I_O	0	500	mA
Operating virtual junction temperature range, T_J	0	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$ = 3.5 V, I_O = 10 mA, $\overline{EN}$ = 0 V, C_o = 4.7 μF/CSR[†] = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS[‡]		T_J	MIN	TYP	MAX	UNIT
Output voltage	3.5 V ≤ V_I ≤ 10 V		25°C		2.5		V
			0°C to 125°C	2.45		2.55	
Dropout voltage	I_O = 10 mA,	V_I = 2.45 V	25°C		5.7	7.5	mV
			0°C to 125°C			10	
	I_O = 100 mA,	V_I = 2.45 V	25°C		57	95	
			0°C to 125°C			105	
	I_O = 500 mA,	V_I = 2.45 V	25°C		330	450	
			0°C to 125°C			500	
Pass-element series resistance			25°C		0.66	0.9	Ω
			0°C to 125°C			1	
Input regulation	V_I = 3.5 V to 10 V, 50 μA ≤ I_O ≤ 500 mA		25°C		7	23	mV
			0°C to 125°C		12.7	29	
Output regulation	I_O = 5 mA to 500 mA, 3.5 V ≤ V_I ≤ 10 V		25°C		18	38	mV
			0°C to 125°C			75	
	I_O = 50 μA to 500 mA, 3.5 V ≤ V_I ≤ 10 V		25°C		24	60	mV
			0°C to 125°C			120	
Ripple rejection	f = 120 Hz,	I_O = 50 μA	25°C	43	53		dB
			0°C to 125°C	40			
	f = 120 Hz,	I_O = 500 mA	25°C	39	51		
			0°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		$\mu V/\sqrt{Hz}$
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR = 1 Ω	C_o = 4.7 μF	25°C		274		μVrms
		C_o = 10 μF	25°C		228		
		C_o = 100 μF	25°C		159		
Quiescent current (active mode)	$\overline{EN}$ ≤ 0.5 V, 0 mA ≤ I_O ≤ 500 mA		25°C		292	390	μA
			0°C to 125°C			540	
Supply current (standby mode)	$\overline{EN}$ = V_I,	2.7 V ≤ V_I ≤ 10 V	25°C		18	475	nA
			0°C to 125°C			1900	
Output current limit	V_O = 0,	V_I = 10 V	25°C		1.07	2	A
			0°C to 125°C			2	
Pass-element leakage current in standby mode	$\overline{EN}$ = V_I,	2.7 V ≤ V_I ≤ 10 V	25°C		0.223	0.5	μA
			0°C to 125°C			1	
Output voltage temperature coefficient			0°C to 125°C		61	75	ppm/°C
Thermal shutdown junction temperature					165		°C
Logic high input voltage (standby mode), EN	2.5 V ≤ V_I ≤ 6 V		25°C	2			V
	6 V ≤ V_I ≤ 10 V		0°C to 125°C	2.7			
Logic low input voltage (active mode), $\overline{EN}$	2.7 V ≤ V_I ≤ 10 V		25°C			0.5	V
			0°C to 125°C			0.5	
Hysteresis voltage, $\overline{EN}$			0°C to 125°C		50		mV
Input current, $\overline{EN}$	0 V ≤ V_I ≤ 10 V		25°C	–0.5		0.5	μA
			0°C to 125°C	–0.5		0.5	
Input voltage, minimum for active pass element			25°C		2	2.5	V
			0°C to 125°C			2.5	

[†] CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_o.

[‡] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics at T_J = 25°C, $V_{I(IN)}$ = 3.5 V, I_O = 10 mA, $\overline{EN}$ = 0 V, C_o = 4.7 µF/CSR[†] = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS[‡]		TPS71025Y			UNIT
			MIN	TYP	MAX	
Output voltage	3.5 V ≤ V_I ≤ 10 V			2.5		V
Dropout voltage	I_O = 10 mA,	V_I = 2.45 V		5.7		mV
	I_O = 100 mA,	V_I = 2.45 V		57		
	I_O = 500 mA,	V_I = 2.45 V		330		
Pass-element series resistance				0.66		Ω
Input regulation	V_I = 3.5 V to 10 V			7		mV
Output regulation	I_O = 5 mA to 500 mA			18		mV
	I_O = 50 µA to 500 mA			24		mV
Ripple rejection	f = 120 Hz,	I_O = 50 µA		53		dB
	f = 120 Hz,	I_O = 500 mA		51		
Output noise-spectral density	f = 120 Hz			2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR = 1 Ω	C_O = 4.7 µF		274		µVrms
		C_O = 10 µF		228		
		C_O = 100 µF		159		
Quiescent current (active mode)	$\overline{EN}$ = 0 V, 0 mA ≤ I_O ≤ 500 mA			292		µA
Supply current (standby mode)	$\overline{EN}$ = V_I,	2.7 V ≤ V_I ≤ 10 V		18		nA
Output current limit	V_O = 0,	V_I = 10 V		1.07		A
Pass-element leakage current in standby mode	$\overline{EN}$ = V_I,	2.7 V ≤ V_I ≤ 10 V		0.223		µA
Output voltage temperature coefficient				61		ppm/°C
Thermal shutdown junction temperature				165		°C
Logic high input voltage (standby mode), $\overline{EN}$	2.5 V ≤ V_I ≤ 6 V		2			V
	6 V ≤ V_I ≤ 10 V		2.7			
Logic low input voltage (active mode), $\overline{EN}$	2.7 V ≤ V_I ≤ 10 V				0.5	V
Hysteresis voltage, $\overline{EN}$				50		mV
Input current, $\overline{EN}$	0 V ≤ V_I ≤ 10 V			0		µA
Input voltage, minimum for active pass element				2		V

[†] CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor , any series resistance added externally, and PWB trace resistance to C_O.

[‡] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TYPICAL CHARACTERISTICS

**OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

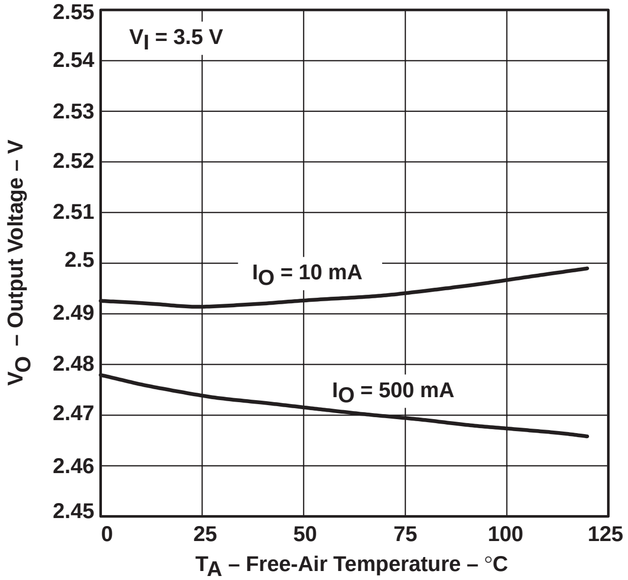


Figure 2

**DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

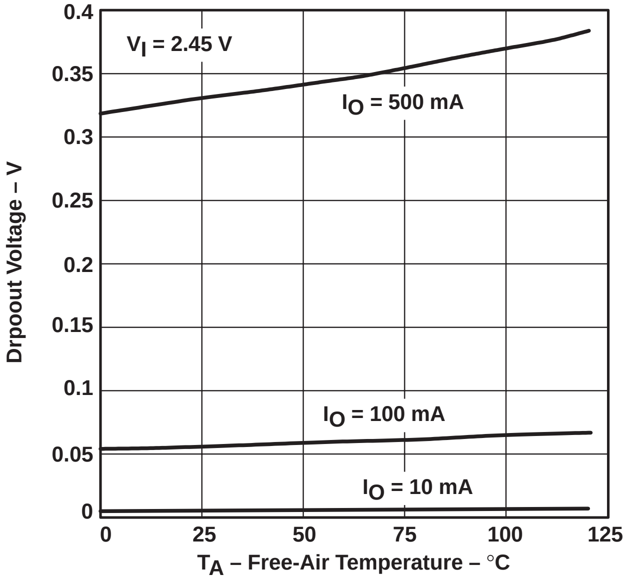


Figure 3

**OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

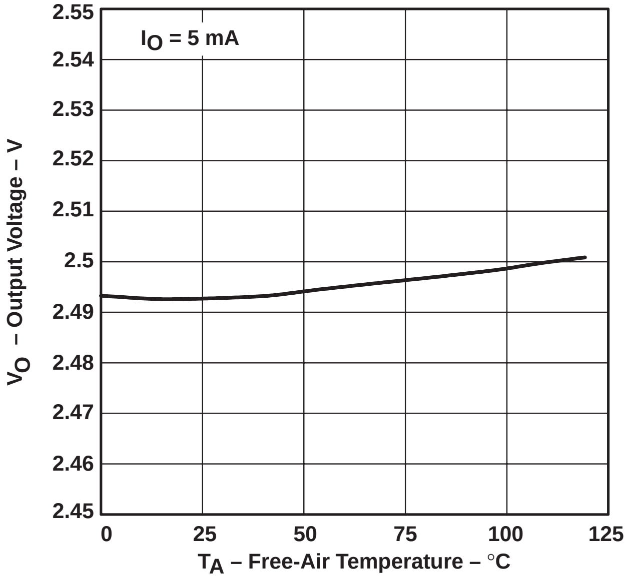


Figure 4

**OUTPUT VOLTAGE
vs
INPUT VOLTAGE**

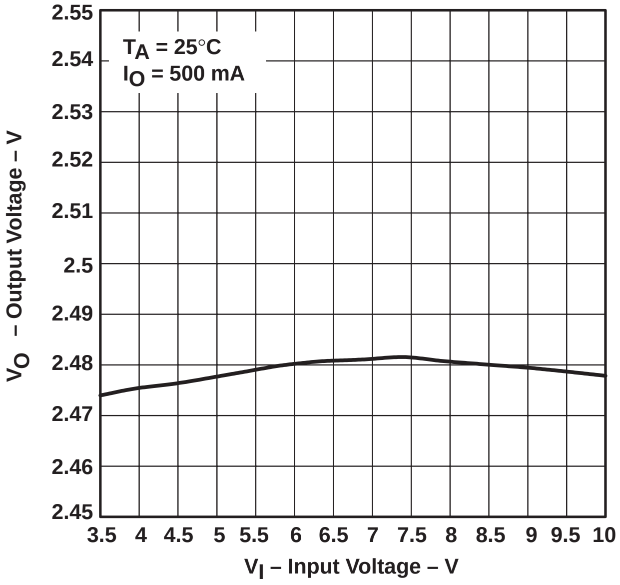


Figure 5

TYPICAL CHARACTERISTICS

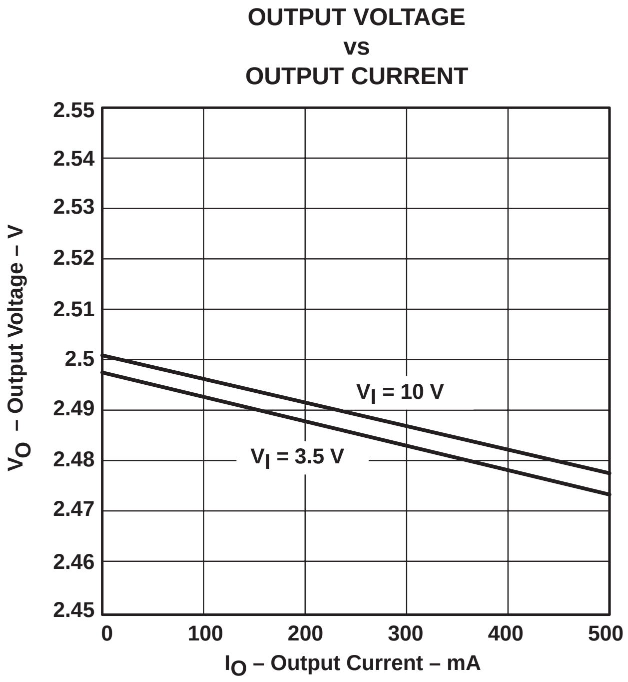

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

Figure 6

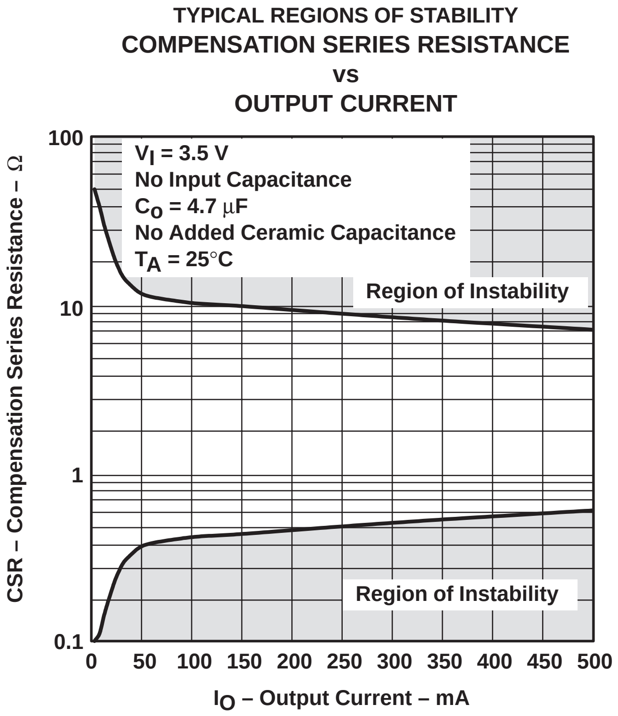

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

Figure 7

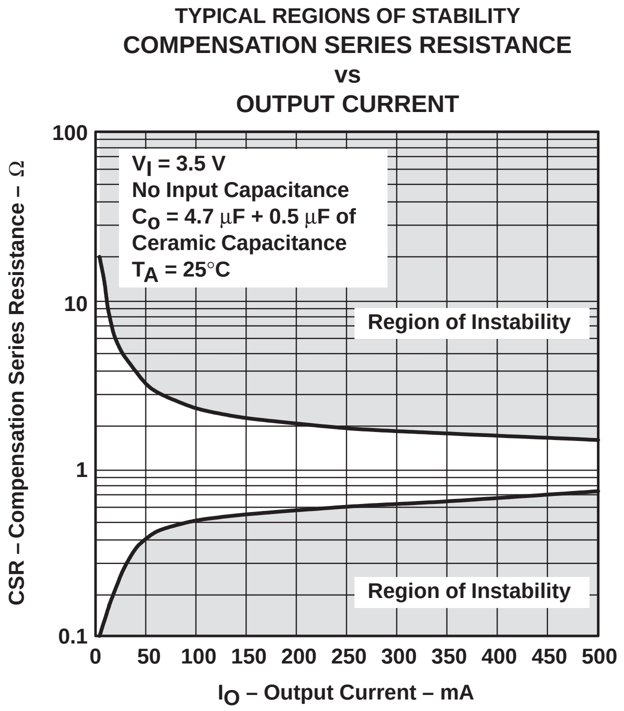

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

Figure 8

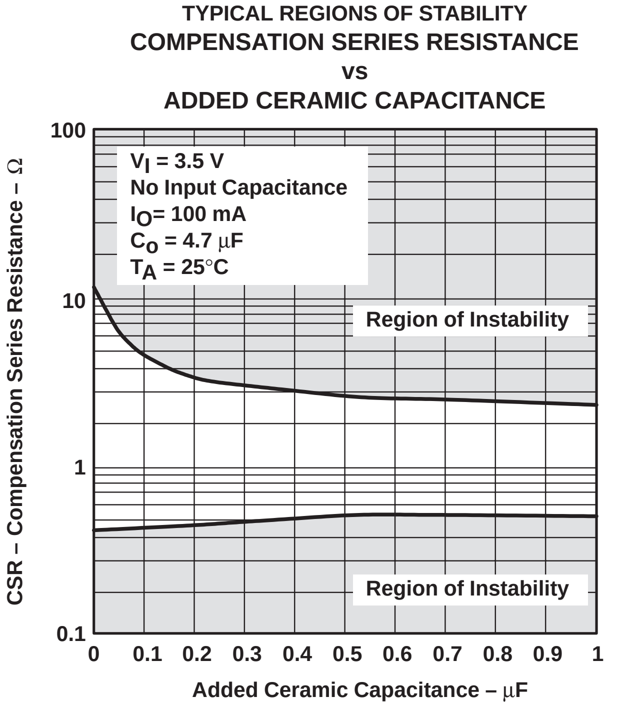

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

Figure 9

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

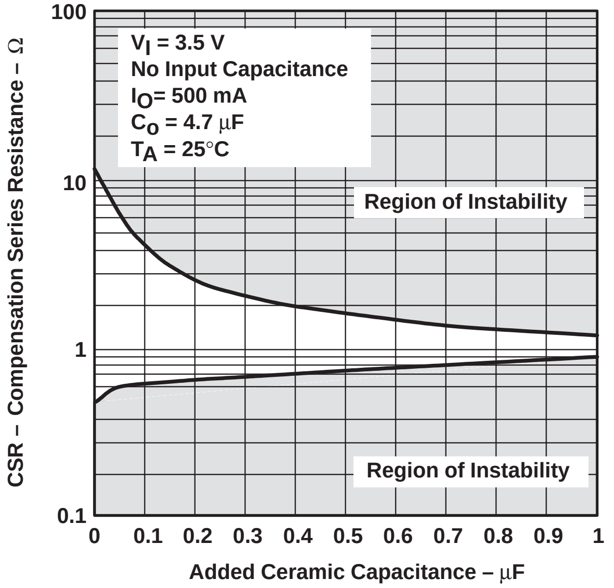


Figure 10

TYPICAL REGIONS OF STABILITY †
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

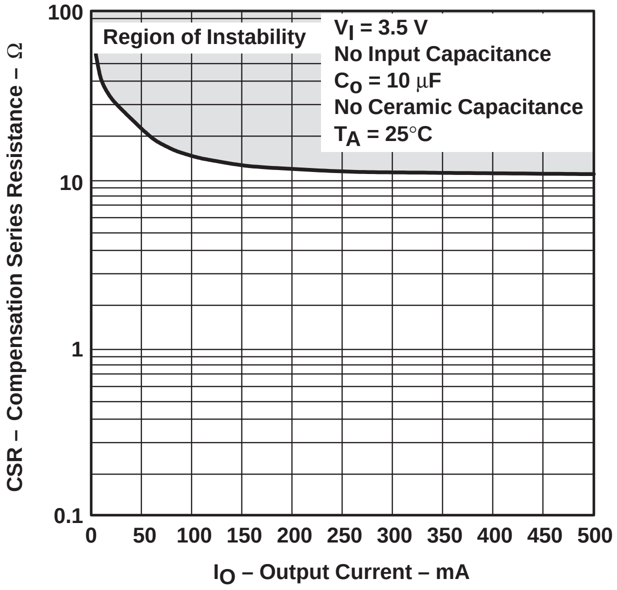


Figure 11

TYPICAL REGIONS OF STABILITY†
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

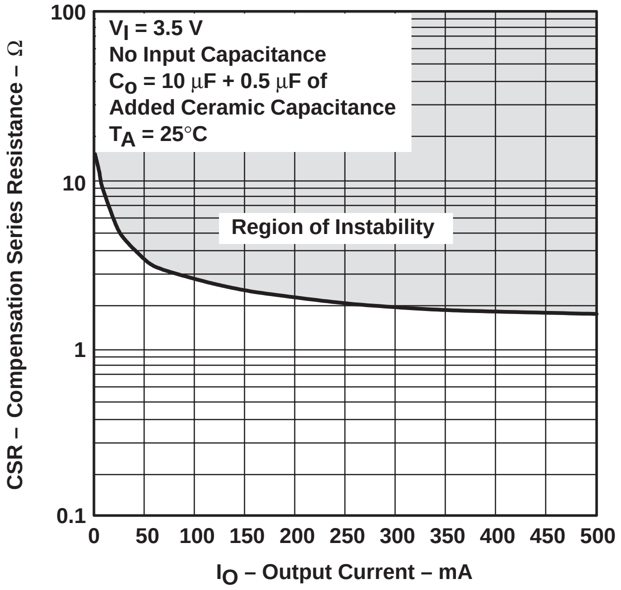


Figure 12

TYPICAL REGIONS OF STABILITY †
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

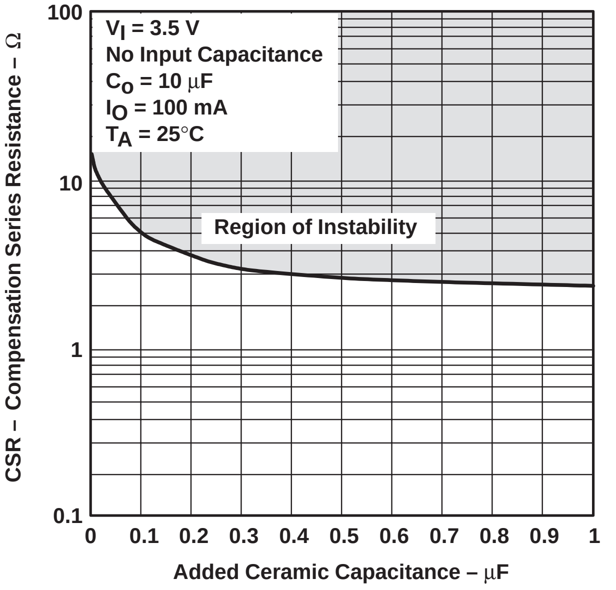


Figure 13

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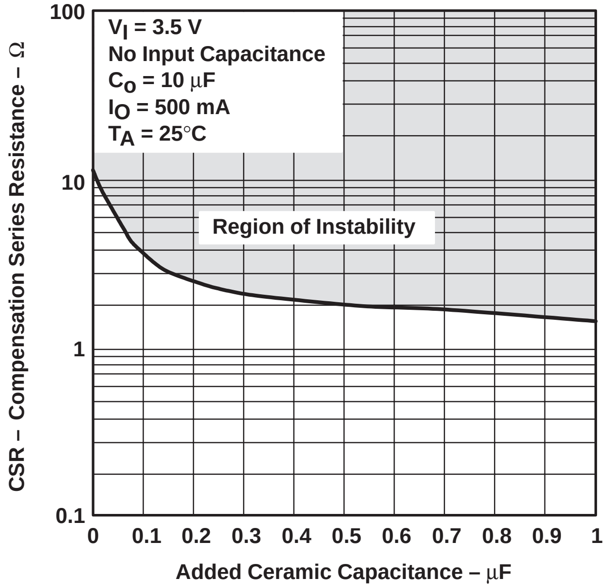
† CSR values below 0.1 Ω are not recommended.

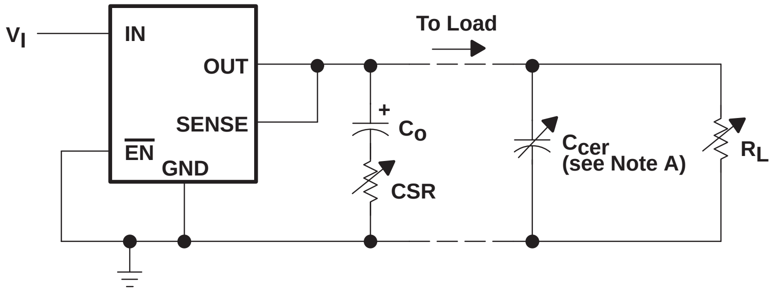
TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY†
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE



† CSR values below 0.1 Ω are not recommended.

Figure 14



NOTE A: Ceramic capacitor

Figure 15. Test Circuit for Typical Regions of Stability (Figures 7 through 14)

THERMAL INFORMATION

In response to system-miniaturization trends, integrated circuits are being offered in low-profile and fine-pitch surface-mount packages. Implementation of many of today's high-performance devices in these packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are illustrated in this discussion:

- Improving the power-dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in the system

Figure 16 is an example of a thermally enhanced PWB layout for the 20-lead TSSOP package. This layout involves adding copper on the PWB to conduct heat away from the device. The $R_{\theta JA}$ for this component/board system is illustrated in Figure 17. The family of curves illustrates the effect of increasing the size of the copper-heat-sink surface area. The PWB is a standard FR4 board (L × W × H = 3.2 inch × 3.2 inch × 0.062 inch); the board traces and heat sink area are 1-oz (per square foot) copper.

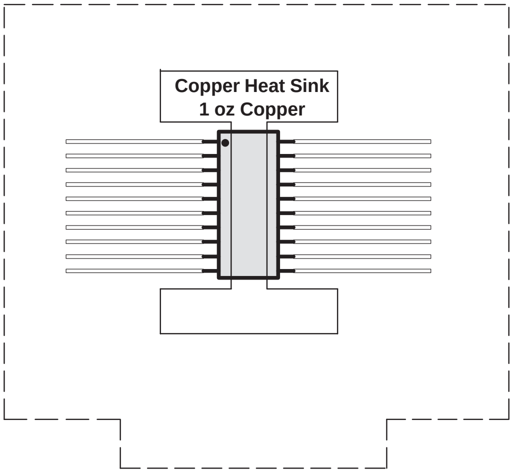


Figure 16. Thermally Enhanced PWB Layout (Not to Scale) for the 20-Pin TSSOP

Figure 18 shows the thermal resistance for the same system with the addition of a thermally conductive compound between the body of the TSSOP package and the PWB copper routed directly beneath the device. The thermal conductivity for the compound used in this analysis is 0.815 W/m × °C.

THERMAL INFORMATION

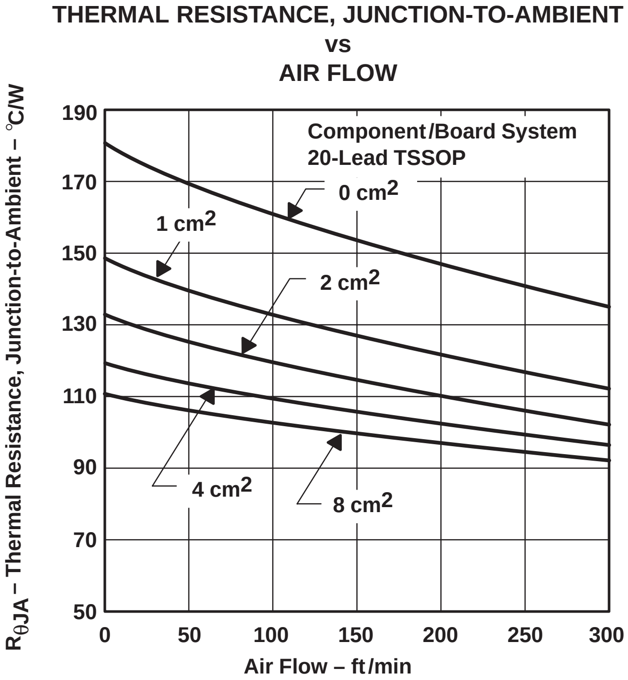


Figure 17

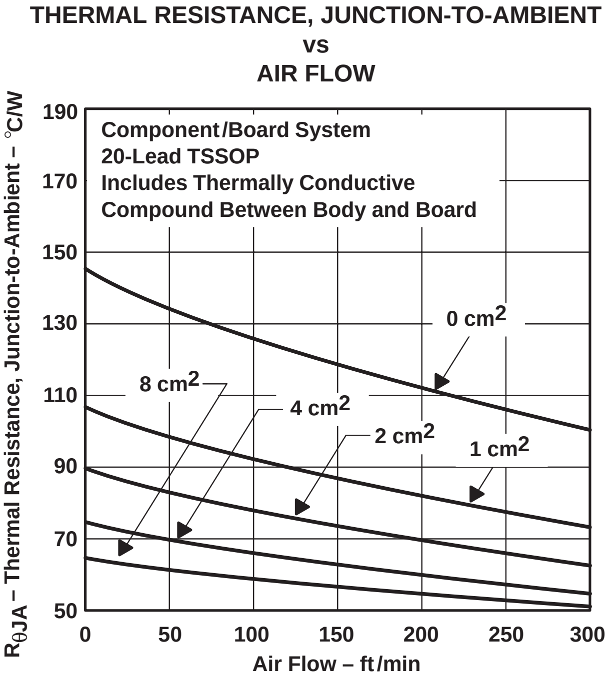


Figure 18

Using these figures to determine the system $R_{\theta JA}$ allows the maximum power-dissipation $P_{D(max)}$ limit to be calculated with the equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}}$$

Where

$T_{J(max)}$ is the maximum allowable junction temperature (i.e., 150°C absolute maximum or 125°C maximum recommended operating temperature for specified operation).

This limit should then be applied to the internal power dissipated by the TPS71025 regulator. The equation for calculating total internal power dissipation of the device is:

$$P_{D(total)} = \left(V_I - V_O\right) \times I_O + \left(V_I \times I_Q\right)$$

Because the quiescent current is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = \left(V_I - V_O\right) \times I_O$$

THERMAL INFORMATION

For a 20-lead TSSOP/FR4 board system with thermally conductive compound between the board and the device body, where T_A = 55°C, airflow = 100 ft/min, and copper heat sink area = 1 cm^2, the maximum power-dissipation limit can be calculated. As indicated in Figure 18, the system $R_{\theta JA}$ is 94°C/W; therefore, the maximum power-dissipation limit is:

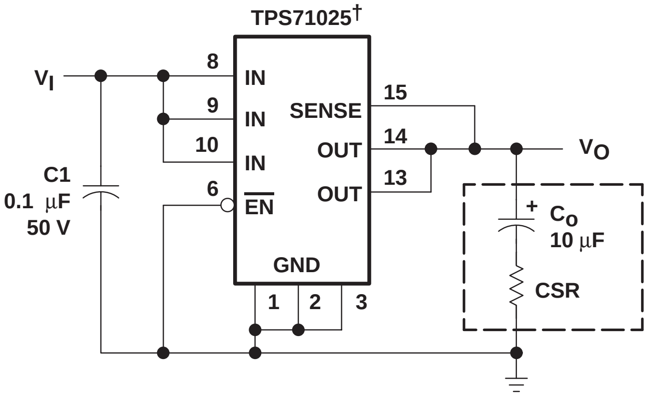
$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}} = \frac{125^\circ C - 55^\circ C}{94^\circ C/W} = 745\ mW$$

If the system implements a TPS71025 regulator where V_I = 3.3 V and I_O = 385 mA, the internal power dissipation is:

$$P_{D(total)} = \left(V_I - V_O\right) \times I_O = (3.3 - 2.5) \times 0.385 = 308\ mW$$

Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the maximum limit. When it does, one of two corrective actions can be taken. The power-dissipation limit can be raised by increasing the airflow or the heat-sink area. Alternatively, the internal power dissipation of the regulator can be lowered by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

APPLICATION INFORMATION



† Capacitor selection is nontrivial. See external capacitor requirements section.

Figure 19. Typical Application Circuit

The TPS71025 low-dropout (LDO) regulator overcomes many of the shortcomings of earlier-generation LDOs, while adding features such as a power-saving shutdown mode.

device operation

The TPS71025, unlike many other LDOs, features very low quiescent current that remains virtually constant even with varying loads. Conventional LDO regulators use a pnp-pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Examination of the data sheets reveals that those devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves. The TPS71025 uses a PMOS transistor to pass current; because the gate of the PMOS element is voltage driven, operating currents are low and stable over the full load range. The TPS71025 specifications reflect actual performance under load.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS71025 quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS71025 also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under 2 µA. If the shutdown feature is not used, $\overline{\text{EN}}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 120 µs.

minimum load requirements

The TPS71025 family is stable even at zero load; no minimum load is required for operation.

SENSE-pin connection

The SENSE pin must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network, and noise pickup feeds through to the regulator output. Routing the SENSE connection to minimize/avoid noise pickup is essential. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

APPLICATION INFORMATION

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 µF) improves load transient response and noise rejection if the TPS71025 is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

As with most LDO regulators, the TPS71025 requires an output capacitor for stability. A low-ESR 10-µF solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 11). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106K035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 mΩ (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to –40°C). Where component height and/or mounting area is a problem, physically smaller, 10-µF devices can be screened for ESR. Figure 7 through Figure 14 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2 µF), the output capacitance can be reduced to 4.7 µF, provided ESR is maintained between 0.7 and 2.5 Ω. Because minimum capacitor ESR is seldom if ever specified, it may be necessary to add a 0.5-Ω to 1-Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As shown in the ESR graphs (Figure 7 through Figure 14), minimum ESR is not a problem when using 10-µF or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS71025. This information (along with the ESR graphs, Figure 7 through Figure 14) is included to assist in selection of suitable capacitance for the application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

APPLICATION INFORMATION

external capacitor requirements (continued)

All load and temperature conditions with up to 1 μF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR[†]	SIZE (H × L × W)[†]
T421C226M010AS	Kemet	22 μF, 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 μF, 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 μF, 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 μF, 35 V	0.3	2.8 × 7.3 × 4.3

Load < 200 mA, ceramic load capacitance < 0.2 μF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR[†]	SIZE (H × L × W)[†]
592D156X0020R2T	Sprague	15 μF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 μF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 μF, 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 μF, 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 μF, full temperature range:

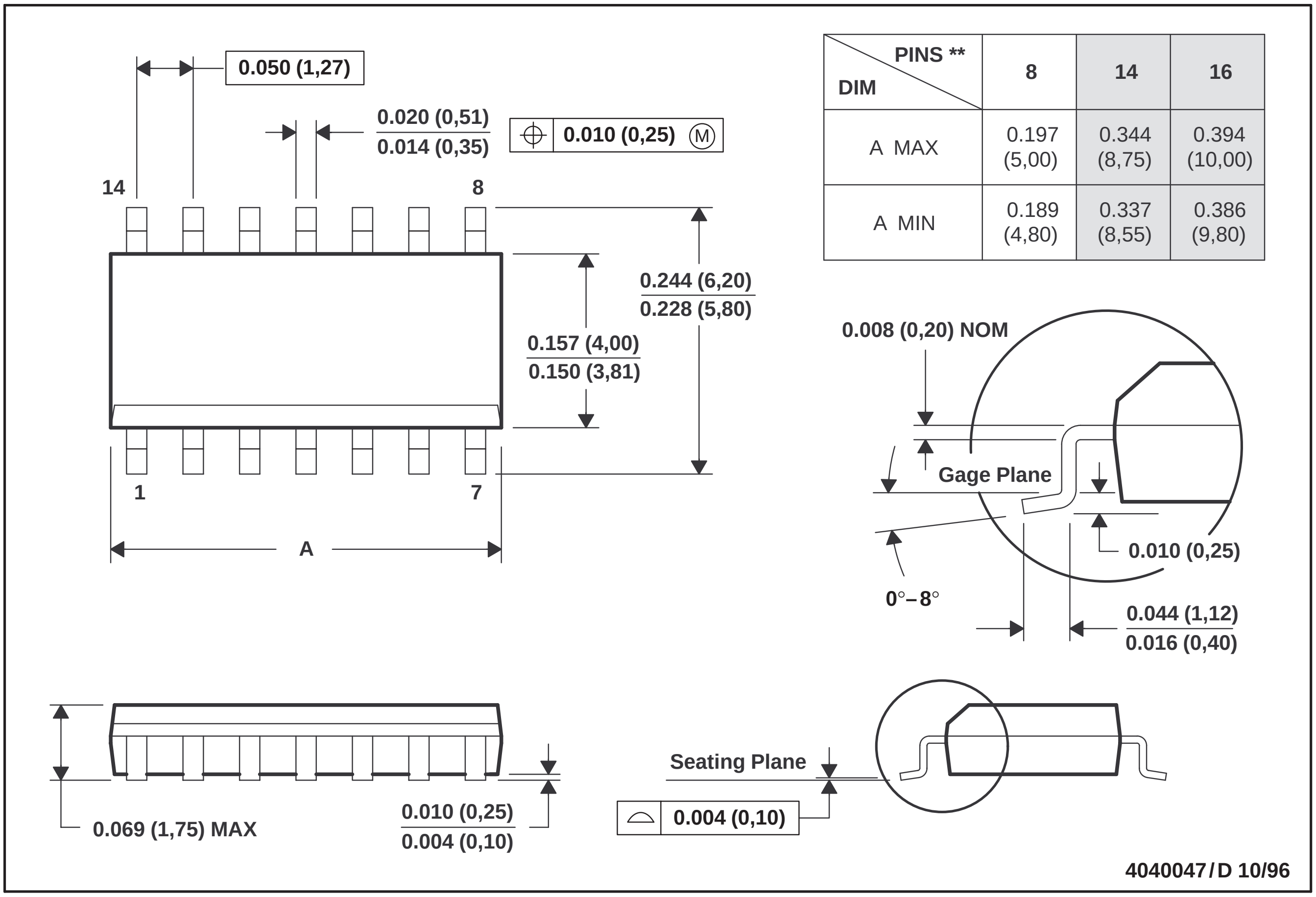
PART NO.	MFR.	VALUE	MAX ESR[†]	SIZE (H × L × W)[†]
195D106X06R3V2T	Sprague	10 μF, 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 μF, 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 μF, 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 μF, 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 μF, 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 μF, 35 V	1.3	2.5 × 7.6 × 2.5

[†] Size is in mm. ESR is maximum resistance at 100 kHz and T_A = 25°C. Listings are sorted by height.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

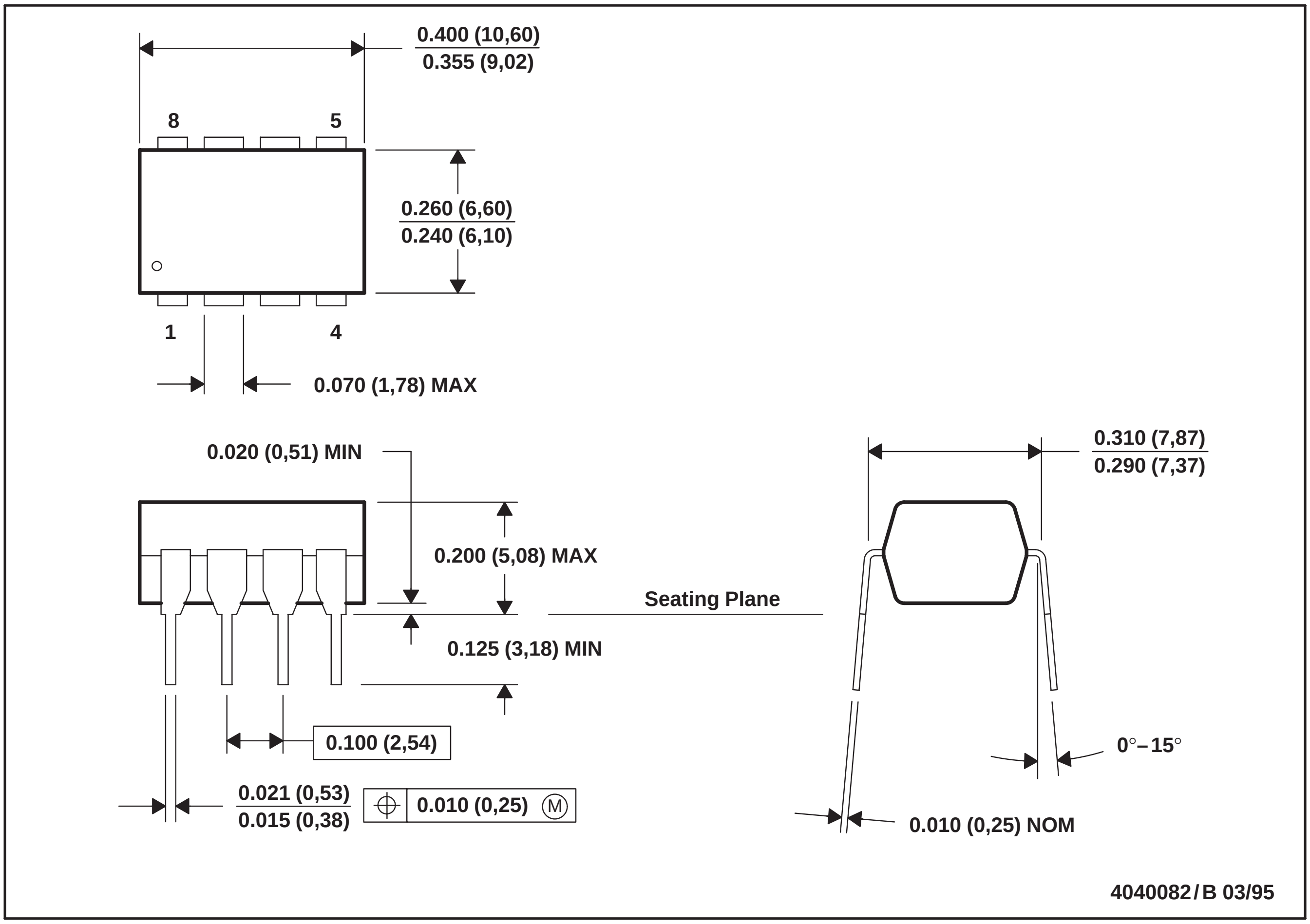


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012

MECHANICAL DATA

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**

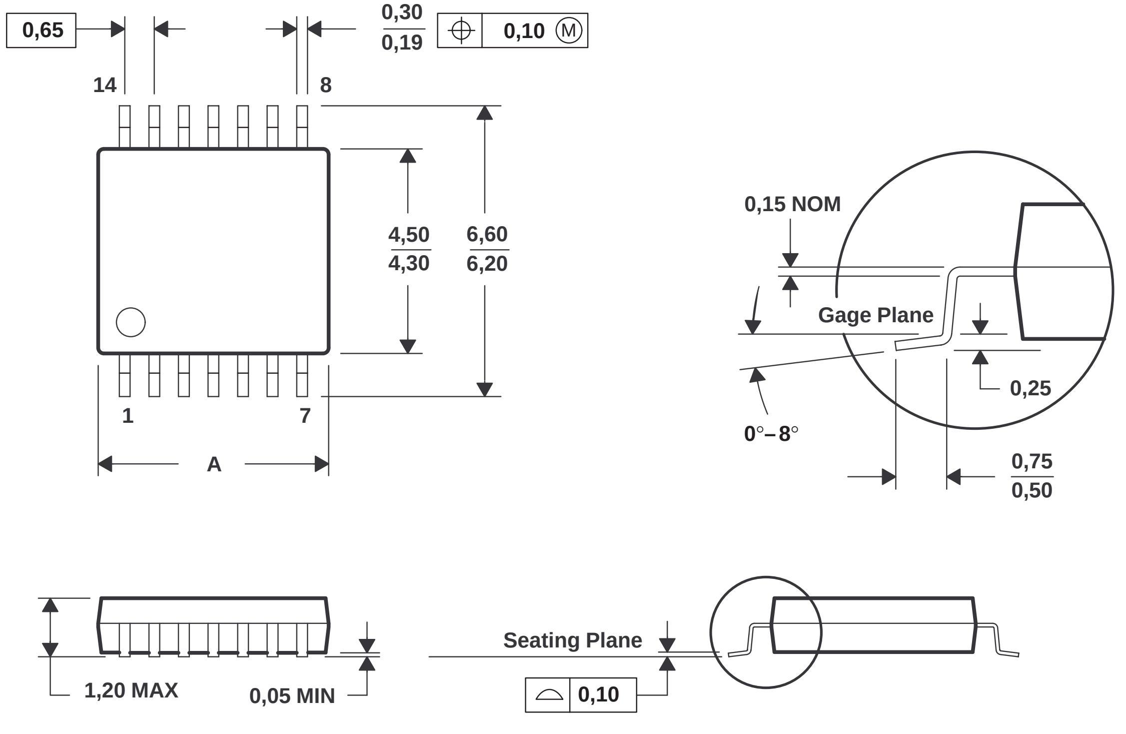


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064 / E 08/96

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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