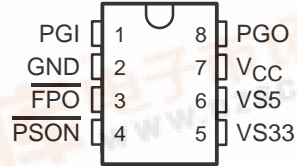


- **Over Voltage Protection and Lock Out for 5 V, 3.3 V, and 12 V**
- **Under Voltage Protection and Lock Out for 5 V and 3.3 V**
- **Fault Protection Output with Open Drain Output Stage**
- **Open Drain Power Good Output Signal for Power Good Input, 5 V and 3.3 V**
- **300 ms Power Good Delay**
- **75 ms Delay for 5-V and 3.3-V Short-Circuit Turn On Protection**
- **38 ms \overline{PSON} Control Debounce**
- **73 μ s Width Noise Deglitches**
- **Wide Power Supply Voltage Range from 4 V to 15 V**

D OR P PACKAGE
(TOP VIEW)



description

The TPS5510 is designed to minimize external components of personal computer switching power supply systems. It provides protection circuits, power good indicator, fault protection output (\overline{FPO}), and a \overline{PSON} control.

OVP (Over Voltage Protection) monitors 5 V, 3.3 V, and 12 V (12 V OV detects via V_{CC} terminal). UVP (Under Voltage Protection) monitors 5 V and 3.3 V. When an OV or UV condition is detected, the PGO (power good output) is asserted low and \overline{FPO} is latched high. \overline{PSON} from low to high resets the protection latch. UVP function will be enabled 75 ms after \overline{PSON} is set low and debounced.

Power good feature monitors PGI, 5 V and 3.3 V and issues a power good signal when they are ready.

The TPS5510 is characterised for operation from $T_J = -40^\circ\text{C}$ to 125°C junction temperature.

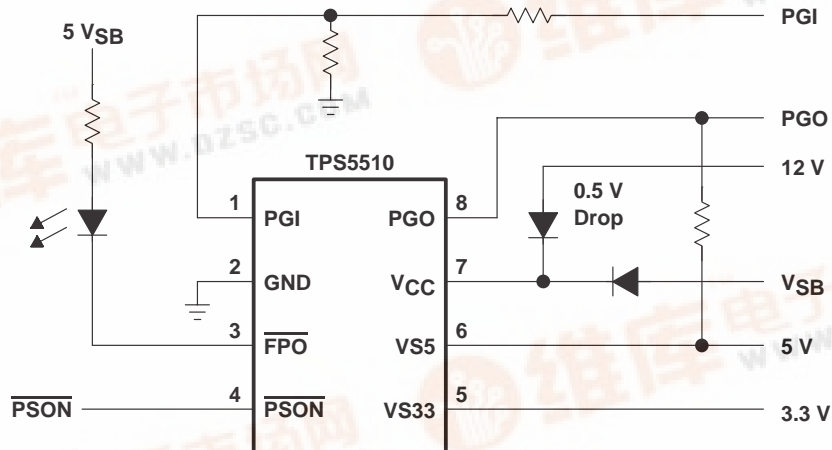
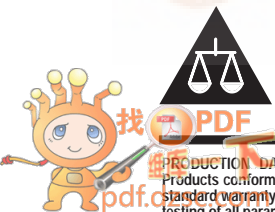


Figure 1. TPS5510 Typical Application

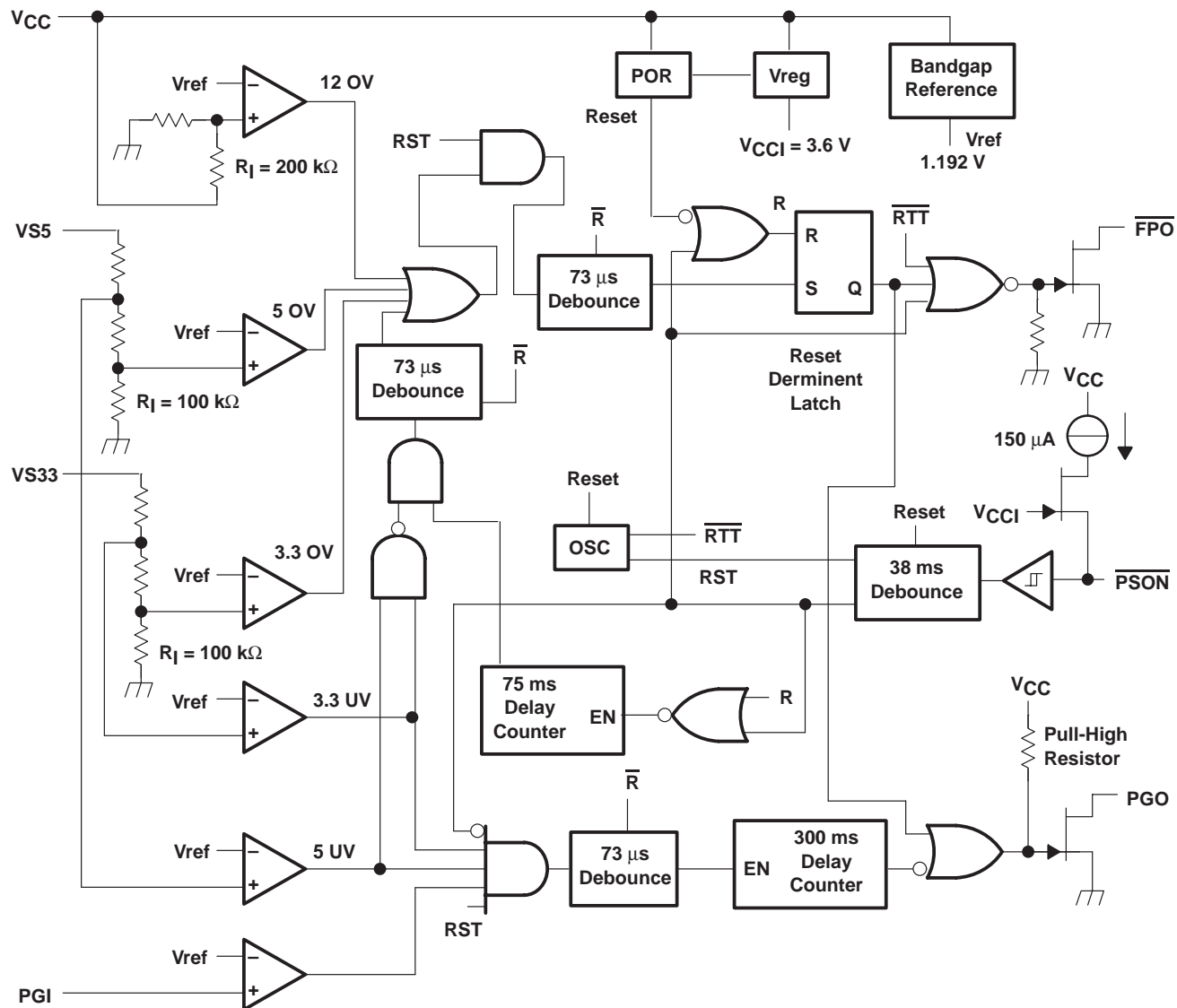
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



TPS5510 3-CHANNEL POWER SUPPLY SUPERVISOR

SLVS168 – JULY 1998

functional block diagram



TPS5510 3-CHANNEL POWER SUPPLY SUPERVISOR

SLVS168 – JULY 1998

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
VS33	5	I	3.3 V over/under voltage protection input pin
VS5	6	I	5 V over/under voltage protection input pin
GND	2		Ground
$\overline{\text{FPO}}$	3	O	Inverted fault protection output, open drain output stage
PGI	1	I	Power good input signal pin
PGO	8	O	Power good output signal pin, open drain output stage
$\overline{\text{PSON}}$	4	I	ON/OFF control input pin
V _{CC}	7	I	Supply voltage/12 V over voltage protection input pin

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	OPERATING FACTOR ABOVE T _A = 25°C	T _A = 125°C POWER RATING
P	1092 mW	8.74 mW/°C	218 mW
D	730 mW	5.84 mW/°C	146 mW

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V _{CC} , (see Note1)	16 V
Output voltage, V _O (FPO)	16 V
Output voltage, V _O (PGO)	8 V
Supply current, I _{CC}	1 mA
Continuous total power dissipation	see Dissipation Rating Table
Operating junction temperature range, T _J	–40°C to 125°C
Storage temperature range, T _{stg}	–65°C to 150°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the device GND terminal.

recommended operating conditions

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage, V _{CC}		4		15	V
Input voltage, V _I	$\overline{\text{PSON}}$, VS5, VS33, PGI			7	V
Output voltage, V _O	FPO			15	V
	PGO			7	V
Operating junction temperature, T _J		–40		125	°C
Output sink current, I _{O(sink)}	FPO			30	mA
	PGO			10	mA
Supply voltage rising time, t _r	See Note 2	1			ms

NOTE 2: V_{CC} rising and falling slew rate must be less than 14 V/ms.

TPS5510

3-CHANNEL POWER SUPPLY SUPERVISOR

SLVS168 – JULY 1998

electrical characteristics, $V_{CC} = 5\text{ V}$, $T_J = \text{full range}$. (unless otherwise specified)

over voltage protection

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Over-voltage threshold	VS33		3.9	4.1	4.3	V
	VS5		5.7	6.1	6.5	
	V_{CC}		13.3	13.8	14.3	
I_{LKG}	Leakage current (\overline{FPO})	$V(\overline{FPO}) = 5\text{ V}$			5	μA
V_{OL}	Low level output voltage (\overline{FPO})	$I_{\text{sink}} = 10\text{ mA}$			0.3	V
		$I_{\text{sink}} = 30\text{ mA}$			0.7	

PGI and PGO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input threshold voltage (PGI)		1.141	1.192	1.242	V
Under-voltage threshold		VS33	2.71	2.83	2.95	V
		VS5	4.1	4.3	4.47	
	Short circuit protection delay time	3.3 V, 5 V	49	75	114	ms
I_{LKG}	Leakage current (PGO)	$PGO = 5\text{ V}$			5	μA
V_{OL}	Low level output voltage (PGO)	Sink current = 10 mA			0.4	V

\overline{PSON} control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input pull-up current	$\overline{PSON} = 0\text{ V}$		150		μA
	High-level input voltage		2.4			V
	Low-level input voltage				1.2	V

total device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	$\overline{PSON} = 5\text{ V}$			1	mA

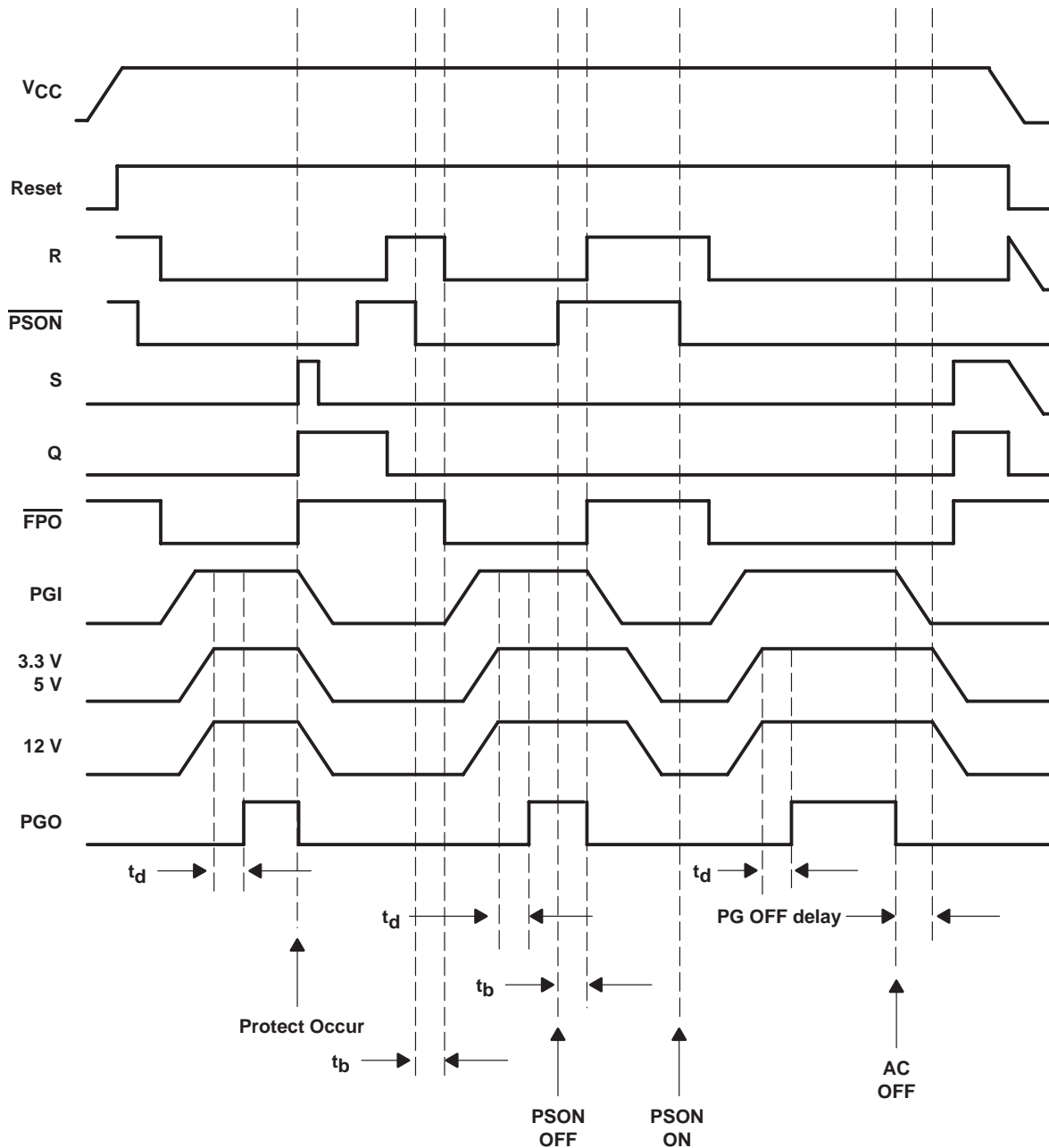
switching characteristics, $V_{CC} = 5\text{ V}$, $T_J = \text{full range}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time (PGI to PGO)		200	300	450	ms
t_b	De-bounce time (\overline{PSON})		24	38	57	ms
	Noise deglitch time		47	73	110	μs

TPS5510 3-CHANNEL POWER SUPPLY SUPERVISOR

SLVS168 – JULY 1998

timing chart



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.