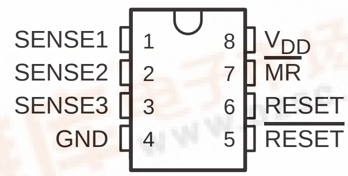
TPS3307-18, TPS3307-25, TPS3307-33
TRIPLE PROCESSOR SUPERVISORS

SLVS199 – DECEMBER 1998

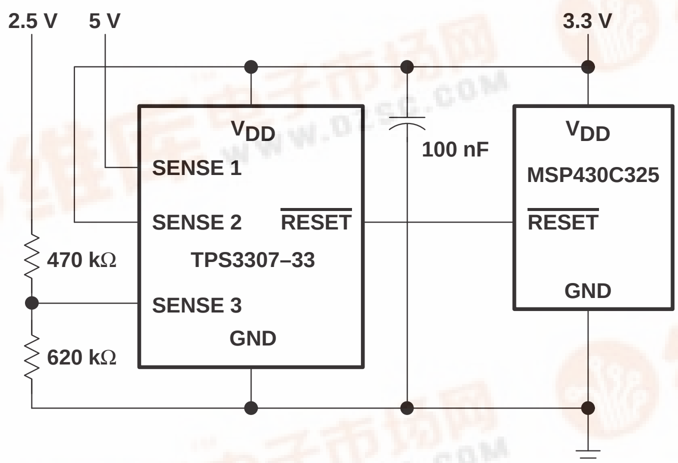
- Triple Supervisory Circuits for DSP and Processor-Based Systems
- Power-On Reset Generator with Fixed Delay Time of 200 ms, No External Capacitor Needed
- Temperature-Compensated Voltage Reference
- Maximum Supply Current of 40 µA
- Supply Voltage Range . . . 2 V to 6 V
- Defined RESET Output from $V_{DD} \geq 1.1$ V
- MSOP-8 and SO-8 Packages
- Temperature Range . . . – 40°C to 85°C

D OR DGN PACKAGE
(TOP VIEW)



typical applications

Figure 1 lists some of the typical applications for the TPS3307 family, and a schematic diagram for a processor-based system application. This application uses TI part numbers TPS3307–33 and MSP430C325.



- Applications using DSPs, Microcontrollers or Microprocessors
- Industrial Equipment
- Programmable Controls
- Automotive Systems
- Portable/Battery Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Notebook/Desktop Computers

Figure 1. Applications Using the TPS3307 Family

description

The TPS3307 family is a series of micropower supply voltage supervisors designed for circuit initialization primarily in DSP and processor-based systems, which require more than one supply voltage.

The product spectrum of the TPS3307-xx is designed for monitoring three independent supply voltages: 3.3 V/1.8 V/adj, 3.3 V/2.5 V/adj or 3.3 V/5 V/adj. The adjustable SENSE input allows the monitoring of any supply voltage >1.25 V.

The various supply voltage supervisors are designed to monitor the nominal supply voltage as shown in the following supply voltage monitoring table.

description (continued)

SUPPLY VOLTAGE MONITORING

DEVICE	NOMINAL SUPERVISED VOLTAGE			THRESHOLD VOLTAGE (TYP)		
	SENSE1	SENSE2	SENSE3	SENSE1	SENSE2	SENSE3
TPS3307-18	3.3 V	1.8 V	User defined	2.93 V	1.68 V	1.25 V†
TPS3307-25	3.3 V	2.5 V	User defined	2.93 V	2.25 V	1.25 V†
TPS3307-33	5 V	3.3 V	User defined	4.55 V	2.93 V	1.25 V†

† The actual sense voltage has to be adjusted by an external resistor divider according to the application requirements.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors the SENSEn inputs and keeps $\overline{\text{RESET}}$ active as long as SENSEn remain below the threshold voltage V_{IT+}.

An internal timer delays the return of the $\overline{\text{RESET}}$ output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d\,typ}$ = 200 ms, starts after all SENSEn inputs have risen above the threshold voltage V_{IT+}. When the voltage at any SENSE input drops below the threshold voltage V_{IT-}, the $\overline{\text{RESET}}$ output becomes active (low) again.

The TPS3307-xx family of devices incorporates a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active. In addition to the active-low $\overline{\text{RESET}}$ output, the TPS3307-xx family includes an active-high RESET output.

The devices are available in either 8-pin MSOP or standard 8-pin SO packages.

The TPS3307-xx devices are characterized for operation over a temperature range of – 40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MARKING DGN PACKAGE	CHIP FORM (Y)
	SMALL OUTLINE (D)	PowerPAD™ μ-SMALL OUTLINE (DGN)		
–40°C to 85°C	TPS3307-18D	TPS3307-18DGN	TIAAP	TPS3307-18Y
	TPS3307-25D	TPS3307-25DGN	TIAAQ	TPS3307-25Y
	TPS3307-33D	TPS3307-33DGN	TIAAR	TPS3307-33Y

FUNCTION/TRUTH TABLES

$\overline{\text{MR}}$	SENSE1>V_{IT1}	SENSE2>V_{IT2}	SENSE3>V_{IT3}	$\overline{\text{RESET}}$	RESET
L	X†	X†	X	L	H
H	0	0	0	L	H
H	0	0	1	L	H
H	0	1	0	L	H
H	0	1	1	L	H
H	1	0	0	L	H
H	1	0	1	L	H
H	1	1	0	L	H
H	1	1	1	H	L

† X = Don't care

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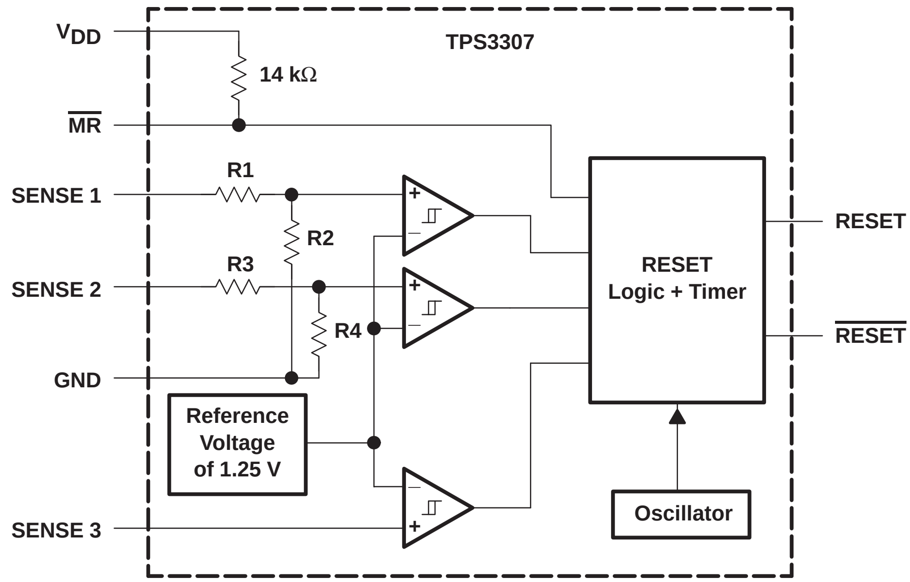
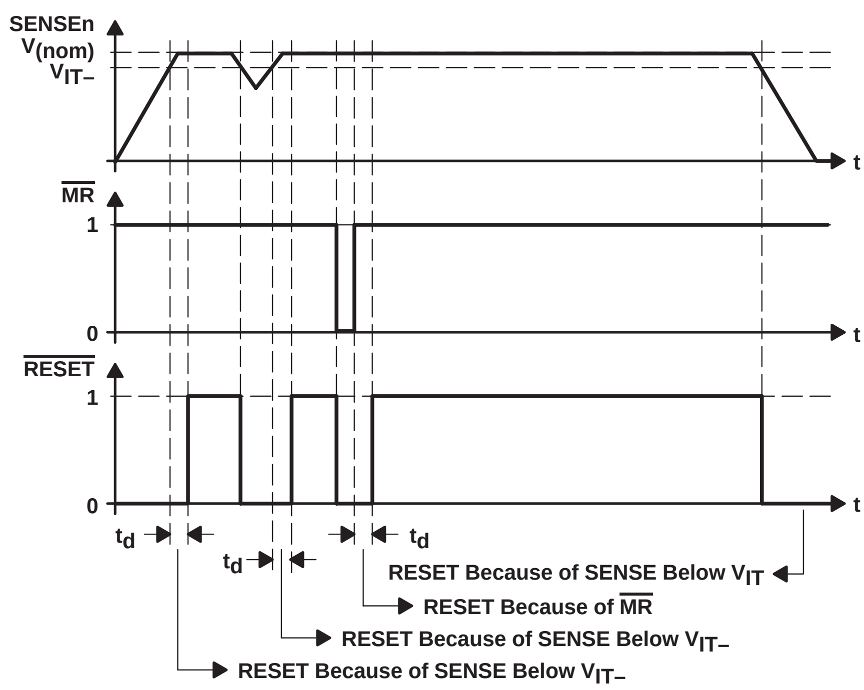
functional block diagram

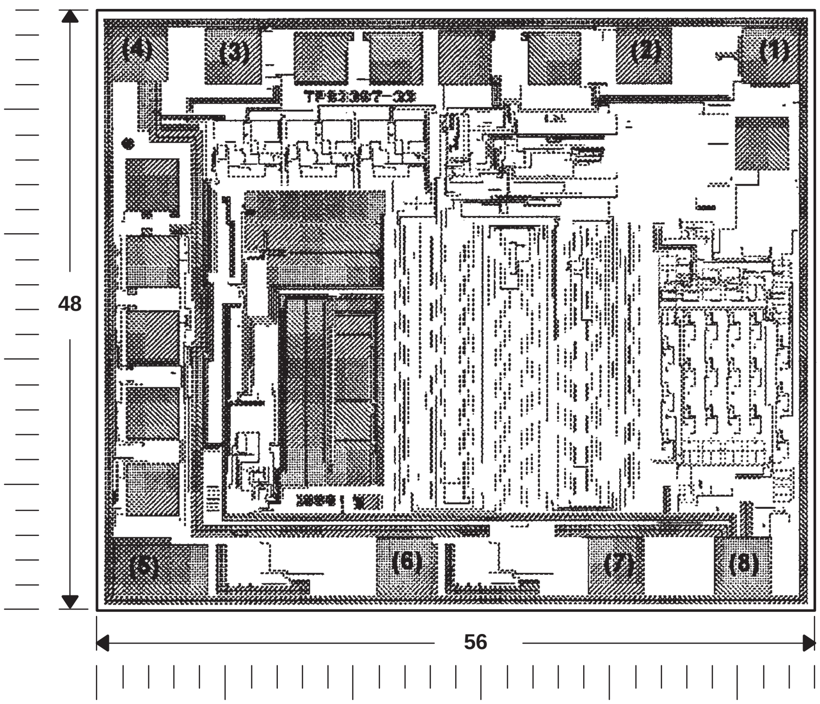


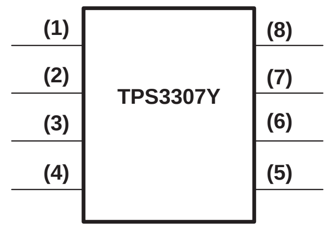
timing diagram



TPS3307Y chip information

These chips, when properly assembled, display characteristics similar to those of the TPS3307. Thermal compression or ultrasonic bonding may take place on the doped aluminium bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.





CHIP THICKNESS: 10 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	4		Ground
$\overline{\text{MR}}$	7	I	Manual reset
$\overline{\text{RESET}}$	5	O	Active-low reset output
RESET	6	O	Active-high reset output
SENSE1	1	I	Sense voltage input 1
SENSE2	2	I	Sense voltage input 2
SENSE3	3	I	Sense voltage input 3
V_{DD}	8		Supply voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note1) . . . . 7 V
All other pins (see Note 1) . . . . –0.3 V to 7 V
Maximum low output current, I_{OL} . . . . 5 mA
Maximum high output current, I_{OH} . . . . –5 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) . . . . ±20 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Soldering temperature . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t = 1000 h continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGN	2.14 mW	17.1 mW/°C	1.37 mW	1.11 mW
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2	6	V
Input voltage at $\overline{MR}$ and SENSE3, V_I	0	V_{DD}+0.3	V
Input voltage at SENSE1 and SENSE2, V_I	0	(V_{DD}+0.3)V_{IT}/1.25V	V
High-level input voltage at $\overline{MR}$, V_{IH}	0.7xV_{DD}		V
Low-level input voltage at $\overline{MR}$, V_{IL}		0.3×V_{DD}	V
Input transition rise and fall rate at $\overline{MR}$, $\Delta t/\Delta V$		50	ns/V
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 2 V to 6 V, I_{OH} = –20 µA	V_{DD}– 0.2V			V
			V_{DD} = 3.3 V, I_{OH} = –2 mA	V_{DD}– 0.4V			
			V_{DD} = 6 V, I_{OH} = –3 mA	V_{DD}– 0.4V			
V_{OL}	Low-level output voltage		V_{DD} = 2 V to 6 V, I_{OL} = 20 µA			0.2	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA			0.4	
			V_{DD} = 6 V, I_{OL} = 3 mA			0.4	
	Power-up reset voltage (see Note 2)		$V_{DD} \geq$ 1.1 V, I_{OL} = 20 µA			0.4	V
V_{IT-}	Negative-going input threshold voltage (see Note 3)	VSENSE3	V_{DD} = 2 V to 6 V, T_A = 0°C to 85°C	1.22	1.25	1.28	V
		VSENSE1, VSENSE2		1.64	1.68	1.72	V
				2.20	2.25	2.30	
				2.86	2.93	3	
				4.46	4.55	4.64	
		VSENSE3	V_{DD} = 2 V to 6 V, T_A = –40°C to 85°C	1.22	1.25	1.29	V
		VSENSE1, VSENSE2		1.64	1.68	1.73	V
				2.20	2.25	2.32	
				2.86	2.93	3.02	
				4.46	4.55	4.67	
V_{hys}	Hysteresis at VSENSEn input		V_{IT-} = 1.25 V		10		mV
			V_{IT-} = 1.68 V		15		
			V_{IT-} = 2.25 V		20		
			V_{IT-} = 2.93 V		30		
			V_{IT-} = 4.55 V		40		
I_H	High-level input current	$\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 6 V		–130	–180	µA
		SENSE1	VSENSE1 = V_{DD} = 6 V		5	8	
		SENSE2	VSENSE2 = V_{DD} = 6 V		6	9	
		SENSE3	VSENSE3 = V_{DD}	–1		1	
I_L	Low-level input current	$\overline{MR}$	$\overline{MR}$ = 0 V, V_{DD} = 6 V		–430	–600	µA
		SENSEn	VSENSE1,2,3 = 0 V	–1		1	
I_{DD}	Supply current					40	µA
C_i	Input capacitance		V_I = 0 V to V_{DD}		10		pF

NOTES: 2. The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, $V_{DD} \geq$ 15 µs/V
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 µF) should be placed close to the supply terminals.

timing requirements at V_{DD} = 2 V to 6 V, R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	SENSEn	$V_{SENSEnL} = V_{IT-}$ –0.2 V, $V_{SENSEnH} = V_{IT+}$ +0.2 V	6			µs
		$\overline{\text{MR}}$	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$	100			ns

switching characteristics at V_{DD} = 2 V to 6 V, R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{I(SENSEn)} \geq V_{IT+}$ + 0.2 V, $\overline{\text{MR}} \geq 0.7 \times V_{DD}$, See timing diagram	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ $\overline{\text{MR}}$ to RESET	$V_{I(SENSEn)} \geq V_{IT+}$ +0.2 V, $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$		200	500	ns
t_{PLH}	Propagation (delay) time, low-to-high level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ $\overline{\text{MR}}$ to RESET					
t_{PHL}	Propagation (delay) time, high-to-low level output	SENSEn to $\overline{\text{RESET}}$ SENSEn to RESET	$V_{IH} = V_{IT+}$ +0.2 V, $V_{IL} = V_{IT-}$ –0.2 V, $\overline{\text{MR}} \geq 0.7 \times V_{DD}$		1	5	µs
t_{PLH}	Propagation (delay) time, low-to-high level output	SENSEn to $\overline{\text{RESET}}$ SENSEn to RESET					

TYPICAL CHARACTERISTICS

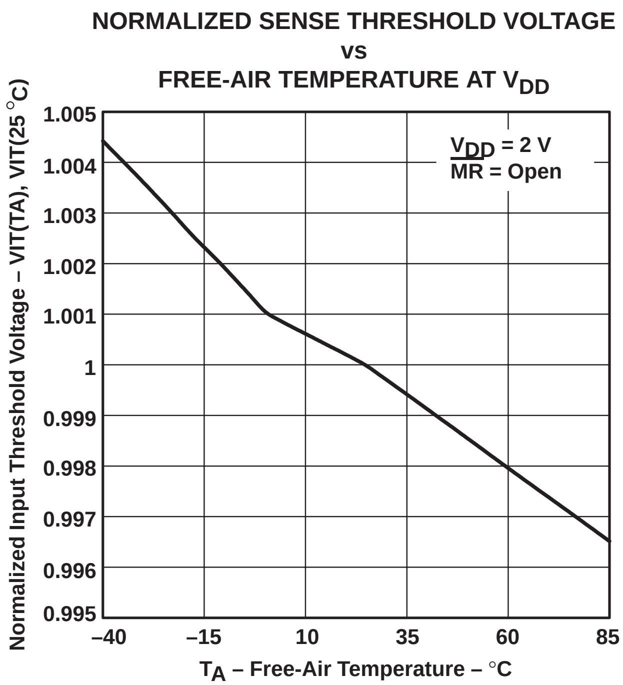


Figure 2

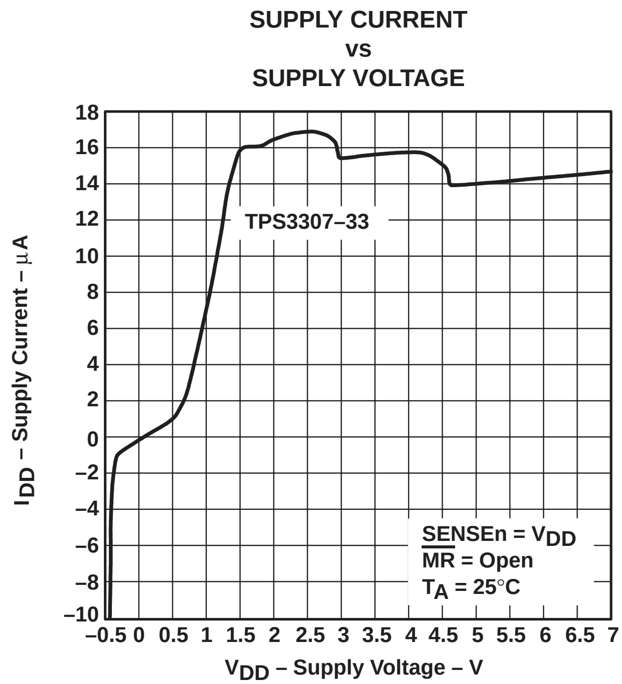


Figure 3

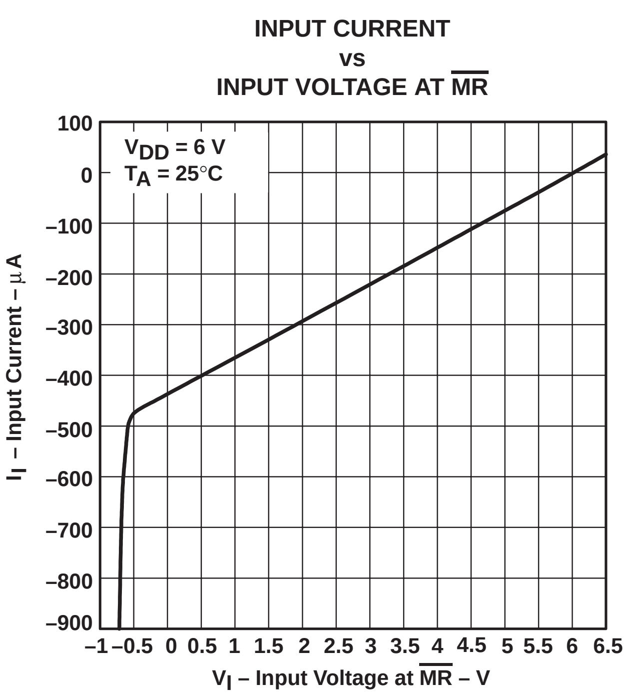


Figure 4

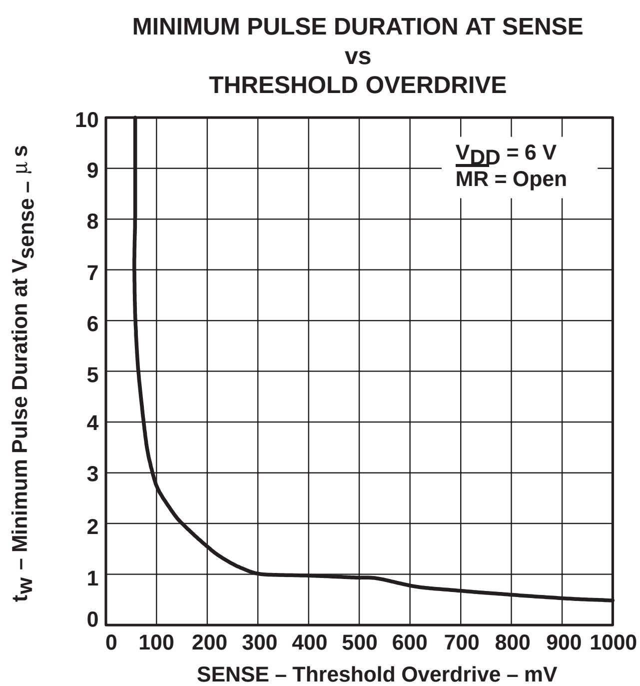


Figure 5

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

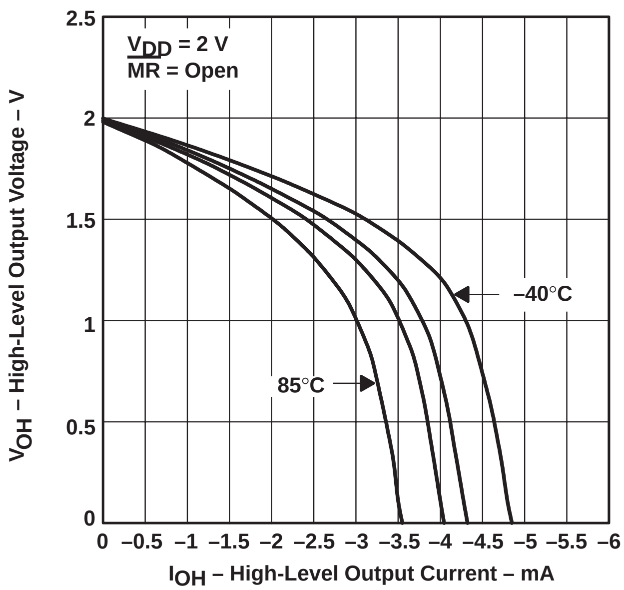


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

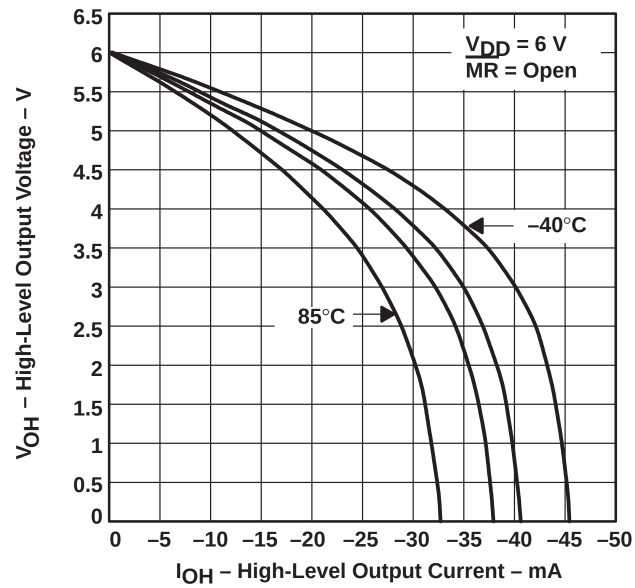


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

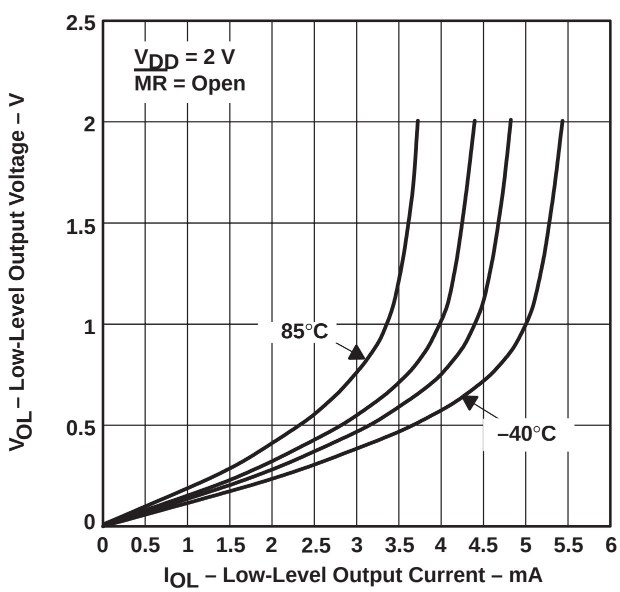


Figure 8

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

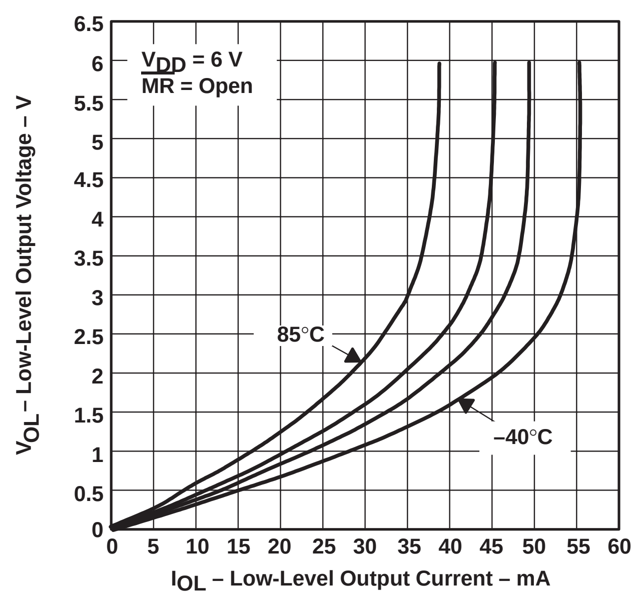
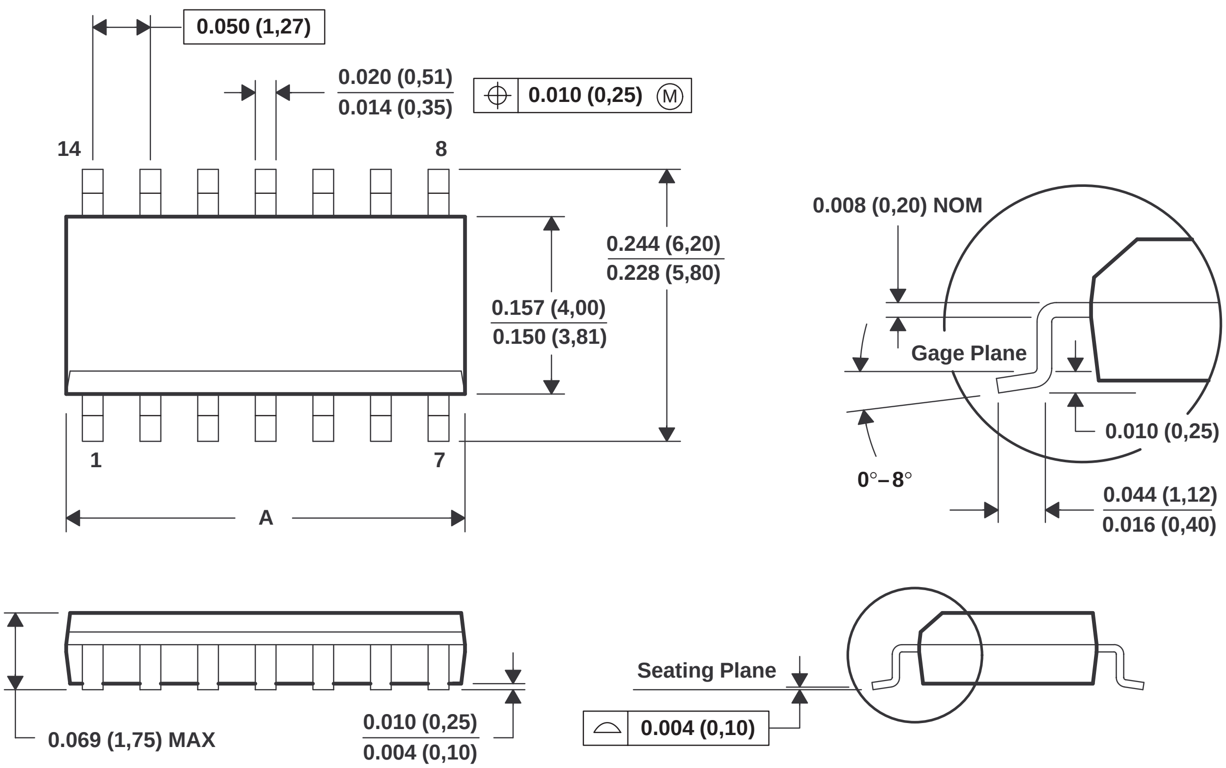


Figure 9

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



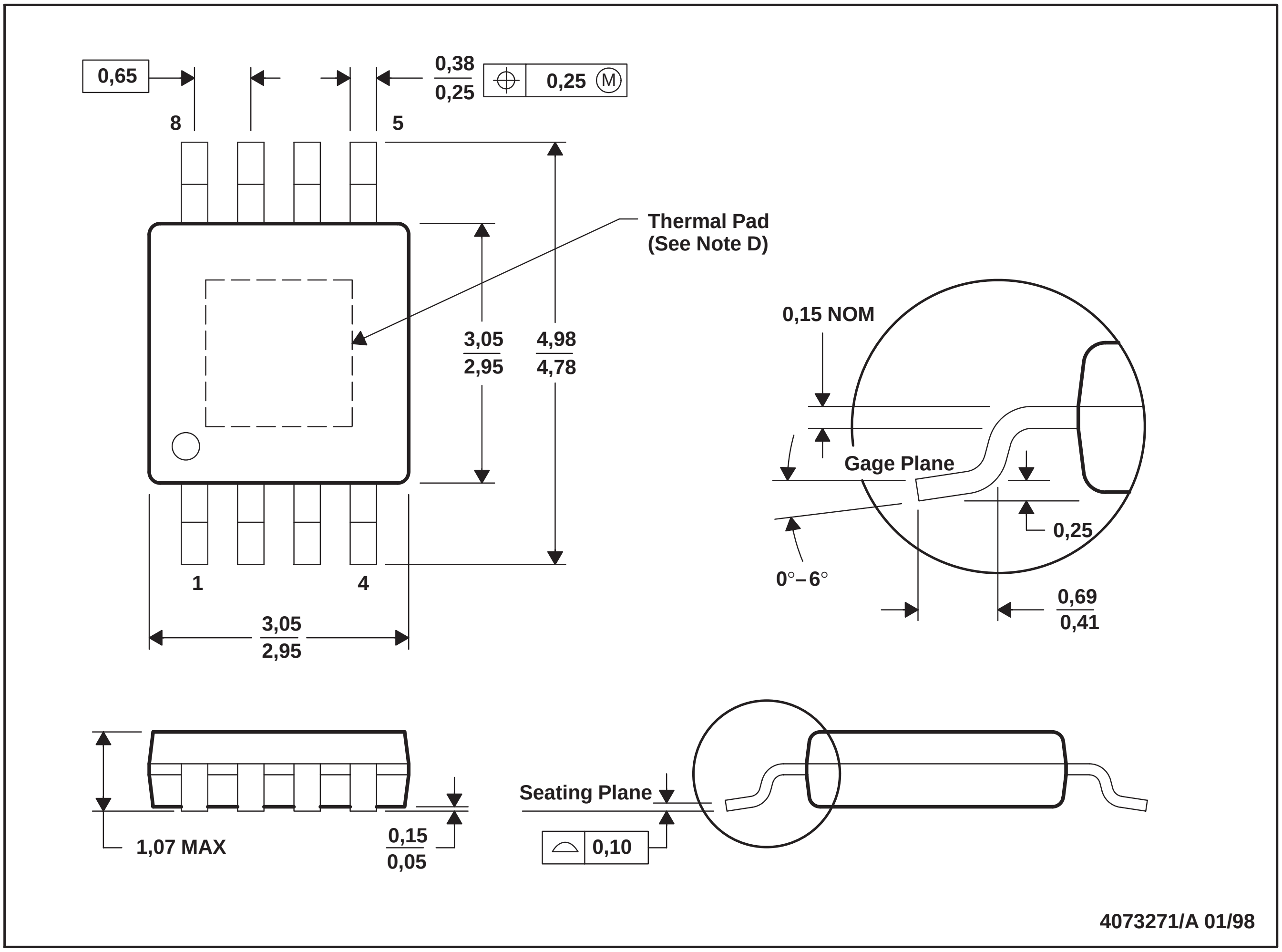
PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

DGN (S-PDSO-G8) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-187