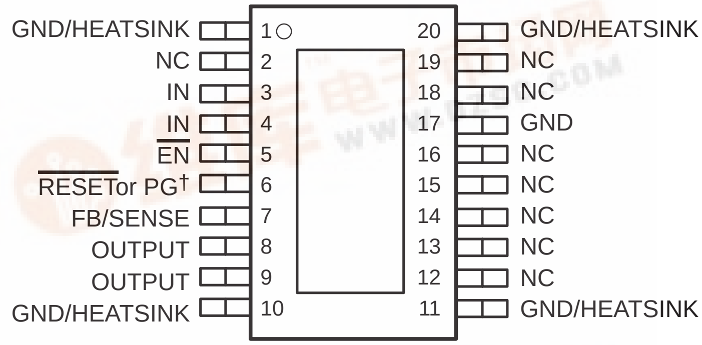
TPS75201Q, TPS75215Q, TPS75218Q, TPS75225Q, TPS75233Q WITH RESET TPS75401Q, TPS75415Q, TPS75418Q, TPS75425Q, TPS75433Q WITH POWER GOOD FAST-TRANSIENT-RESPONSE 2-A LOW-DROPOUT VOLTAGE REGULATORS

SLVS242 – MARCH 2000

- **2-A Low-Dropout Voltage Regulator**
- **Available in 1.5-V, 1.8-V, 2.5-V, 3.3-V Fixed Output and Adjustable Versions**
- **Open Drain Power-On Reset With 100-ms Delay (TPS752xxQ)**
- **Open Drain Power-Good (PG) Status Output (TPS754xxQ)**
- **Dropout Voltage Typically 210 mV at 2 A (TPS75233Q)**
- **Ultra Low 75-μA Typical Quiescent Current**
- **Fast Transient Response**
- **2% Tolerance Over Specified Conditions for Fixed-Output Versions**
- **20-Pin TSSOP (PWP) PowerPAD™ Package**
- **Thermal Shutdown Protection**

PWP PACKAGE
(TOP VIEW)

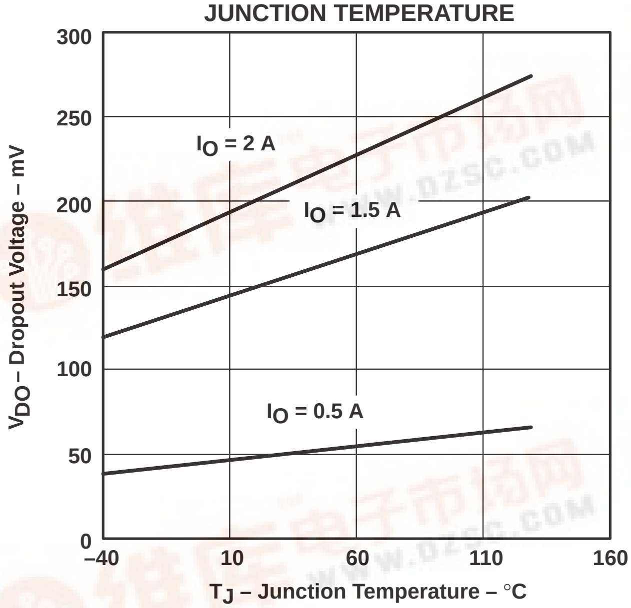


NC – No internal connection
† PG is on the TPS754xx and RESET is on the TPS752xx

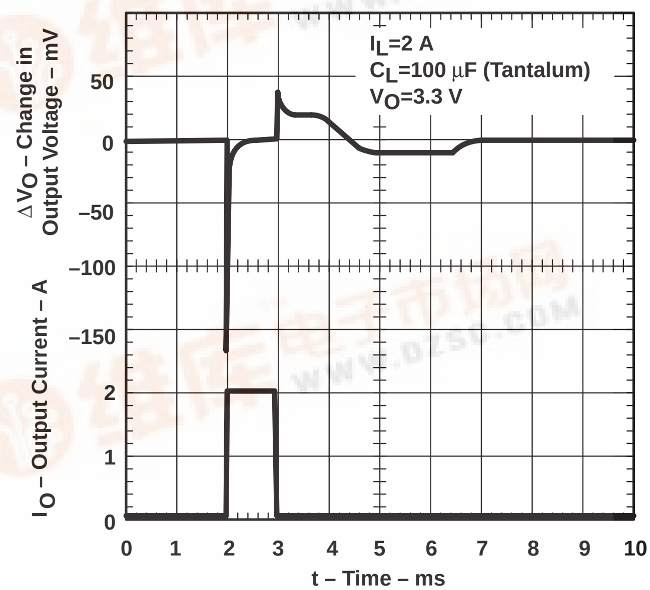
description

The TPS752xxQ and TPS754xxQ are low dropout regulators with integrated power-on reset and power good (PG) functions respectively. These devices are capable of supplying 2 A of output current with a dropout of 210 mV (TPS75233Q, TPS75433Q). Quiescent current is 75 μA at full load and drops down to 1 μA when the device is disabled. TPS752xxQ and TPS754xxQ are designed to have fast transient response for larger load current changes.

TPS75x33Q
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE



TPS75x33Q
LOAD TRANSIENT RESPONSE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

description (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 210 mV at an output current of 2 A for the TPS75x33Q) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 75 µA over the full range of output current, 1 mA to 2 A). These two key specifications yield a significant improvement in operating life for battery-powered systems.

The device is enabled when the EN pin is connected to a low-level input voltage. This LDO family also features a sleep mode; applying a TTL high signal to EN (enable) shuts down the regulator, reducing the quiescent current to 1 µA at T_J = 25°C.

The RESET (SVS, POR, or power on reset) output of the TPS752xxQ initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS752xxQ monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage. When the output reaches 95% of its regulated voltage, RESET goes to a high-impedance state after a 100-ms delay. RESET goes to a logic-low state when the regulated output voltage is pulled below 95% (i.e., over load condition) of its regulated voltage.

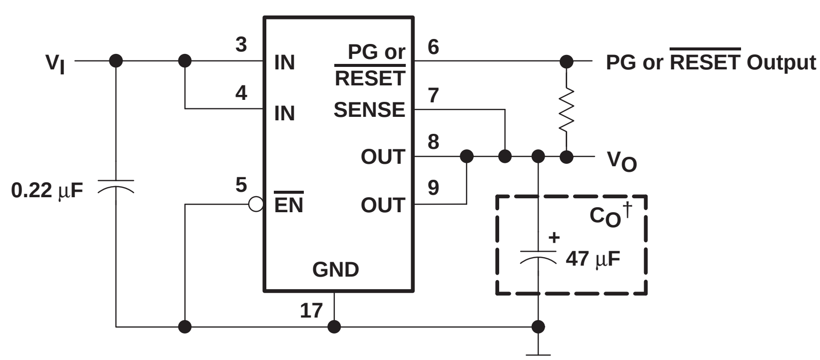
The TPS754xxQ has a power good terminal (PG) as an active high, open drain output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS752xxQ or the TPS754xxQ are offered in 1.5-V, 1.8-V, 2.5-V, and 3.3-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS752xxQ and the TPS754xxQ families are available in 20 pin TSSOP (PWP) packages.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (TYP)	TSSOP (PWP)	
		RESET	PG
–40°C to 125°C	3.3 V	TPS75233QPWP	TPS75433QPWP
	2.5 V	TPS75225QPWP	TPS75425QPWP
	1.8 V	TPS75218QPWP	TPS75418QPWP
	1.5 V	TPS75215QPWP	TPS75415QPWP
	Adjustable 1.5 V to 5 V	TPS75201QPWP	TPS75401QPWP

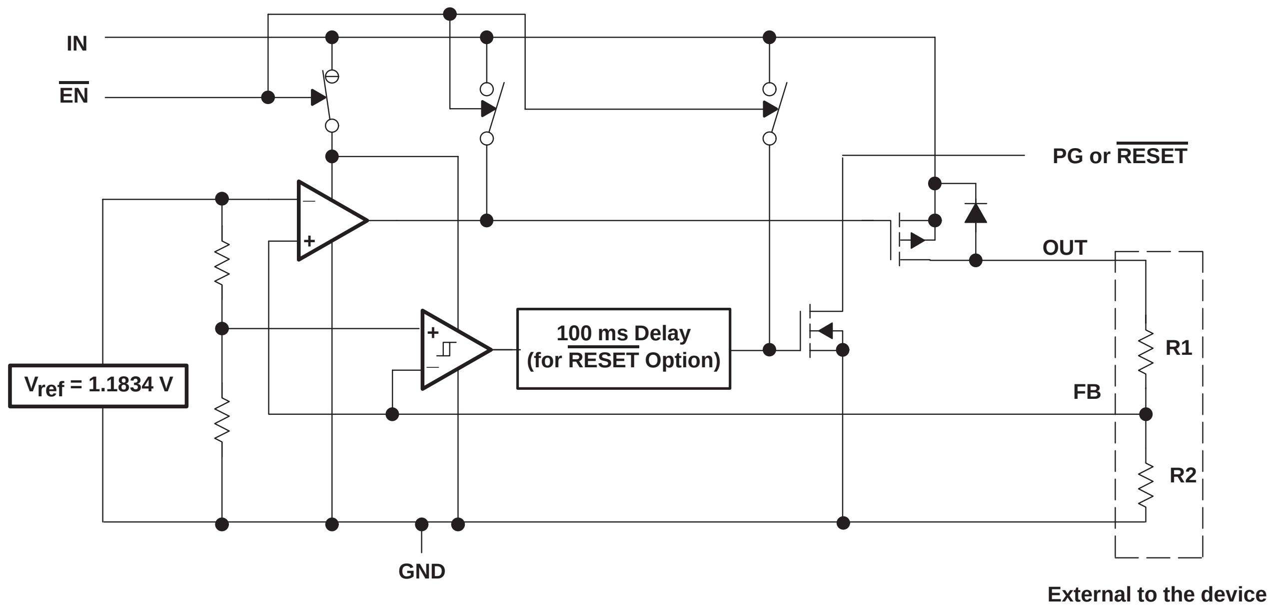
The TPS75x01 is programmable using an external resistor divider (see application information). The PWP package is available taped and reeled. Add an R suffix to the device type (e.g., TPS75201QPWPR) to indicate tape and reel.



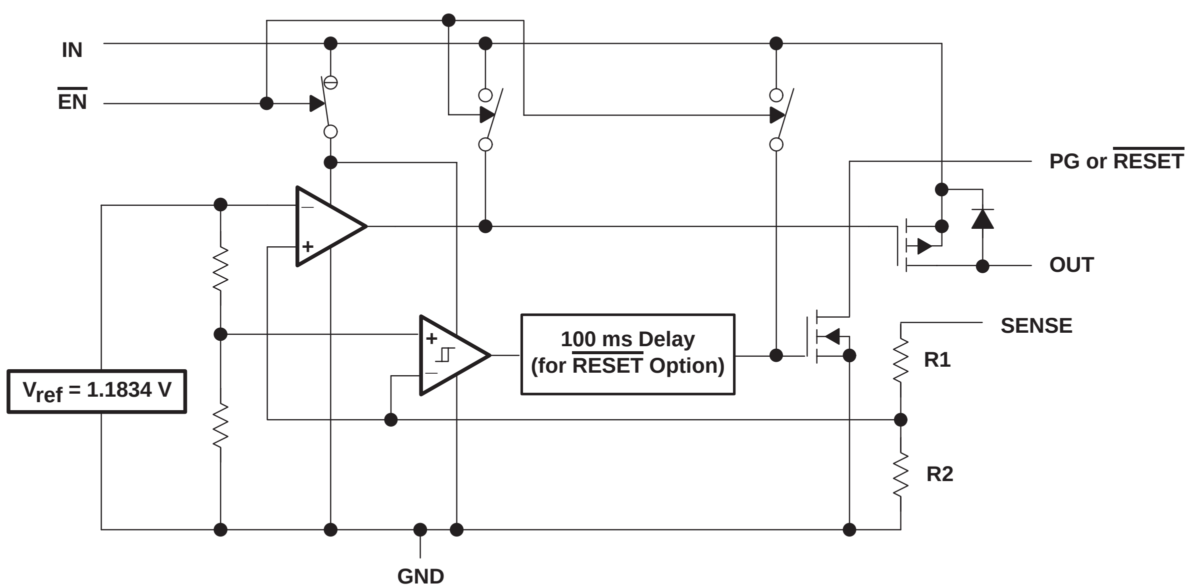
† See application information section for capacitor selection details.

Figure 1. Typical Application Configuration (For Fixed Output Options)

functional block diagram—adjustable version



functional block diagram—fixed-voltage version



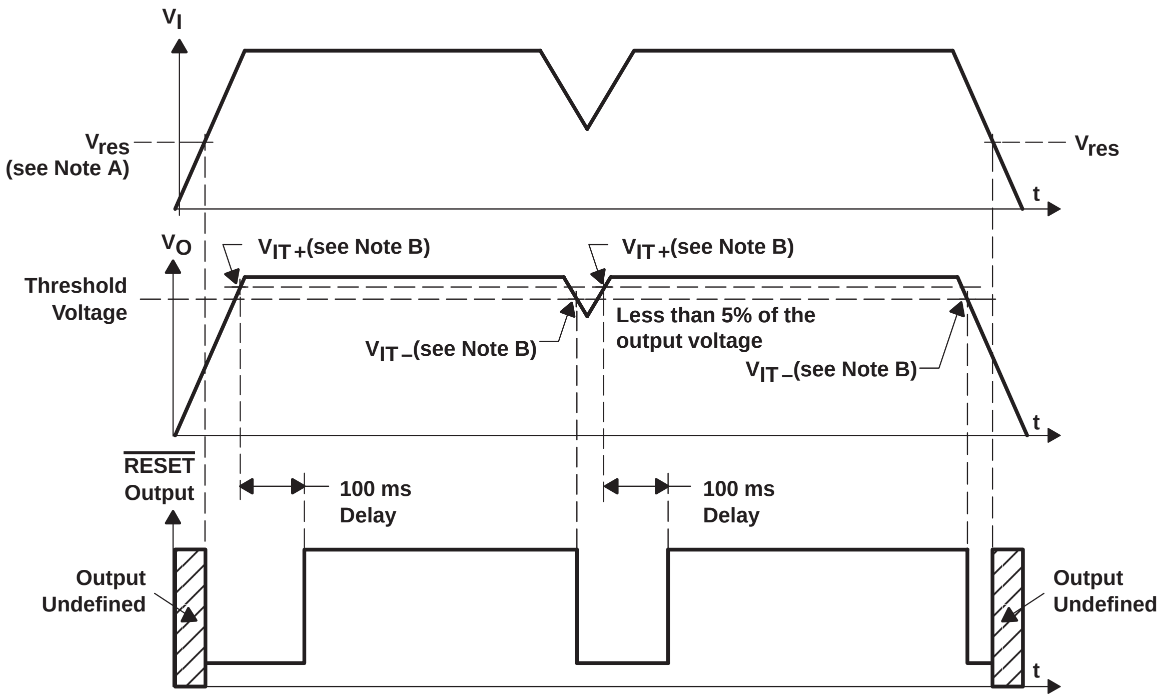
Terminal Functions (TPS752xxQ)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
EN	5	I	Enable Input
FB/SENSE	7	I	Feedback input voltage for adjustable device (sense input for fixed-voltage option)
GND	17		Regulator ground
GND/HEATSINK	1, 10, 11, 20		Ground/heatsink
IN	3, 4	I	Input voltage
NC	2, 12, 13, 14, 15, 16, 18, 19		No connection
OUTPUT	8, 9	O	Regulated output voltage
RESET	6	O	Reset output

Terminal Functions (TPS754xxQ)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
EN	5	I	Enable Input
FB/SENSE	7	I	Feedback input voltage for adjustable device (sense input for fixed-voltage option)
GND	17		Regulator ground
GND/HEATSINK	1, 10, 11, 20		Ground/heatsink
IN	3, 4	I	Input voltage
NC	2, 12, 13, 14, 15, 16, 18, 19		No connection
OUTPUT	8, 9	O	Regulated output voltage
PG	6	O	Power good output

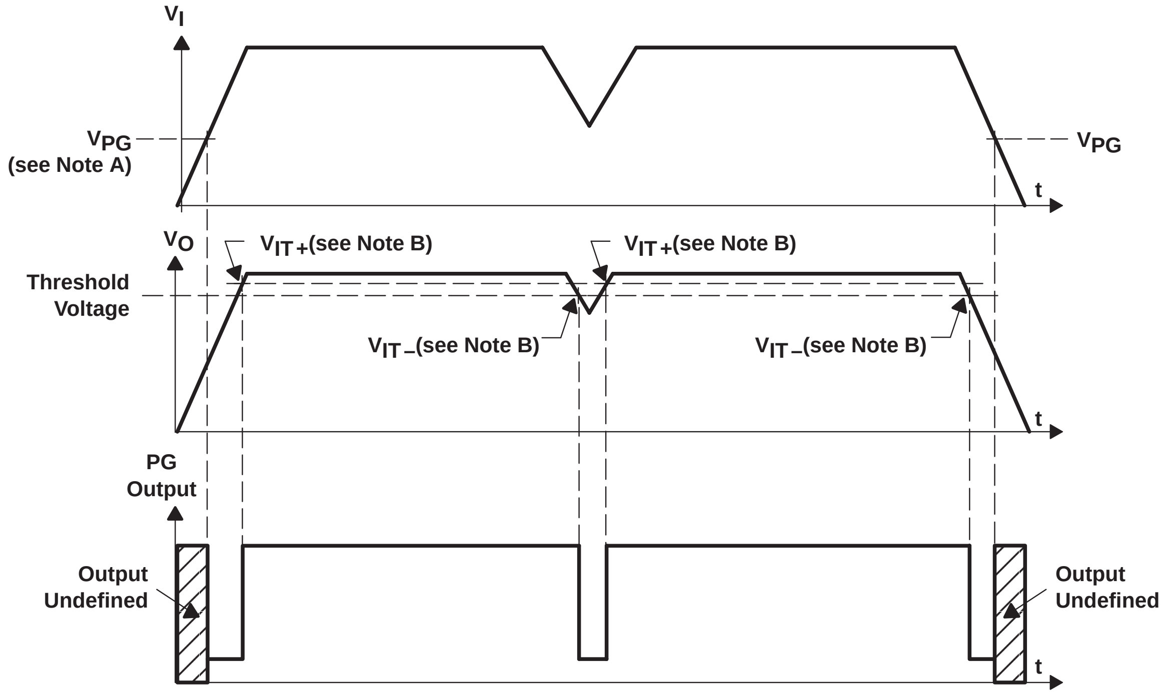
TPS752xxQ RESET timing diagram



NOTES: A. V_{res} is the minimum input voltage for a valid RESET. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. VIT –Trip voltage is typically 5% lower than the output voltage (95%V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

TPS754xxQ PG timing diagram



NOTES: A. V_{PG} is the minimum input voltage for a valid PG. The symbol V_{PG} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. VIT –Trip voltage is typically 17% lower than the output voltage (83%V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

absolute maximum ratings over operating junction temperature range (unless otherwise noted)†

Input voltage range‡, V_I . . . . . . –0.3 V to 5.5 V
Voltage range at EN . . . . . . –0.3 V to 16.5 V
Maximum RESET voltage (TPS752xxQ) . . . . . . 16.5 V
Maximum PG voltage (TPS754xxQ) . . . . . . 16.5 V
Peak output current . . . . . . Internally limited
Output voltage, V_O (OUTPUT, FB) . . . . . . 5.5 V
Continuous total power dissipation . . . . . . See dissipation rating tables
Operating virtual junction temperature range, T_J . . . . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . . . . –65°C to 150°C
ESD rating, HBM . . . . . . 2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
PWP§	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP¶	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

§ This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in^2).
¶ This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2). For more information, refer to TI technical brief SLMA002.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I#	2.7	5	V
Output voltage range, V_O	1.5	5	V
Output current, I_O	0	2.0	A
Operating virtual junction temperature, T_J	–40	125	°C

To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.

electrical characteristics over recommended operating junction temperature range (T_J = –40°C to 125°C), $V_I = V_{O(typ)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0 V, C_O = 47 μF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage (see Notes 1 and 3)	Adjustable Voltage	1.5 V ≤ V_O ≤ 5 V,	T_J = 25°C		V_O		V
		1.5 V ≤ V_O ≤ 5 V		0.98V_O		1.02V_O	
	1.5 V Output	T_J = 25°C,	2.7 V < V_{IN} < 5 V		1.5		
		2.7 V < V_{IN} < 5 V		1.470		1.530	
	1.8 V Output	T_J = 25°C,	2.8 V < V_{IN} < 5 V		1.8		
		2.8 V < V_{IN} < 5 V		1.764		1.836	
	2.5 V Output	T_J = 25°C,	3.5 V < V_{IN} < 5 V		2.5		
		3.5 V < V_{IN} < 5 V		2.450		2.550	
	3.3 V Output	T_J = 25°C,	4.3 V < V_{IN} < 5 V		3.3		
		4.3 V < V_{IN} < 5 V		3.234		3.366	
Quiescent current (GND current) (see Note 1)		T_J = 25°C,	See Note 3		75		μA
		See Note 3				125	
Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 1 and 2)		V_O + 1 V < V_I ≤ 5 V,	T_J = 25°C,		0.01		%/V
		V_O + 1 V < V_I < 5 V				0.1	
Load regulation (see Note 3)					1		mV
Output noise voltage		BW = 300 Hz to 50 kHz, V_O = 1.5 V C_O = 100 μF,	T_J = 25°C		60		μVrms
Output current Limit		V_O = 0 V			3.3	4.5	A
Thermal shutdown junction temperature					150		°C
Standby current		$\overline{EN}$ = V_I,	T_J = 25°C,		1		μA
		$\overline{EN}$ = V_I				10	μA
FB input current	TPS75x01Q	FB = 1.5 V		–1		1	μA
High level enable input voltage				2			V
Low level enable input voltage						0.7	V
Power supply ripple rejection (see Note 2)		f = 100 Hz, T_J = 25°C,	C_O = 100 μF, See Note 1, I_O = 2 A		60		dB
Reset (TPS752xxQ)	Minimum input voltage for valid $\overline{RESET}$	$I_{O(RESET)}$ = 300μA,	$V_{(RESET)}$ ≤ 0.8 V		1	1.3	V
	Trip threshold voltage	V_O decreasing		92		98	%V_O
	Hysteresis voltage	Measured at V_O			0.5		%V_O
	Output low voltage	V_I = 2.7 V,	$I_{O(RESET)}$ = 1 mA		0.15	0.4	V
	Leakage current	$V_{(RESET)}$ = 5 V				1	μA
	RESET time-out delay				100		ms

NOTES: 1. Minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum IN voltage 5V.
2. If V_O ≤ 1.8 V then V_{imin} = 2.7 V, V_{imax} = 5 V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{imax} - 2.7\ V\right)}{100} \times 1000$$

If $V_O \geq$ 2.5 V then V_{imin} = V_O + 1 V, V_{imax} = 5 V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{imax} - \left(V_O + 1\ V\right)\right)}{100} \times 1000$$

3. I_O = 1 mA to 2 A

electrical characteristics over recommended operating junction temperature range (T_J = –40°C to 125°C), $V_I = V_{O(typ)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0 V, C_O = 47 µF (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PG (TPS754xxQ)	Minimum input voltage for valid PG	$I_{O(PG)}$ = 300 µA	V(PG) ≤ 0.8 V		1.1	1.3	V
	Trip threshold voltage	V_O decreasing		80		86	$\%V_O$
	Hysteresis voltage	Measured at V_O			0.5		$\%V_O$
	Output low voltage	$I_{O(PG)}$ = 1 mA			0.15	0.4	V
	Leakage current	$V_{(PG)}$ = 5.5 V				1	µA
Input current (EN)		$\overline{EN} = V_I$		–1		1	µA
		$\overline{EN}$ = 0 V		–1	0	1	µA
High level $\overline{EN}$ input voltage				2			V
Low level $\overline{EN}$ input voltage						0.7	V
Dropout voltage (3.3 V Output) (see Note 4)		I_O = 2 A, T_J = 25°C	V_I = 3.2 V,		210		mV
		I_O = 2 A,	V_I = 3.2 V			400	

NOTE 4: IN voltage equals V_O(Typ) – 100 mV; TPS75x15Q, TPS75x18Q and TPS75x25Q dropout voltage limited by input voltage range limitations (i.e., TPS75x33Q input voltage needs to drop to 3.2 V for purpose of this test).

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	2, 3
		vs Junction temperature	4, 5,
	Ground current	vs Junction temperature	6
	Power supply ripple rejection	vs Frequency	7
	Output spectral noise density	vs Frequency	8
Z_o	Output impedance	vs Frequency	9
V_{DO}	Dropout voltage	vs Input voltage	10
		vs Junction temperature	11
	Line transient response		12, 14
	Load transient response		13, 15
V_O	Output voltage	vs Time	16
	Equivalent series resistance (ESR)	vs Output current	18, 19

TYPICAL CHARACTERISTICS

TPS75x33Q
OUTPUT VOLTAGE vs OUTPUT CURRENT

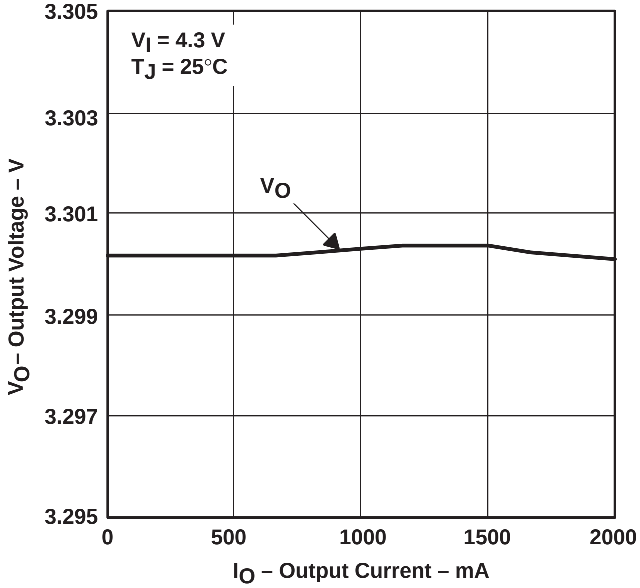


Figure 2

TPS75x15Q
OUTPUT VOLTAGE vs OUTPUT CURRENT

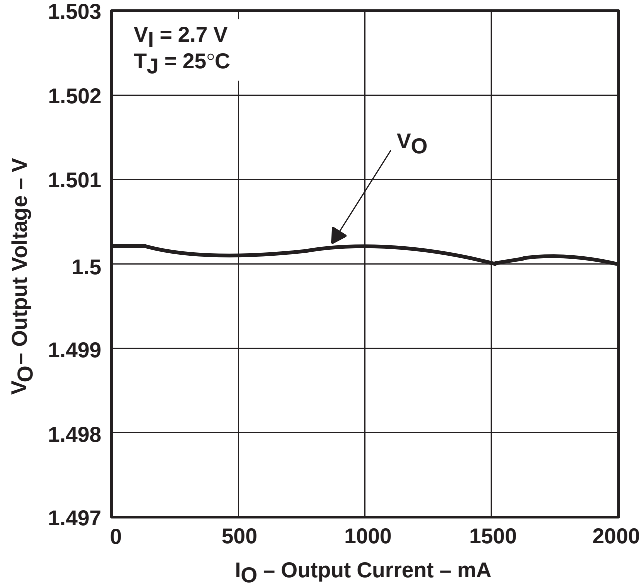


Figure 3

TPS75x33Q
OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

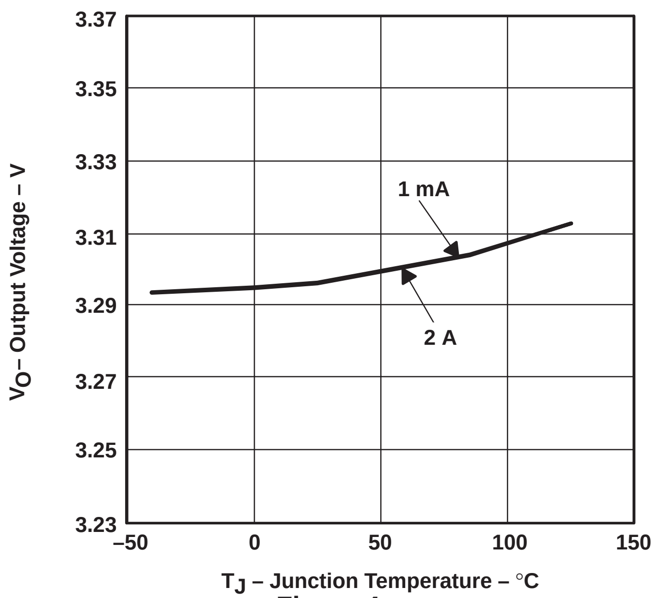


Figure 4

TPS75x15Q
OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

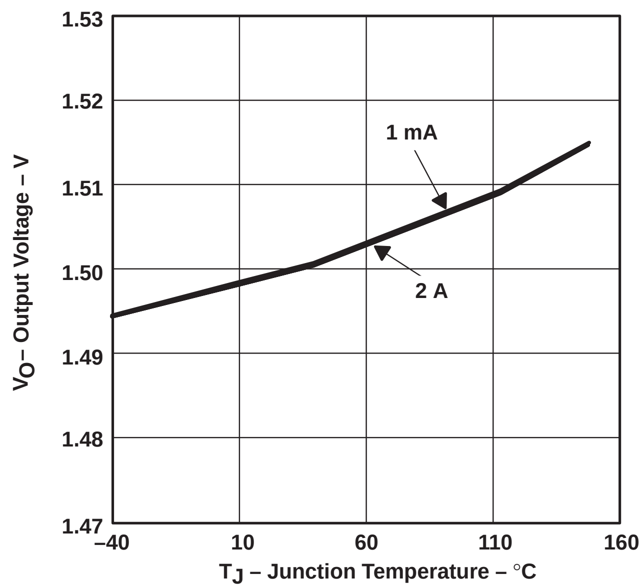


Figure 5

TYPICAL CHARACTERISTICS

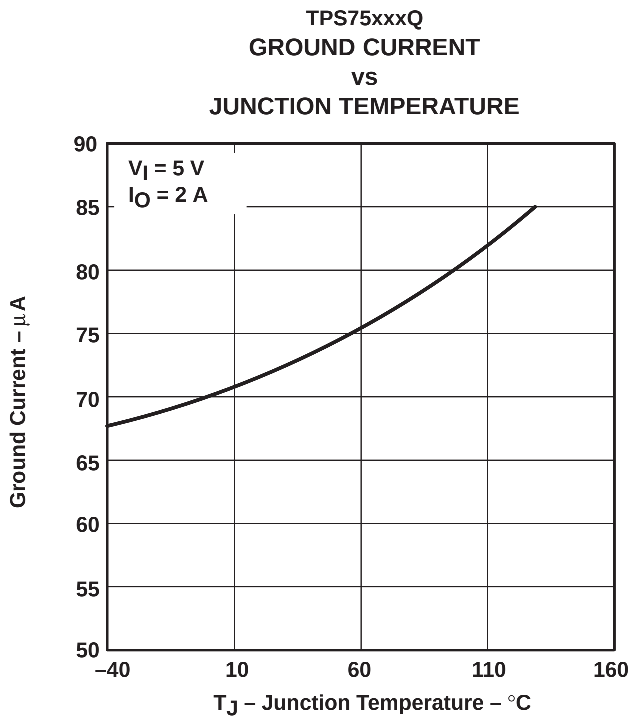


Figure 6

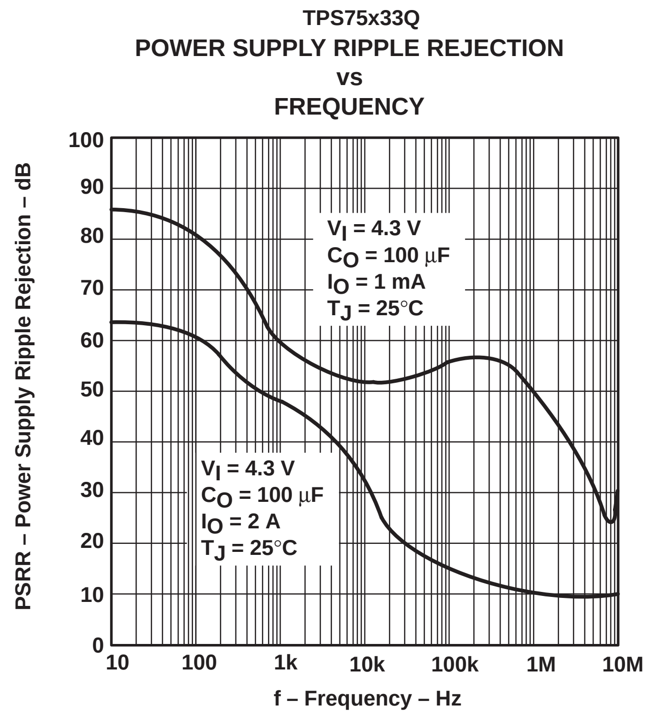


Figure 7

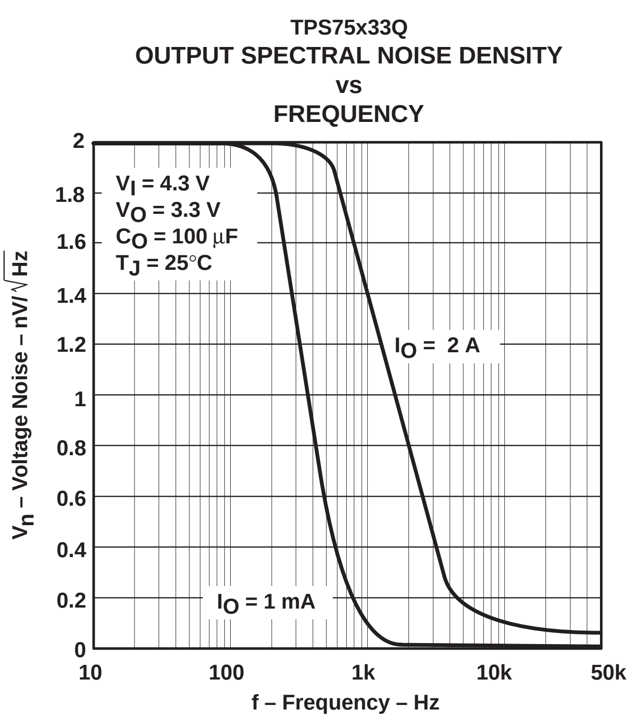


Figure 8

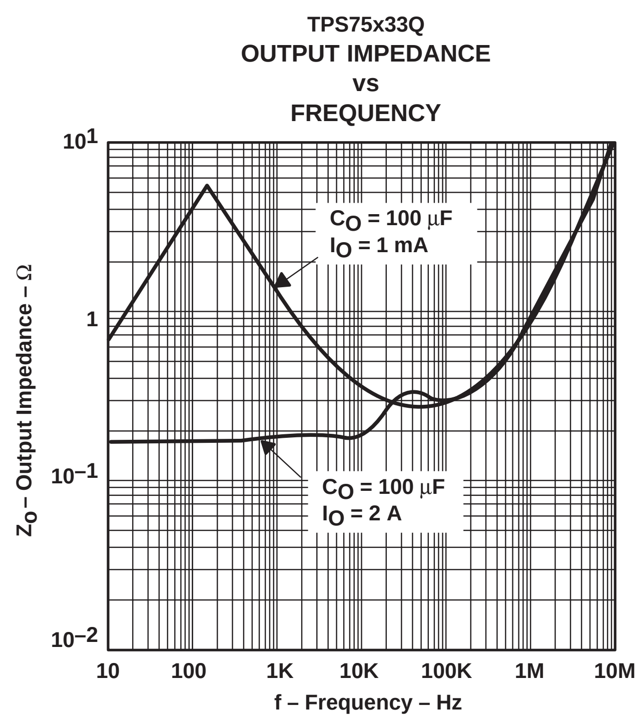


Figure 9

TYPICAL CHARACTERISTICS

TPS75x01Q
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

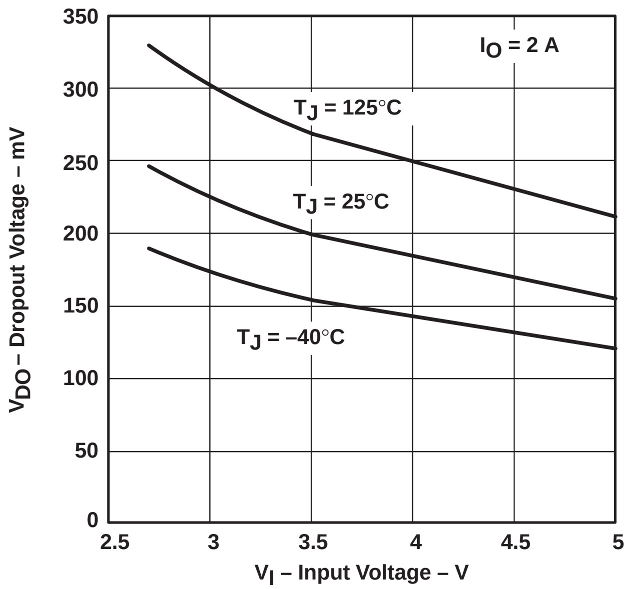


Figure 10

TPS75x33Q
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

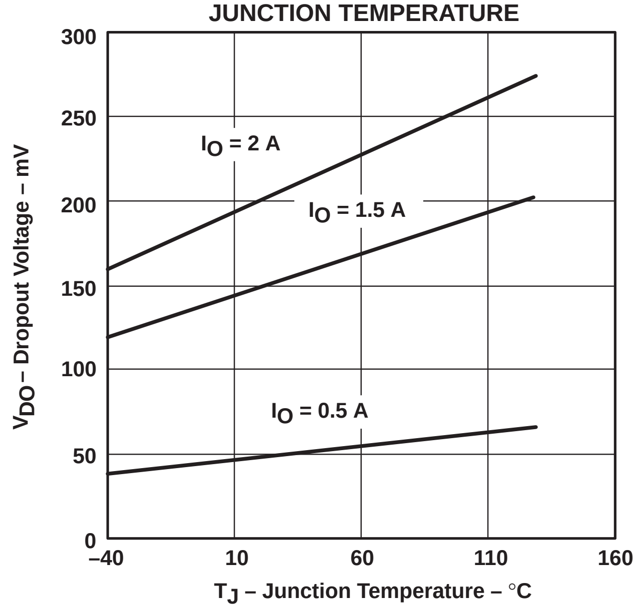


Figure 11

TPS75x15Q
LINE TRANSIENT RESPONSE

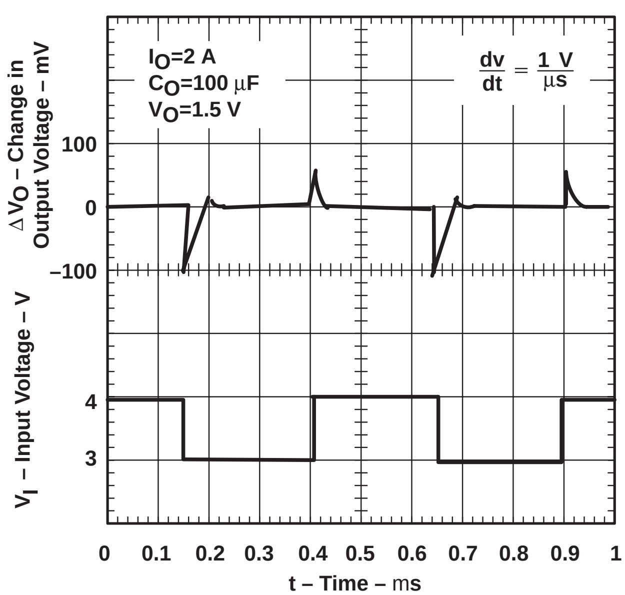


Figure 12

TPS75x15Q
LOAD TRANSIENT RESPONSE

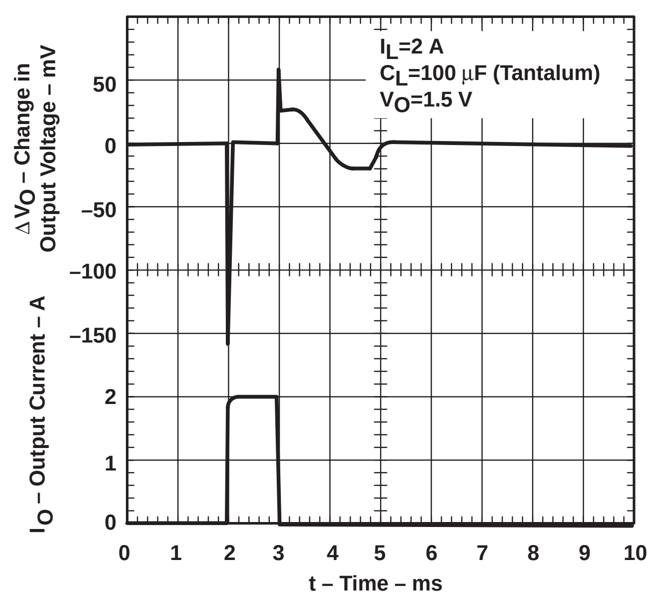


Figure 13

TYPICAL CHARACTERISTICS

TPS75x33Q
LINE TRANSIENT RESPONSE

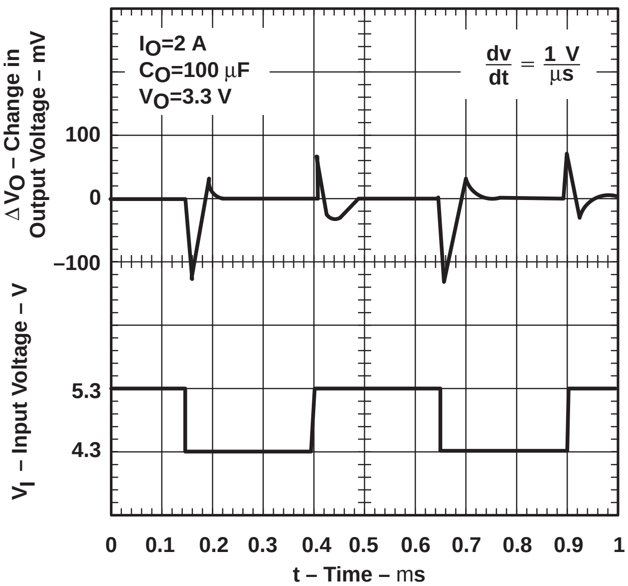


Figure 14

TPS75x33Q
LOAD TRANSIENT RESPONSE

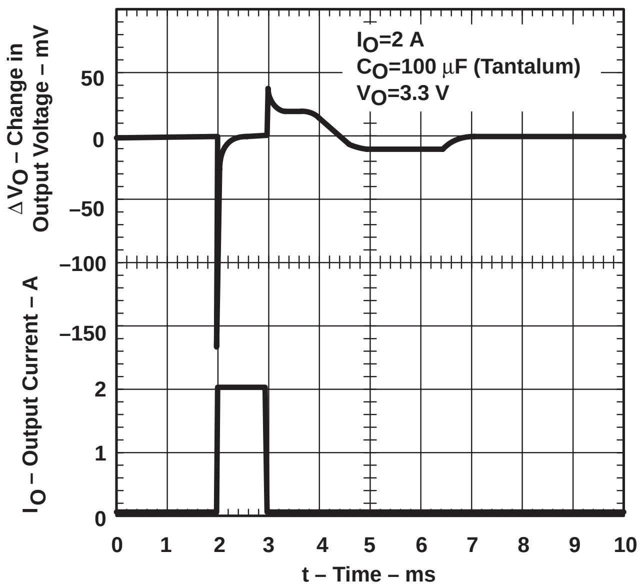


Figure 15

TPS75x33Q
OUTPUT VOLTAGE
vs
TIME (STARTUP)

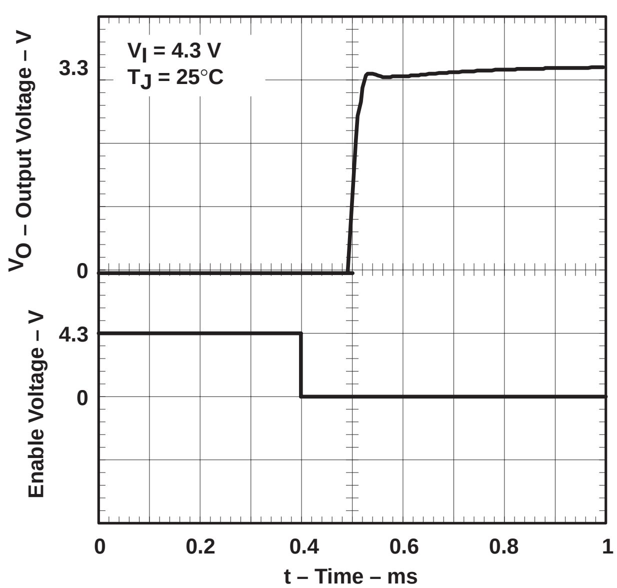


Figure 16

TYPICAL CHARACTERISTICS

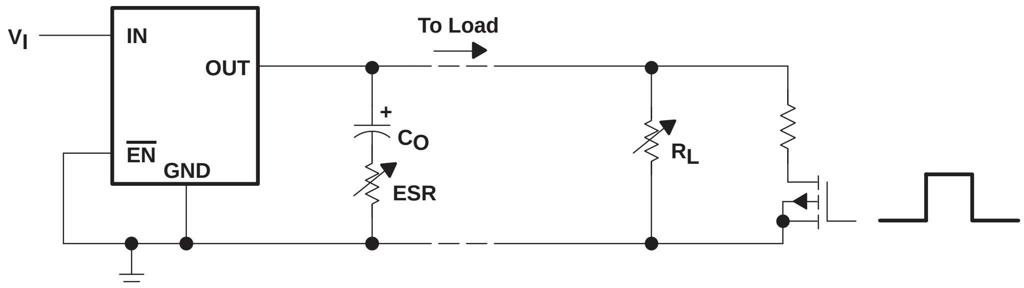


Figure 17. Test Circuit for Typical Regions of Stability (Figures 18 and 19) (Fixed Output Options)

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

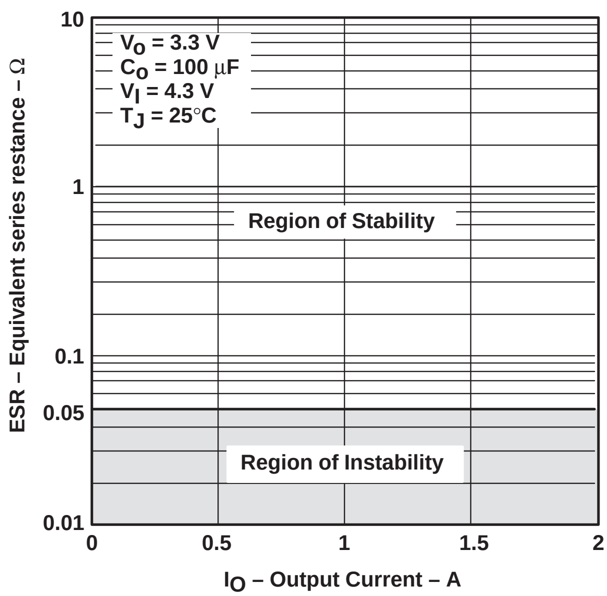


Figure 18

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

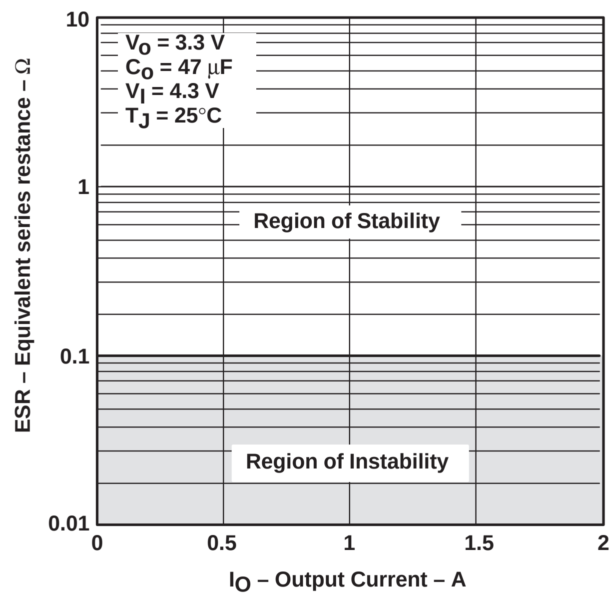


Figure 19

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

APPLICATION INFORMATION

The TPS752xxQ or TPS754xxQ families include four fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V and 3.3 V), and an adjustable regulator, the TPS75x01Q (adjustable from 1.5 V to 5 V).

minimum load requirements

The TPS752xxQ and TPS754xxQ families are stable even at no load; no minimum load is required for operation.

pin functions

enable ($\overline{\text{EN}}$)

The $\overline{\text{EN}}$ terminal is an input which enables or shuts down the device. If $\overline{\text{EN}}$ is a logic high, the device will be in shutdown mode. When $\overline{\text{EN}}$ goes to logic low, then the device will be enabled.

power good (PG) (TPS752xxQ)

The PG terminal is an open drain, active high output that indicates the status of V_O (output of the LDO). When V_O reaches 83% of the regulated voltage, PG will go to a high impedance state. It will go to a low-impedance state when V_O falls below 83% (i.e. over load condition) of the regulated voltage. The open drain output of the PG terminal requires a pullup resistor.

sense (SENSE)

The SENSE terminal of the fixed-output options must be connected to the regulator output, and the connection should be as short as possible. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way to minimize/avoid noise pickup. Adding RC networks between the SENSE terminal and V_O to filter noise is not recommended because it may cause the regulator to oscillate.

feedback (FB)

FB is an input terminal used for the adjustable-output options and must be connected to an external feedback resistor divider. The FB connection should be as short as possible. It is essential to route it in such a way to minimize/avoid noise pickup. Adding RC networks between FB terminal and V_O to filter noise is not recommended because it may cause the regulator to oscillate.

reset ($\overline{\text{RESET}}$) (TPS754xxQ)

The $\overline{\text{RESET}}$ terminal is an open drain, active low output that indicates the status of V_O. When V_O reaches 95% of the regulated voltage, $\overline{\text{RESET}}$ will go to a low-impedance state after a 100-ms delay. $\overline{\text{RESET}}$ will go to a high-impedance state when V_O is below 95% of the regulated voltage. The open-drain output of the $\overline{\text{RESET}}$ terminal requires a pullup resistor.

GND/HEATSINK

All GND/HEATSINK terminals are connected directly to the mount pad for thermal-enhanced operation. These terminals could be connected to GND or left floating.

input capacitor

For a typical application, an input bypass capacitor (0.22 µF – 1 µF) is recommended for device stability. This capacitor should be as close to the input pins as possible. For fast transient condition where droop at the input of the LDO may occur due to high inrush current, it is recommended to place a larger capacitor at the input as well. The size of this capacitor is dependant on the output current and response time of the main power supply, as well as the distance to the load (LDO).

APPLICATION INFORMATION

output capacitor

As with most LDO regulators, the TPS752xxQ and TPS754xxQ require an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 47 µF and the ESR (equivalent series resistance) must be between 100 mΩ and 10 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described in this section. Larger capacitors provide a wider range of stability and better load transient response.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet these guidelines.

ESR and transient response

LDOs typically require an external output capacitor for stability. In fast transient response applications, capacitors are used to support the load current while LDO amplifier is responding. In most applications, one capacitor is used to support both functions.

Besides its capacitance, every capacitor also contains parasitic impedances. These parasitic impedances are resistive as well as inductive. The resistive impedance is called equivalent series resistance (ESR), and the inductive impedance is called equivalent series inductance (ESL). The equivalent schematic diagram of any capacitor can therefore be drawn as shown in Figure 22.

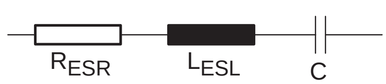


Figure 20. ESR and ESL

APPLICATION INFORMATION

In most cases one can neglect the effect of inductive impedance ESL. Therefore, the following application focuses mainly on the parasitic resistance ESR.

Figure 21 shows the output capacitor and its parasitic impedances in a typical LDO output stage.

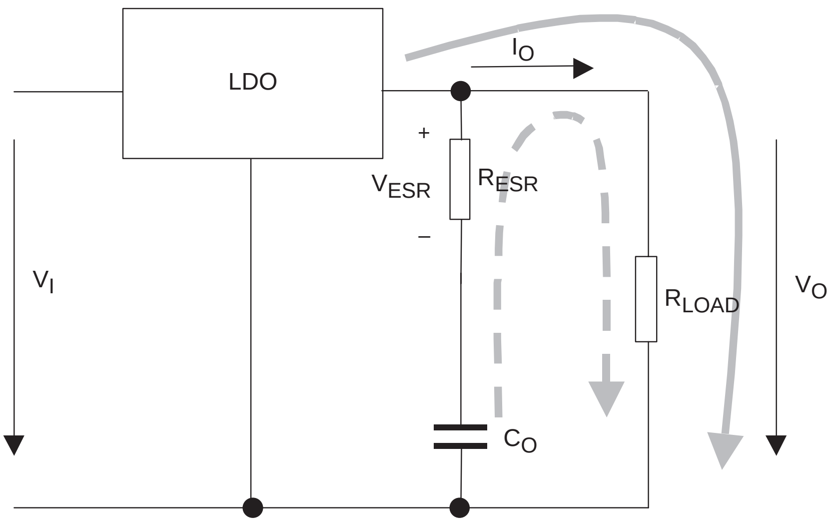


Figure 21. LDO Output Stage With Parasitic Resistances ESR and ESL

In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ($V(C_O) = V_O$). This means no current is flowing into the C_O branch. If I_O suddenly increases (transient condition), the following occurs:

- The LDO is not able to supply the sudden current need due to its response time (t_1 in Figure 22). Therefore, capacitor C_O provides the current for the new load condition (dashed arrow). C_O now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop will occur at R_{ESR}. This voltage is shown as V_{ESR} in Figure 21.
- When C_O is conducting current to the load, initial voltage at the load will be $V_O = V(C_O) – V_{ESR}$. Due to the discharge of C_O, the output voltage V_O will drop continuously until the response time t_1 of the LDO is reached and the LDO will resume supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as t_2 in Figure 22.

The figure also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

From above, the following conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage droop during the LDO response period.

APPLICATION INFORMATION

conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement.

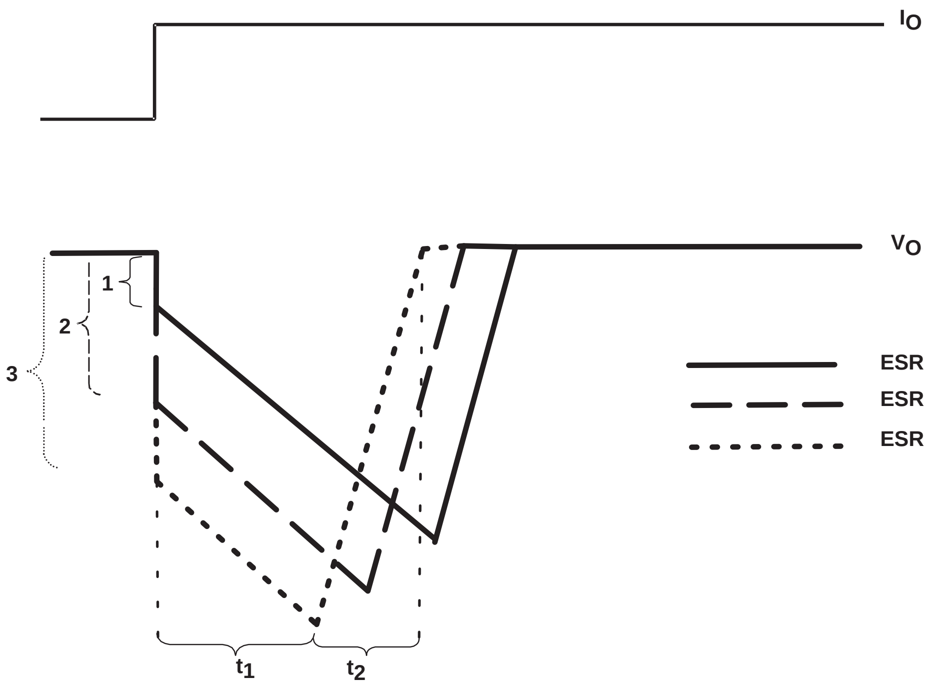


Figure 22. Correlation of Different ESRs and Their Influence to the Regulation of V_O at a Load Step From Low-to-High Output Current

APPLICATION INFORMATION

programming the TPS75x01Q adjustable LDO regulator

The output voltage of the TPS75x01Q adjustable regulator is programmed using an external resistor divider as shown in Figure 25. The output voltage is calculated using:

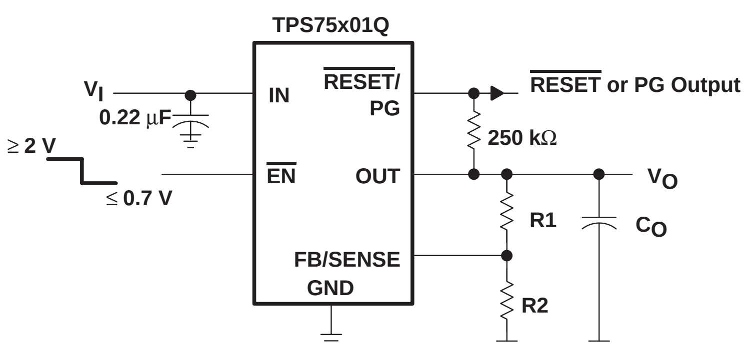
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where:

V_{ref} = 1.1834 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 40-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 40 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	33.2	30.1	kΩ
3.3 V	53.6	30.1	kΩ
3.6 V	61.9	30.1	kΩ

NOTE: To reduce noise and prevent oscillation, R1 and R2 need to be as close as possible to the FB/SENSE terminal.

Figure 23. TPS75x01Q Adjustable LDO Regulator Programming

APPLICATION INFORMATION

regulator protection

The TPS752xxQ and TPS754xxQ PMOS-pass transistors has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS752xxQ and TPS754xxQ also feature internal current limiting and thermal protection. During normal operation, the TPS752xxQ and TPS754xxQ limit output current to approximately 3.3 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \qquad (3)$$

Where:

$T_J max$ is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 34.6°C/W for the 20-terminal PWP with no airflow (see Table 1).

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O \qquad (4)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

THERMAL INFORMATION

thermally enhanced TSSOP-20 (PWP – PowerPad™)

The thermally enhanced PWP package is based on the 20-pin TSSOP, but includes a thermal pad [see Figure 24(c)] to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

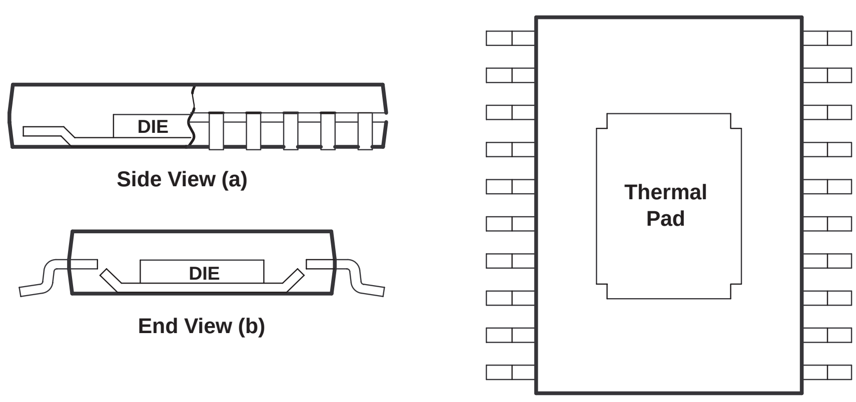


Figure 24. Views of Thermally Enhanced PWP Package

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air (reference Figure 26(a), 8 cm^2 of copper heat sink and natural convection). Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly (see Figures 25 and 26). The line drawn at 0.3 cm^2 in Figures 25 and 26 indicates performance at the minimum recommended heat-sink size, illustrated in Figure 28.

THERMAL INFORMATION

thermally enhanced TSSOP-20 (PWP – PowerPad™) (continued)

The thermal pad is directly connected to the substrate of the IC, which for the TPS752xxQPWP and TPS754xxQPWP series is a secondary electrical connection to device ground. The heat-sink surface that is added to the PWP can be a ground plane or left electrically isolated. In TO220-type surface-mount packages, the thermal connection is also the primary electrical connection for a given terminal which is not always ground. The PWP package provides up to 16 independent leads that can be used as inputs and outputs (Note: leads 1, 10, 11, and 20 are internally connected to the thermal pad and the IC substrate).

THERMAL RESISTANCE
vs
COPPER HEAT-SINK AREA

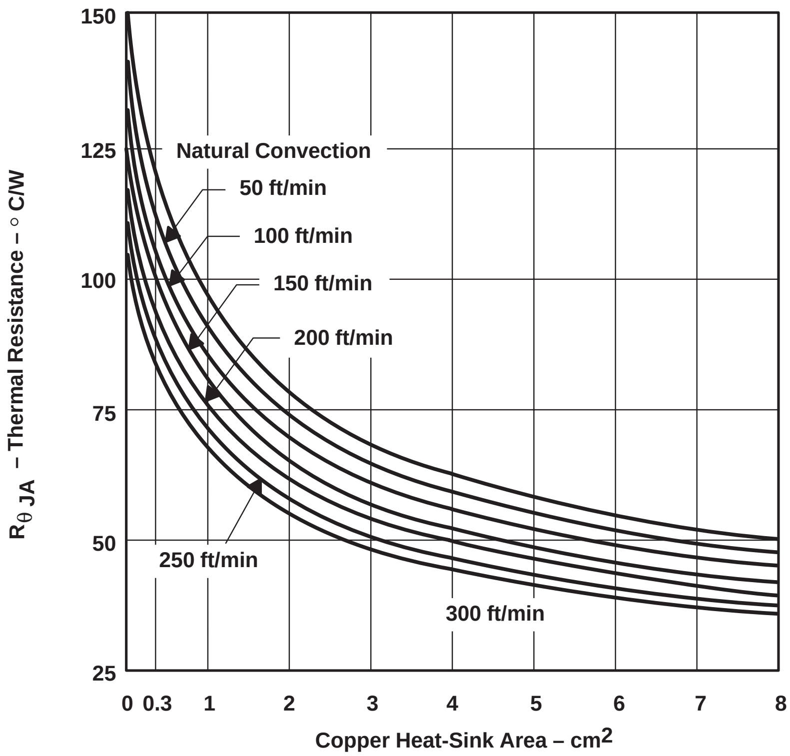


Figure 25

THERMAL INFORMATION

thermally enhanced TSSOP-20 (PWP – PowerPad™) (continued)

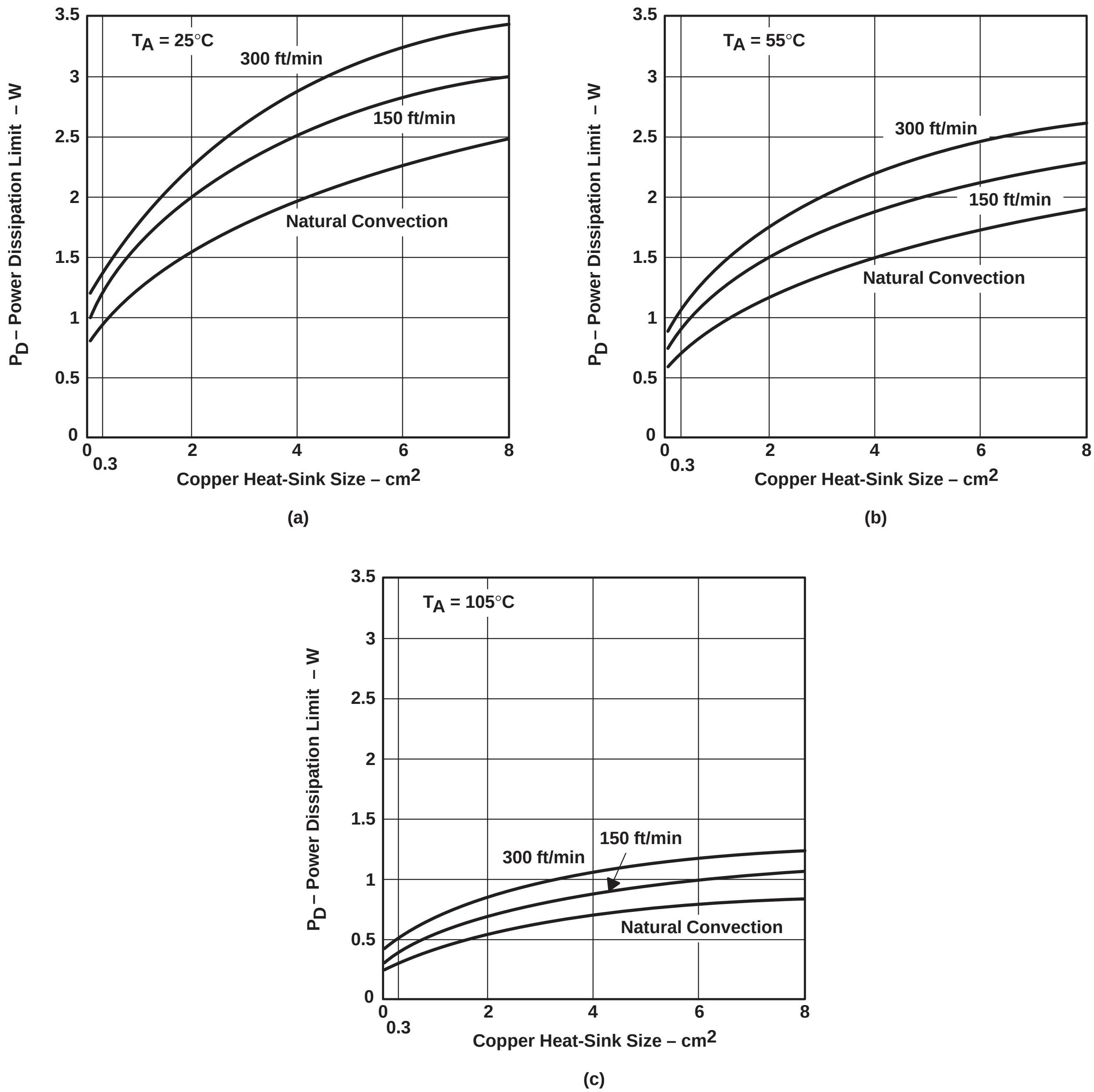
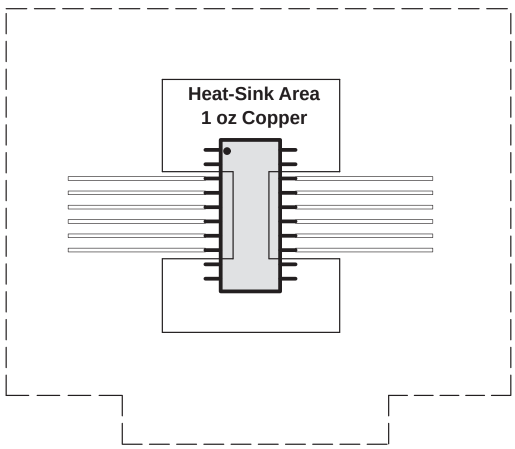


Figure 26. Power Ratings of the PWP Package at Ambient Temperatures of 25°C, 55°C, and 105°C

THERMAL INFORMATION

thermally enhanced TSSOP-20 (PWP – PowerPad™) (continued)

Figure 27 is an example of a thermally enhanced PWB layout for use with the new PWP package. This board configuration was used in the thermal experiments that generated the power ratings shown in Figure 25 and Figure 26. As discussed earlier, copper has been added on the PWB to conduct heat away from the device. $R_{\theta JA}$ for this assembly is illustrated in Figure 25 as a function of heat-sink area. A family of curves is included to illustrate the effect of airflow introduced into the system.



Board thickness	62 mils
Board size	3.2 in. × 3.2 in.
Board material	FR4
Copper trace/heat sink	1 oz
Exposed pad mounting	63/67 tin/lead solder

Figure 27. PWB Layout (Including Copper Heatsink Area) for Thermally Enhanced PWP Package

From Figure 25, $R_{\theta JA}$ for a PWB assembly can be determined and used to calculate the maximum power-dissipation limit for the component/PWB assembly, with the equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA(system)}} \tag{5}$$

Where:

$T_J$max is the maximum specified junction temperature (150°C absolute maximum limit, 125°C recommended operating limit) and T_A is the ambient temperature.

$P_{D(max)}$ should then be applied to the internal power dissipated by the TPS75233QPWP regulator. The equation for calculating total internal power dissipation of the TPS75233QPWP is:

$$P_{D(total)} = \left(V_I - V_O\right) \times I_O + V_I \times I_Q \tag{6}$$

Since the quiescent current of the TPS75233QPWP is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = \left(V_I - V_O\right) \times I_O \tag{7}$$

For the case where T_A = 55°C, airflow = 200 ft/min, copper heat-sink area = 4 cm^2, the maximum power-dissipation limit can be calculated. First, from Figure 25, we find the system $R_{\theta JA}$ is 50°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA(system)}} = \frac{125^\circ C - 55^\circ C}{50^\circ C/W} = 1.4\ W \tag{8}$$

THERMAL INFORMATION

thermally enhanced TSSOP-20 (PWP – PowerPad™) (continued)

If the system implements a TPS75233QPWP regulator, where V_I = 5 V and I_O = 800 mA, the internal power dissipation is:

$$P_{D(total)} = \left(V_I - V_O\right) \times I_O = (5 - 3.3) \times 0.8 = 1.36\ \text{W} \quad (9)$$

Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the calculated limit. When it does, one of two corrective actions should be made: raising the power-dissipation limit by increasing the airflow or the heat-sink area, or lowering the internal power dissipation of the regulator by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

mounting information

The primary requirement is to complete the thermal contact between the thermal pad and the PWB metal. The thermal pad is a solderable surface and is fully intended to be soldered at the time the component is mounted. Although voiding in the thermal-pad solder-connection is not desirable, up to 50% voiding is acceptable. The data included in Figures 25 and 26 is for soldered connections with voiding between 20% and 50%. The thermal analysis shows no significant difference resulting from the variation in voiding percentage.

Figure 28 shows the solder-mask land pattern for the PWP package. The minimum recommended heat-sink area is also illustrated. This is simply a copper plane under the body extent of the package, including metal routed under terminals 1, 10, 11, and 20.

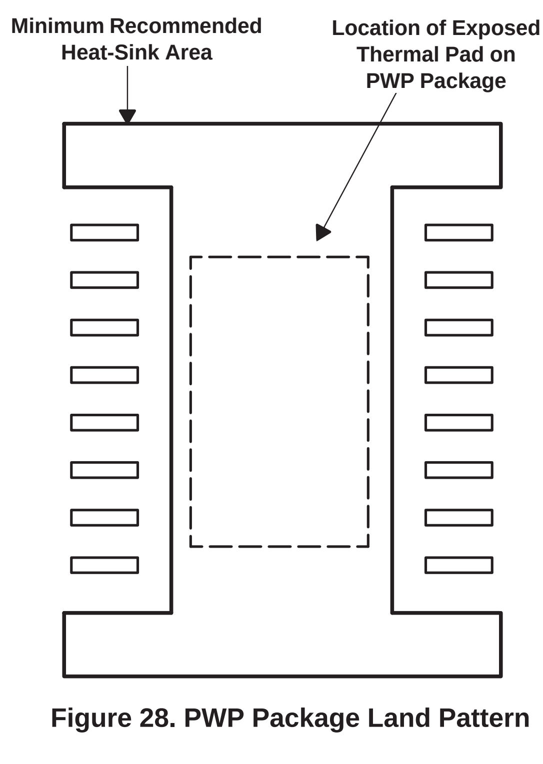
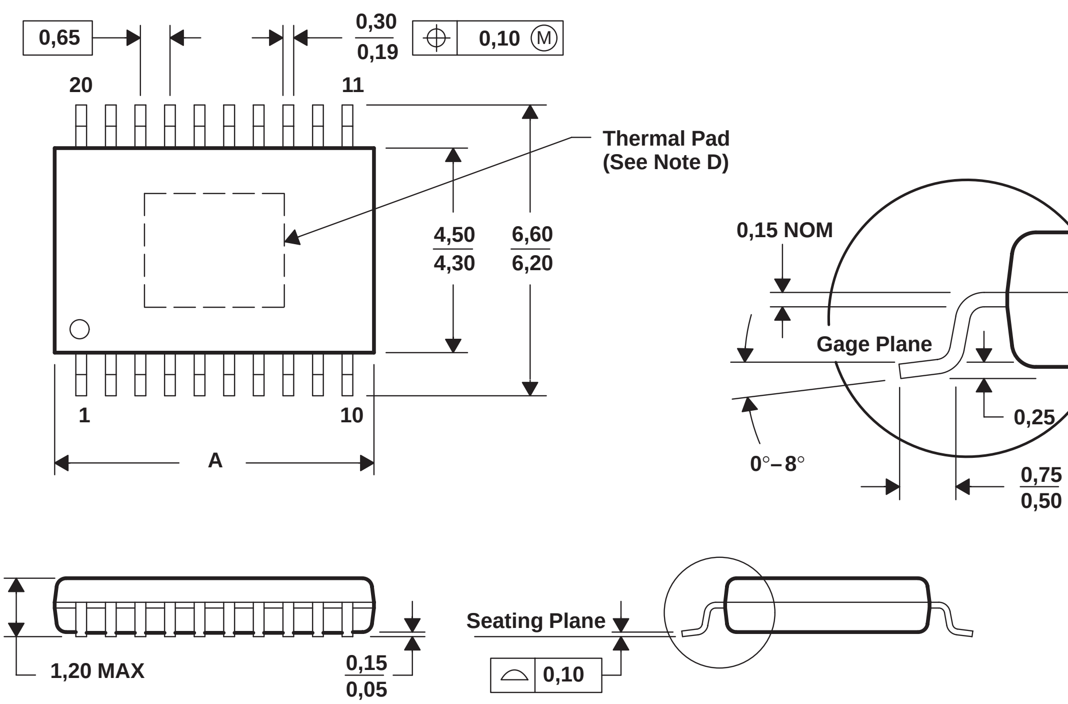


Figure 28. PWP Package Land Pattern

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

20-PIN SHOWN



PINS ** / DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/E 03/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

IMPORTANT NOTICE