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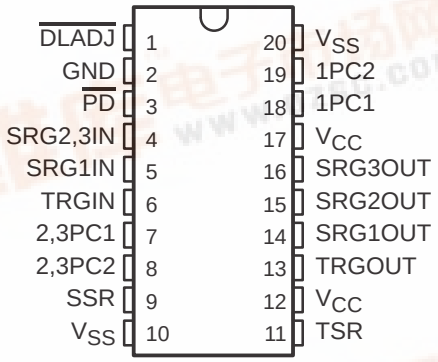
TMS3472A SERIAL DRIVER

SOCS025B – FEBRUARY 1991

- TTL-Compatible Inputs
- CCD-Compatible Outputs
- Variable-Output Slew Rates With External Resistor Control
- Frame-Transfer Operation
- Solid-State Reliability
- Adjustable Clock Levels

DW PACKAGE
(TOP VIEW)



description

The TMS3472A serial driver is a monolithic CMOS integrated circuit designed to drive the serial-register gate (SRGn) and transfer-gate (TRG) inputs of the Texas Instruments (TI™) TC241 (monochrome) CCD image sensor. The TMS3472A interfaces the TI TMS3471C or a user-defined timing generator to the TC241; it receives TTL signals from the timing generator and outputs level-shifted and slew-rate-adjusted signals to the image sensor. The TMS3472A contains three noninverting serial drivers and one noninverting transfer driver as well as circuitry for slew-rate adjustment.

The voltage levels on SRG1OUT, SRG2OUT, SRG3OUT, and TRGOUT are controlled by the levels on V_{SS} and V_{CC}. $\overline{\text{DLADJ}}$, $\overline{\text{PD}}$, SRG1IN, SRG2,3IN, and TRGIN are TTL compatible. A high level on $\overline{\text{PD}}$ allows the TMS3472 to operate normally with the level-shifted and slew-rate-adjusted outputs following the inputs. When $\overline{\text{PD}}$ is low, the device is in a low power-consumption mode and all outputs are at V_{CC}.

The slew rate of SRG1OUT, SRG2OUT, and SRG3OUT is controlled by connecting a resistor between V_{CC} and SSR. The TRGOUT slew rate is controlled by connecting a resistor between V_{CC} and TSR. The larger the resistor values, the longer the rise and fall times are.

The TMS3472A is available in a 20-pin surface-mount package (DW) and is characterized for operation from –20°C to 45°C.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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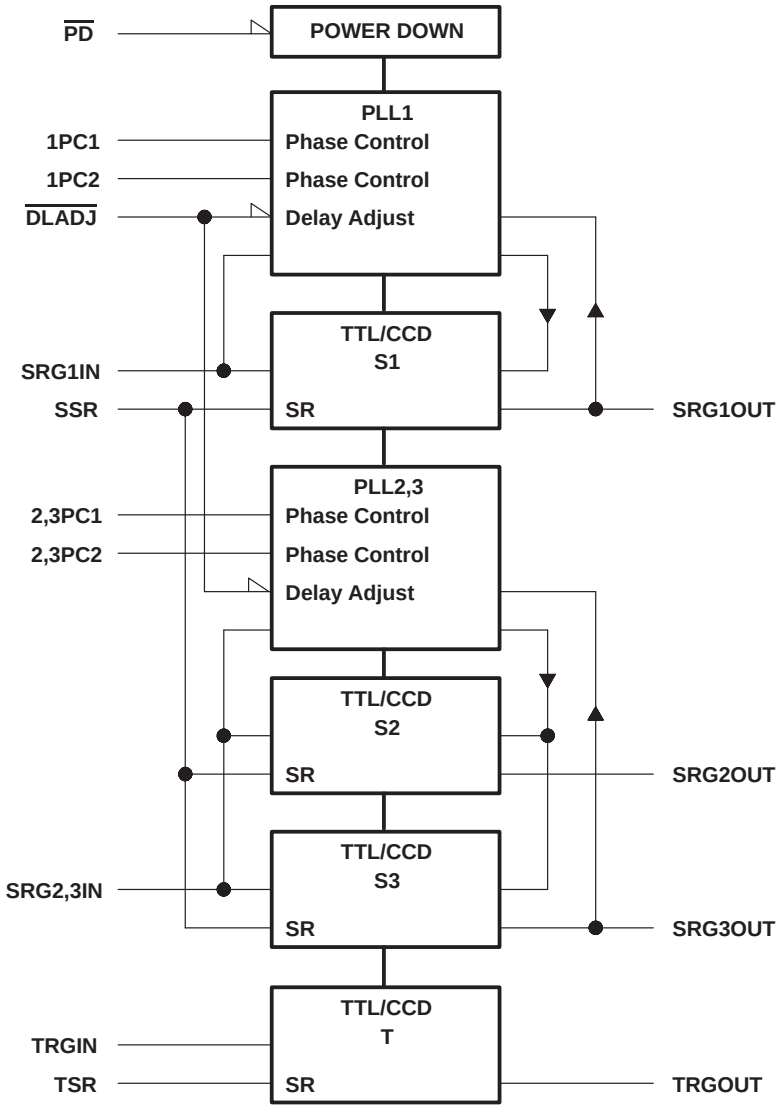
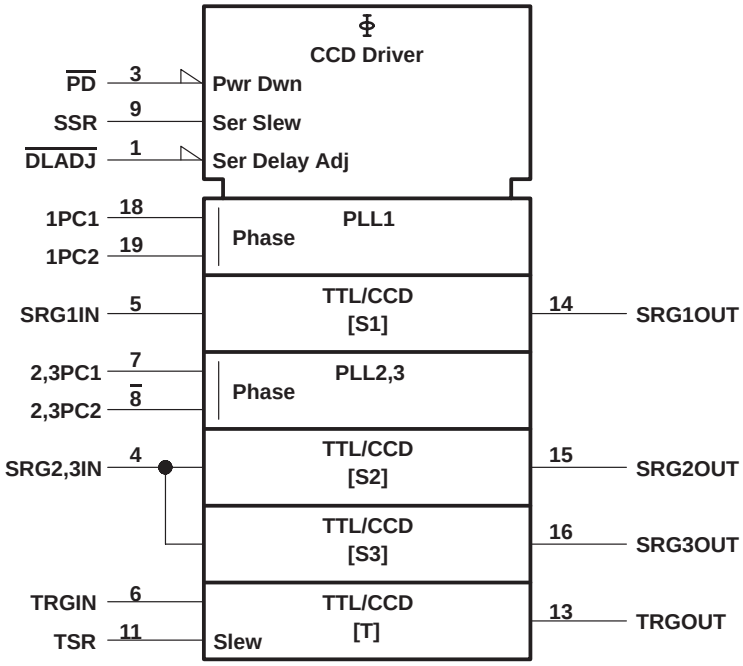
TEXAS INSTRUMENTS

functional block diagram



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{DLADJ}}$	1	I	Delay adjust for all serial-register gates
GND	2		Ground
2,3PC1‡	7	I	Phase-adjust control for SRG2OUT, SRG3OUT
2,3PC2‡	8	I	
1PC1‡	18	I	Phase-adjust control for SRG1OUT
1PC2‡	19	I	
$\overline{\text{PD}}$	3	I	Power down
SRG1IN	5	I	Serial-register gate 2 and 3 in
SRG2,3IN	4	I	Serial-register gate 1 in
SRG1OUT	14	O	Serial-register gate 1 out
SRG2OUT	15	O	Serial-register gate 2 out
SRG3OUT	16	O	Serial-register gate 3 out
SSR	9	I	Serial-register gate out slew-rate adjust
TRGIN	6	I	Transfer gate in
TRGOUT	13	O	Transfer gate out
TSR	11	I	Transfer gate out slew-rate adjust
V_{CC}§	12	I	Positive supply voltage
V_{CC}§	17	I	
V_{SS}§	10	I	Negative supply voltage
V_{SS}§	20	I	

‡ A 270-pF capacitor should be connected between terminals 7 and 8 and between terminals 18 and 19.

§ All terminals of the same name should be connected together externally.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Positive supply voltage, V_{CC} (see Note 1) . . . . . 3 V
Negative supply voltage, V_{SS} (see Note 2) . . . . . –11.1 V
Continuous total power dissipation at (or below), $T_A \le 25°C$:
Unmounted device (see Figure 1) . . . . . 825 mW
Mounted device (see Figure 1) . . . . . 1150 mW
Operating free-air temperature range, T_A . . . . . – 20°C to 45°C
Storage temperature range, T_{STG} . . . . . – 55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for voltage levels only.

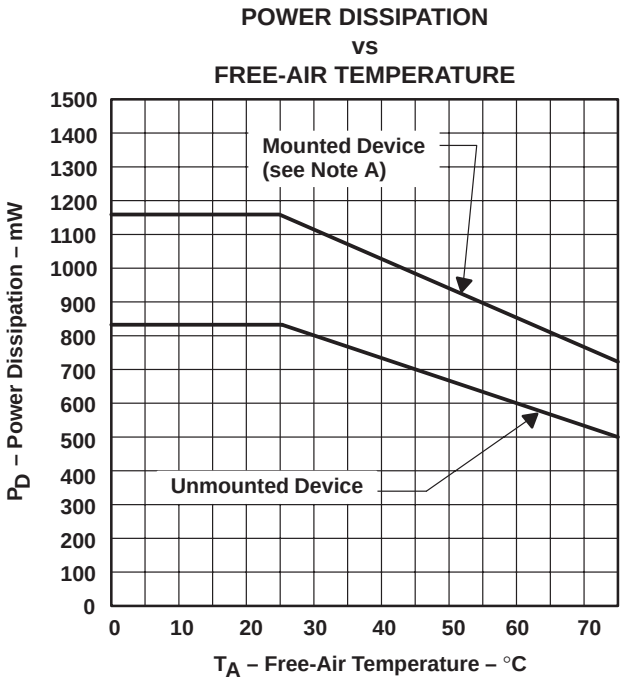


Figure 1

NOTE A: The mounted-device derating curve of Figure 1 is obtained under the following conditions:
The board is 50 mm by 50 mm by 1.6 mm thick.
The board material is glass epoxy.
The copper thickness of all the etch runs is 35 microns.
Etch run dimensions – All 20 etch runs are 0.4 mm by 22 mm.
Each chip is soldered to the board.
An aluminum cooling fin 10 mm by 10 mm by 1 mm thick is coupled to the chip with thermal paste.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC}†		0	1	2.2	V
Negative supply voltage, V_{SS} (see Note 2)†		–11.1	–10.4	–9.7	V
High-level input voltage, V_{IH}	$\overline{DLADJ}$, SRG1IN, SRG2,3IN, TRGIN	2	5		V
	$\overline{PD}$	2.5	5		
Low-level input voltage, V_{IL}	$\overline{DLADJ}$, SRG1IN, SRG2,3IN, TRGIN		0	0.8	V
	$\overline{PD}$		0	0.9	
Slope-bias resistance		10		50	kΩ
Operating free-air temperature, T_A		–20		45	°C

† V_{CC} and V_{SS} have 100-mA current limits. Adequate decoupling capacitors are required from these pins to ground.

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)‡

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH\ (serial)}$ = 48 mA (peak), $I_{OH\ (transfer)}$ = 67 mA (peak)	V_{CC}–0.5	V_{CC}	V_{CC}+0.5	V
V_{OL}	Low-level output voltage	$I_{OL\ (serial)}$ = 48 mA (peak), $I_{OL\ (transfer)}$ = 32 mA (peak)	V_{SS}–0.6	V_{SS}	V_{SS}+0.8	V
I_{IH}	High-level input current	V_{IH} = 5 V			50	µA
I_{IL}	Low-level input current	V_{IL} = 0			±10	µA
I_{SS}	Supply current	No load, $\overline{PD}$ at 0 V			–0.85	mA
		Average load			–55	

‡ These parameters are measured with T_A = 25°C, V_{SS} = –10.3 V, V_{CC} = 2.1 V, slope-bias resistance on SSR and TSR = 22 kΩ, frequency of SRG1OUT, SRG2OUT, and SRG3OUT = 4.8 MHz, and frequency of TRGOUT = 2.1 MHz. The load is a TC241 monochrome CCD image sensor.

switching characteristics for SRG1OUT, SRG2OUT, and SRG3OUT

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
	Jitter	See Note 3		2	ns
t_{d1}	See Figure 2		15	30	ns
t_{d2}				37	ns
t_{d3}			82		ns
$t_{w(H)}$	Pulse duration, high		35		ns
$t_{w(L)}$	Pulse duration, low		65		ns
	Slew rate			400	V/μs
	Noise amplitude			300	mV

NOTE 3: These parameters are measured with T_A = 25°C, V_{SS} = –10.3 V, V_{CC} = 2.1 V, slope-bias resistance on SSR = 22 kΩ, and frequency of SRG1OUT, SRG2OUT, and SRG3OUT = 4.8 MHz. The load is a TC241 monochrome CCD image sensor.

switching characteristics for TRGOUT

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_r	Rise time	See Note 4	135	185	ns
t_f	Fall time		50	100	ns

NOTE 4: These parameters are measured with T_A = 25°C, V_{SS} = –10.3 V, V_{CC} = 2.1 V, slope-bias resistance on TSR = 22 kΩ, and frequency of TRGOUT = 2.1 MHz. The load is a TC241 monochrome CCD image sensor.

PARAMETER MEASUREMENT INFORMATION

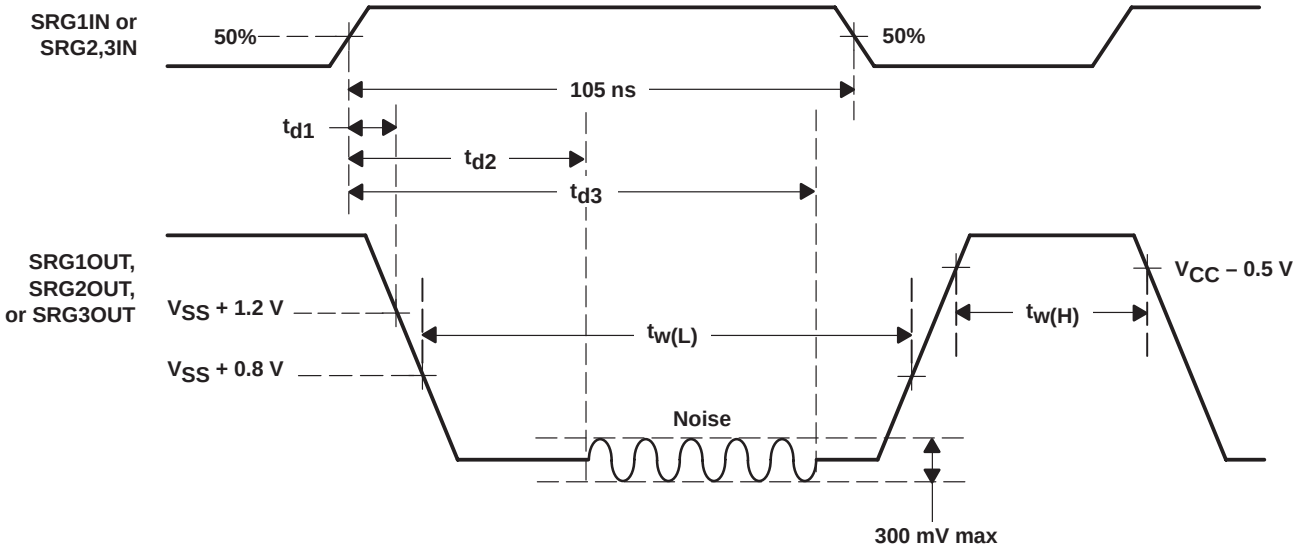
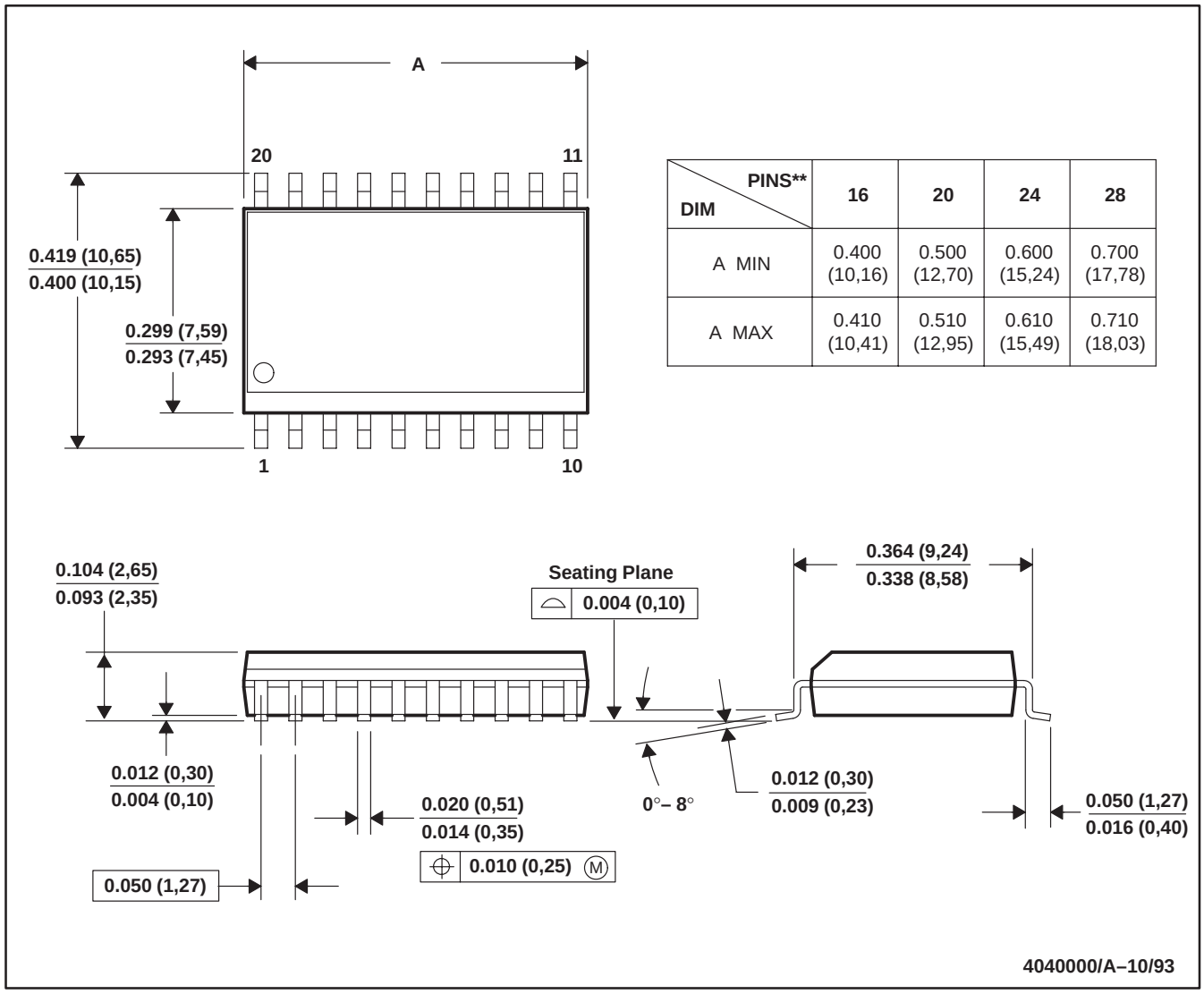


Figure 2. Serial-Register-Gate Timing Diagram

MECHANICAL DATA

DW/R-PDSO-G** **PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE**

20 PIN SHOWN



DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

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