NEC

# MOS FIELD EFFECT TRANSISTOR

# 2SK3307

## SWITCHING
## N-CHANNEL POWER MOS FET
## INDUSTRIAL USE

### DESCRIPTION

The 2SK3307 is N-channel MOS Field Effect Transistor designed for high current switching applications.

### ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|---|---|
| 2SK3307 | TO-3P |

### FEATURES

- Super low on-state resistance:

★ $R_{DS(on)1}$ = 9.5 mΩ MAX. ($V_{GS}$ = 10 V, $I_D$ = 35 A)

★ $R_{DS(on)2}$ = 14 mΩ MAX. ($V_{GS}$ = 4 V, $I_D$ = 35 A)

- Low $C_{iss}$: $C_{iss}$ = 4650 pF TYP.
- Built-in gate protection diode

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C)

| | | | | |
|---|---|---|---|---|
| | Drain to Source Voltage | $V_{DSS}$ | 60 | V |
| | Gate to Source Voltage | $V_{GSS(AC)}$ | ±20 | V |
| | Drain Current (DC) | $I_{D(DC)}$ | ±70 | A |
| | Drain Current (pulse) Note1 | $I_{D(pulse)}$ | ±280 | A |
| ★ | Total Power Dissipation ($T_C$ = 25°C) | $P_T$ | 120 | W |
| | Total Power Dissipation ($T_A$ = 25°C) | $P_T$ | 3.0 | W |
| | Channel Temperature | $T_{ch}$ | 150 | °C |
| | Storage Temperature | $T_{stg}$ | –55 to +150 | °C |
| ★ | Single Avalanche Current Note2 | $I_{AS}$ | 45 | A |
| ★ | Single Avalanche Energy Note2 | $E_{AS}$ | 202 | mJ |

**Notes 1.** PW ≤ 10 μs, Duty cycle ≤ 1 %

★ **2.** Starting $T_{ch}$ = 25 °C, $R_G$ = 25 Ω, $V_{GS}$ = 20 V → 0 V

### THERMAL RESISTANCE

| | | | | |
|---|---|---|---|---|
| ★ | Channel to Case | Rth(ch-C) | 1.04 | °C/W |
| | Channel to Ambient | Rth(ch-A) | 41.7 | °C/W |



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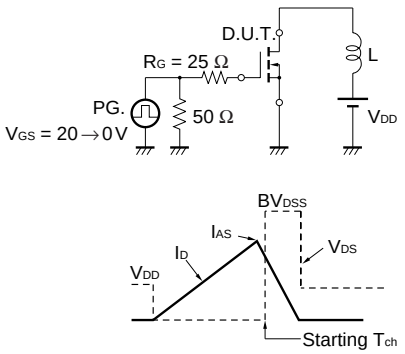
The mark ★ shows major revised points.

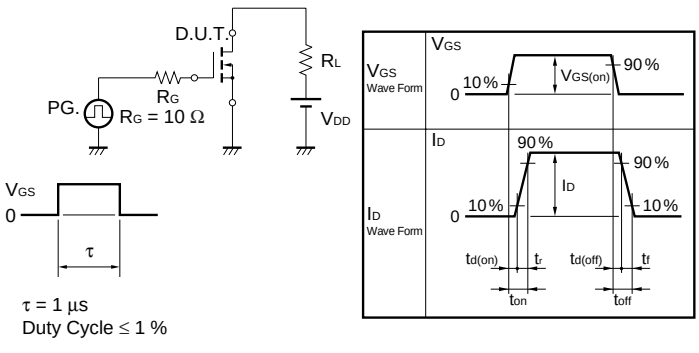
## ★ ELECTRICAL CHARACTERISTICS ($T_A$ = 25 °C)

| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Drain to Source On-state Resistance | $R_{DS(on)1}$ | $V_{GS}$ = 10 V, $I_D$ = 35 A | | 7.5 | 9.5 | mΩ |
| | $R_{DS(on)2}$ | $V_{GS}$ = 4 V, $I_D$ = 35 A | | 10.5 | 14 | mΩ |
| Gate to Source Cut-off Voltage | $V_{GS(off)}$ | $V_{DS}$ = 10 V, $I_D$ = 1 mA | 1.5 | 2.0 | 2.5 | V |
| Forward Transfer Admittance | $\|y_{fs}\|$ | $V_{DS}$ = 10 V, $I_D$ = 35 A | 30 | 47 | | S |
| Drain Leakage Current | $I_{DSS}$ | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | | | 10 | μA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±10 | μA |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz | | 4650 | | pF |
| Output Capacitance | $C_{oss}$ | | | 780 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 380 | | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $I_D$ = 35 A, $V_{GS(on)}$ = 10 V, $V_{DD}$ = 30 V, | | 90 | | ns |
| Rise Time | $t_r$ | $R_G$ = 10 Ω | | 1260 | | ns |
| Turn-off Delay Time | $t_{d(off)}$ | | | 270 | | ns |
| Fall Time | $t_f$ | | | 370 | | ns |
| Total Gate Charge | $Q_G$ | $I_D$ = 70 A , $V_{DD}$ = 48 V, $V_{GS}$ = 10 V | | 90 | | nC |
| Gate to Source Charge | $Q_{GS}$ | | | 14 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | | | 38 | | nC |
| Body Diode Forward Voltage | $V_{F(S-D)}$ | $I_F$ = 70 A, $V_{GS}$ = 0 V | | 1.0 | | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 70 A, $V_{GS}$ = 0 V, | | 60 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 100 A/μs | | 110 | | nC |

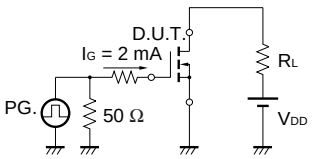
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**




**TEST CIRCUIT 2 SWITCHING TIME**

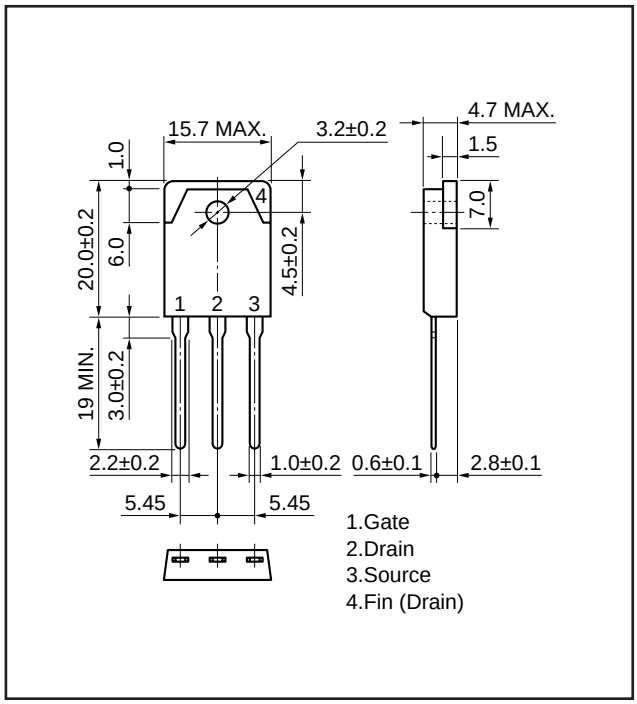



**TEST CIRCUIT 3 GATE CHARGE**

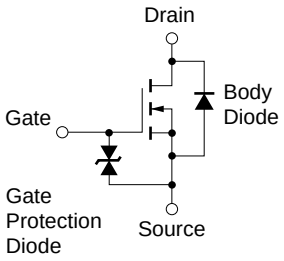


## PACKAGE DRAWING (Unit: mm)

**TO-3P (MP-88)**




## EQUIVALENT CIRCUIT




**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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