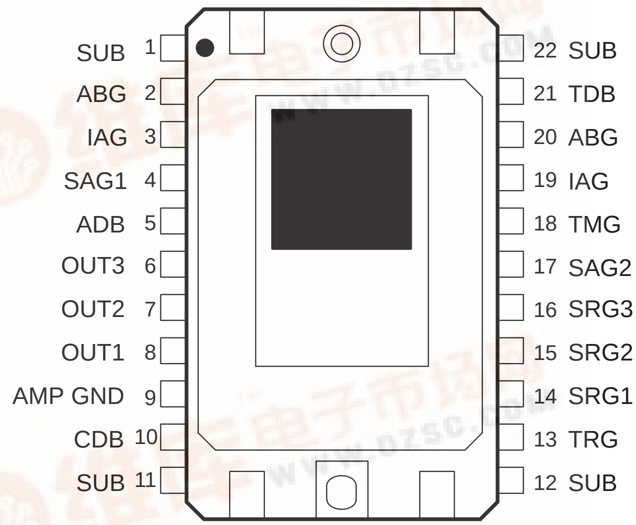
- **High-Resolution, Solid-State Monochrome Image Sensor for Video or Still-Picture Photography**
- **Frame Transfer With Two Field Memories Allows Multimode Operation**
- **1044 (H) x 576 (V) Active Elements in Image-Sensing Area**
- **11-mm Image-Area Diagonal Is Compatible With 2/3” Vidicon Optics**
- **Fast-Clear Capability**
- **Electron-Hole Recombination Antiblooming**
- **Dynamic Range . . . More Than 60 dB**
- **High Photoresponse Uniformity**
- **On-Chip Cross-Coupled Resets for Easy Off-Chip Implementation of CCSH Video-Signal Processing**
- **Solid-State Reliability With No Image Burn-in, Residual Imaging, Image Distortion, Image Lag, or Microphonics**
- **Low Dark Current**

DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TC271 is a frame-transfer charge-coupled-device (CCD) image sensor with two field memories. It is suitable for use in PAL-video or still-picture photography applications. Its image-sensing area is configured into 580 lines; 576 of these are active and the remaining four are used for dark reference. Each line is configured into 1080 pixels with 1044 active and 36 for dark reference. The TC271 has a standard aspect ratio of 4:3 and a standard 11-mm image-sensing-area diagonal. Its blooming protection, which is an integral part of each pixel, is based on electron-hole recombination and is activated by clocking the antiblooming gate.

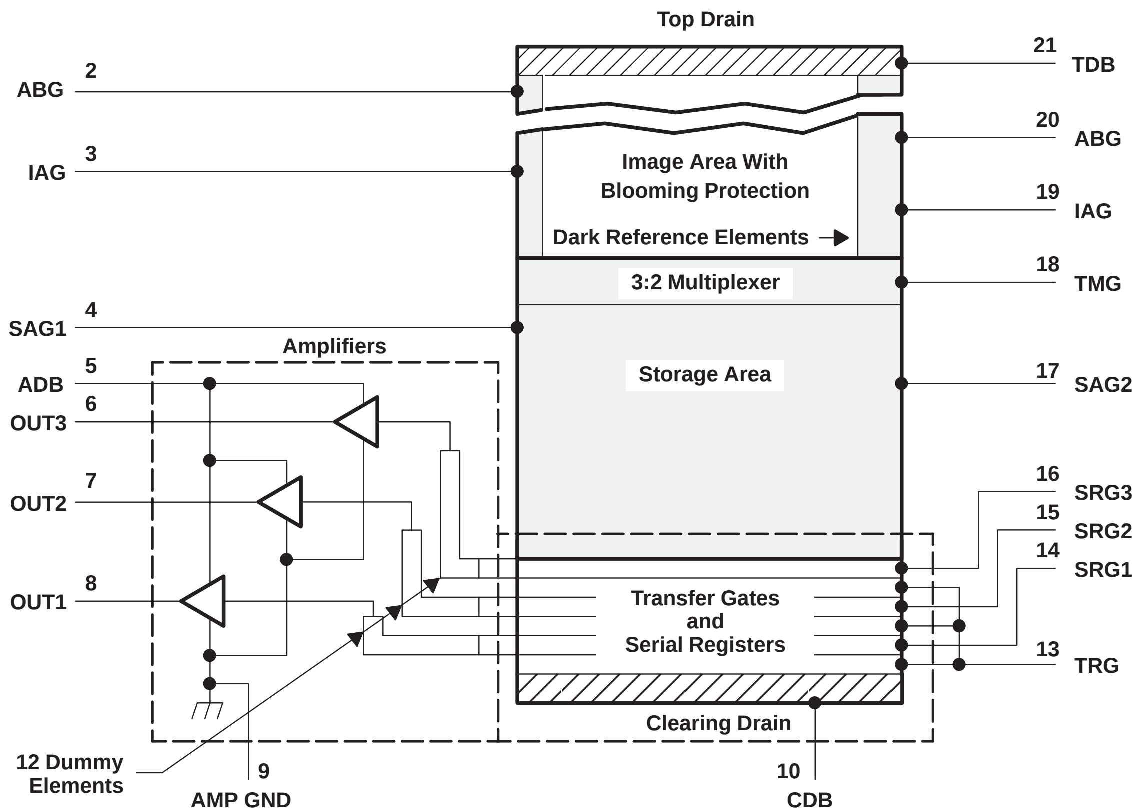
One important aspect of the TC271 high-resolution sensor is its ability to simultaneously capture both fields of a TV frame. Its two independently addressable memories allow separate storage of each field and operation in a variety of modes, including CCIR with true interlace, CCIR with pseudointerlace, progressive scan, and nonstandard pseudointerlace with a resolution of 1152 lines.

A unique multiplexer section (see Figure 1) rearranges the horizontal pixels into vertical groups of three and separates and loads the image into the two field memories. The independent addressing of each field memory provides flexibility for different modes of operation. The interdigitated layout of the memories allows each memory to share the same bank of three serial registers and associated charge-detection amplifiers (see Figure 2 and the functional block diagram). Each register and associated amplifier reads out every third column of the image area (see Figure 3). The three amplifiers are optimized dual-source followers that allow the use of off-chip double correlated-clamp sample-and-hold amplifiers for removing KTC noise.

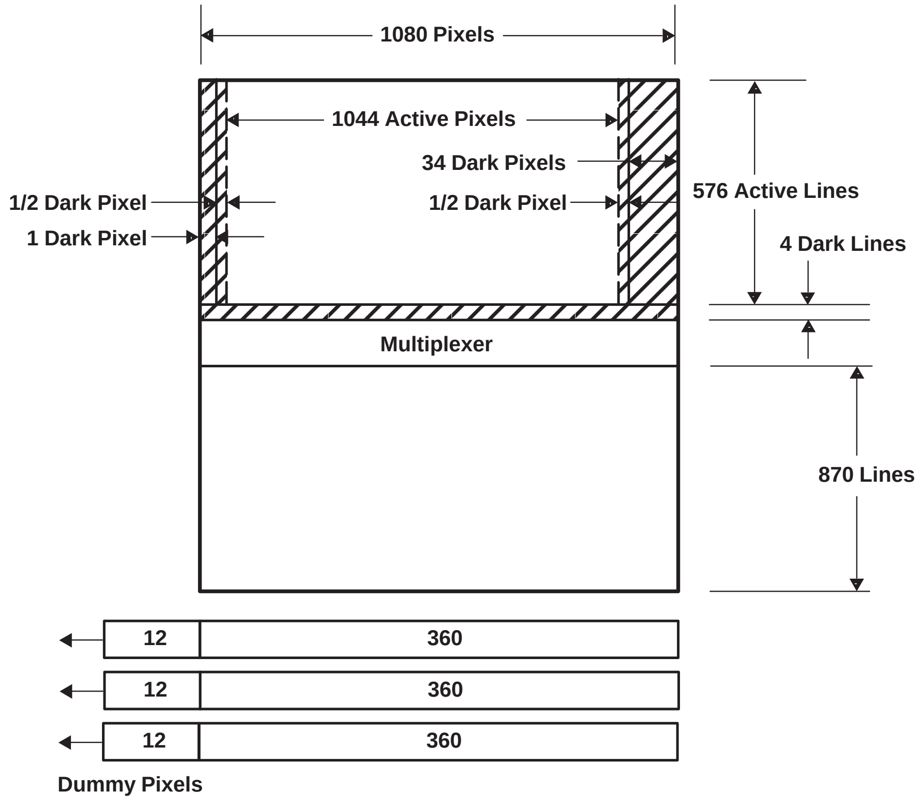
The TC271 is built using TI-proprietary virtual-phase technology, which provides devices with high blue response, low dark current, high photoresponse uniformity, and single-phase clocking. The TC271 is characterized for operation from –10°C to 40°C.

This MOS device contains limited built-in gate protection. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to SUB. Under no circumstances should pin voltages exceed absolute maximum ratings. Avoid shorting OUTn to ADB during operation to prevent damage to the amplifier. The device can also be damaged if the output terminals are reverse-biased and an excessive current is allowed to flow. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

functional block diagram



sensor topology diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ABG†	2	I	Antiblooming gate
ABG†	20	I	Antiblooming gate
ADB	5	I	Supply voltage for amplifier-drain bias
AMP GND	9		Amplifier ground
CDB	10	I	Supply voltage for clearing-drain bias
IAG†	3	I	Image-area gate
IAG†	19	I	Image-area gate
OUT1	8	O	Output signal 1
OUT2	7	O	Output signal 2
OUT3	6	O	Output signal 3
SAG1	4	I	Storage-area gate
SAG2	17	I	Storage-area gate
SRG1	14	I	Serial-register gate 1
SRG2	15	I	Serial-register gate 2
SRG3	16	I	Serial-register gate 3
SUB†	1		Substrate and clock return
SUB†	11		Substrate and clock return
SUB†	12		Substrate and clock return
SUB†	22		Substrate and clock return
TDB	21	I	Supply voltage for top-drain bias
TMG	18	I	Transfer-multiplex gate
TRG	13	I	Transfer gate

† All pins of the same name should be connected together externally (i.e., pin 2 to pin 20, pin 3 to pin 19, etc.).

detailed description

The TC271 consists of five basic functional blocks: (1) the image-sensing area, (2) the multiplexer block, (3) the image-storage area with dual-field memories, (4) the serial-register and transfer gates, and (5) the low-noise signal-processing amplifier block with charge-detection nodes. The location of each of these blocks is identified in the functional block diagram.

image-sensing area

Figure 4 and Figure 5 show cross sections with potential-well diagrams and top views of image-sensing elements. As light enters the silicon in the image-sensing area, free electrons are generated and collected in the potential wells of the sensing elements. During this time, blooming protection is activated by applying a burst of pulses to the antiblooming-gate inputs every horizontal-blanking interval. This prevents blooming caused by the spilling of charge from overexposed elements into neighboring elements. Thirty-four full columns and one half-column of elements at the right edge of the image-sensing area are shielded from incident light; these elements provide the dark reference used in subsequent video-processing circuits to restore the video-black level. There are also one full column and one half-column of light-shielded elements at the left edge of the image-sensing area and four lines of light-shielded elements at the bottom of the image area immediately above the multiplexer. The latter prevent charge leakage from the image area into the multiplexer.

multiplexer and image-storage area

After integration, the multiplexer rearranges two horizontal lines into vertical groups of three and separates and loads the image into the storage area. Figure 1 shows the layout of the multiplexer gate and its interface to the two field memories. Figure 2 shows the interface region between the storage area and the three serial registers. A drain is also provided to clear the image-sensing and image-storage areas of unwanted charge. Such charge can accumulate in the imager during the startup of operation or under special circumstances when nonstandard TV operation is desired. The sensor's independently addressable memories allow several different modes of sensor operation including (1) a normal-light mode, (2) a low-light mode, (3) a still mode, and (4) a progressive-scan mode. The timing for these four modes is given in Figure 6 through Figure 9. The parallel-transfer timing is shown in Figure 10.

serial registers and amplifiers

After transfer to the serial registers (see Figure 11, which shows the horizontal timing that gives the necessary sequence of pulses for transfer from the storage area to the serial registers), the charge is converted to a signal voltage at the sense node and buffered with a dual-stage source follower. The three serial registers are typically clocked 120 degrees out of phase with each serial-gate pulse supplying a detection-node reset signal for one of the other two serial gates (see Figure 12). The readout timing, which includes the three serial pulses and the pixel-clamp pulses used in an off-chip double-correlated sampling circuit, is shown in Figure 13. The detection nodes and amplifiers are located some distance from the edge of the storage area. Twelve dummy elements are incorporated at the end of each serial register to span the distance. The location of the dummy elements, which are considered to be part of the amplifiers, is shown in the functional block diagram. A schematic of the detection node and amplifier is given in Figure 3.

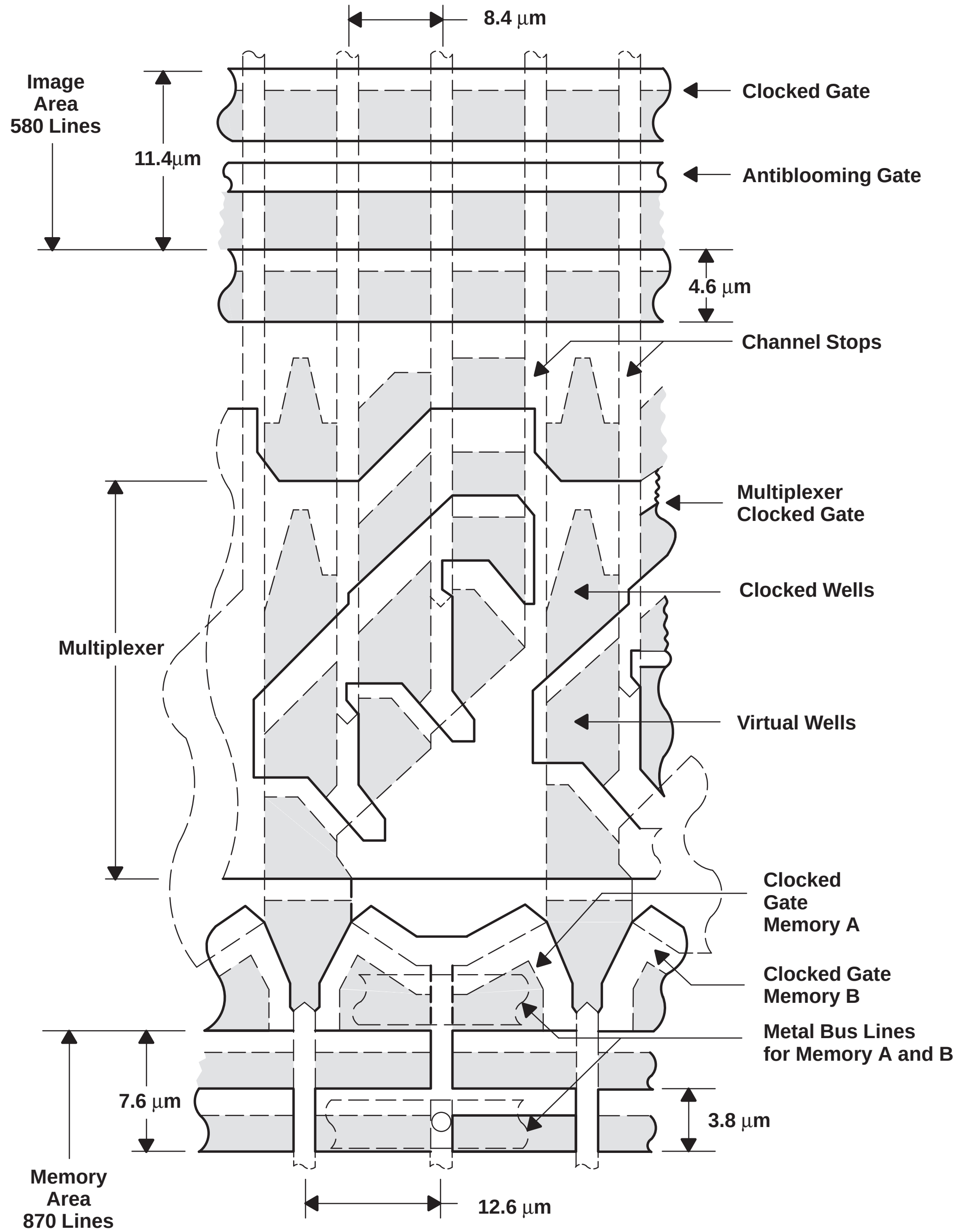


Figure 1. Layout of Multiplexing Gate

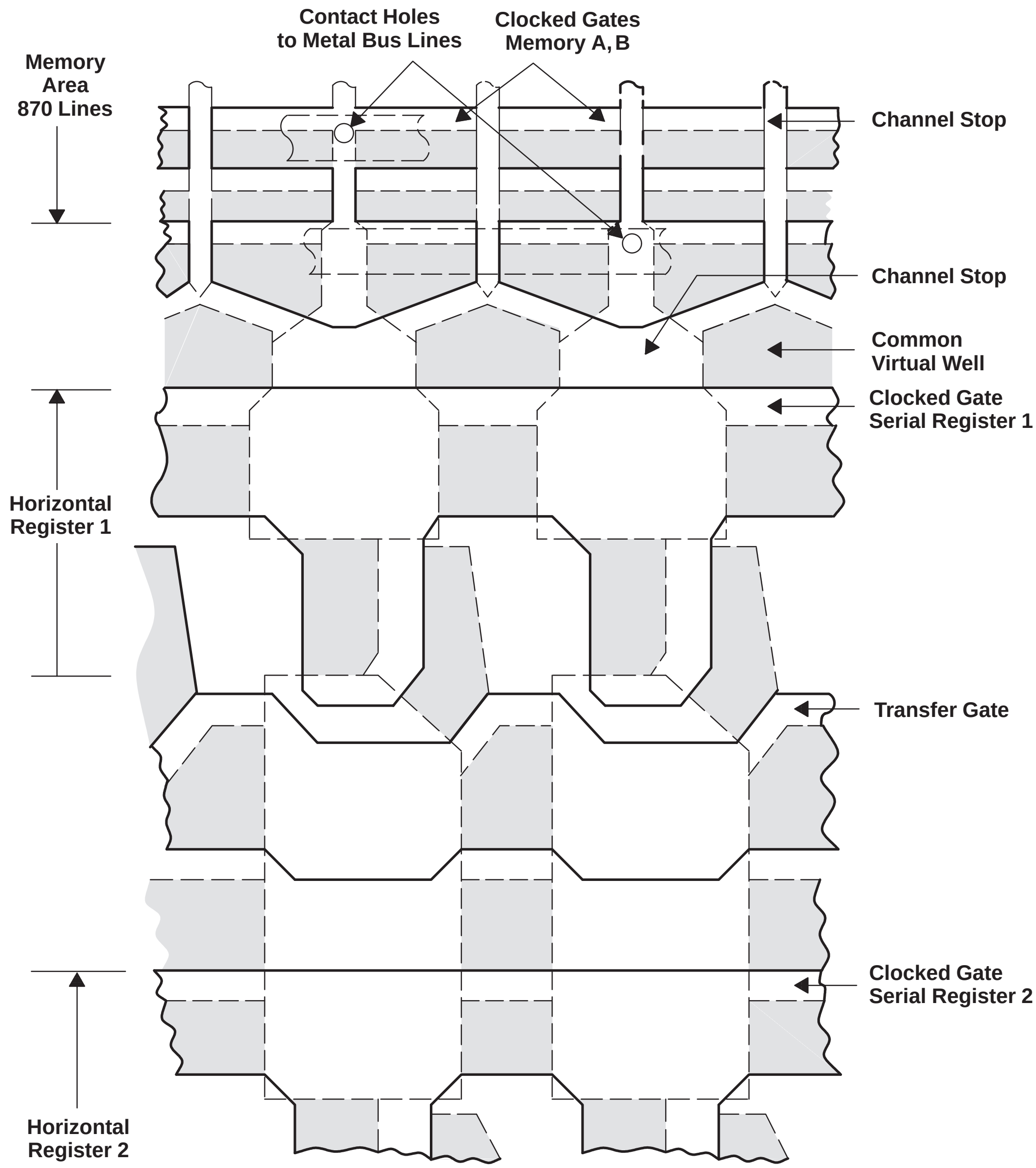


Figure 2. Layout of the Interface Region Between the Memories and the Serial Registers

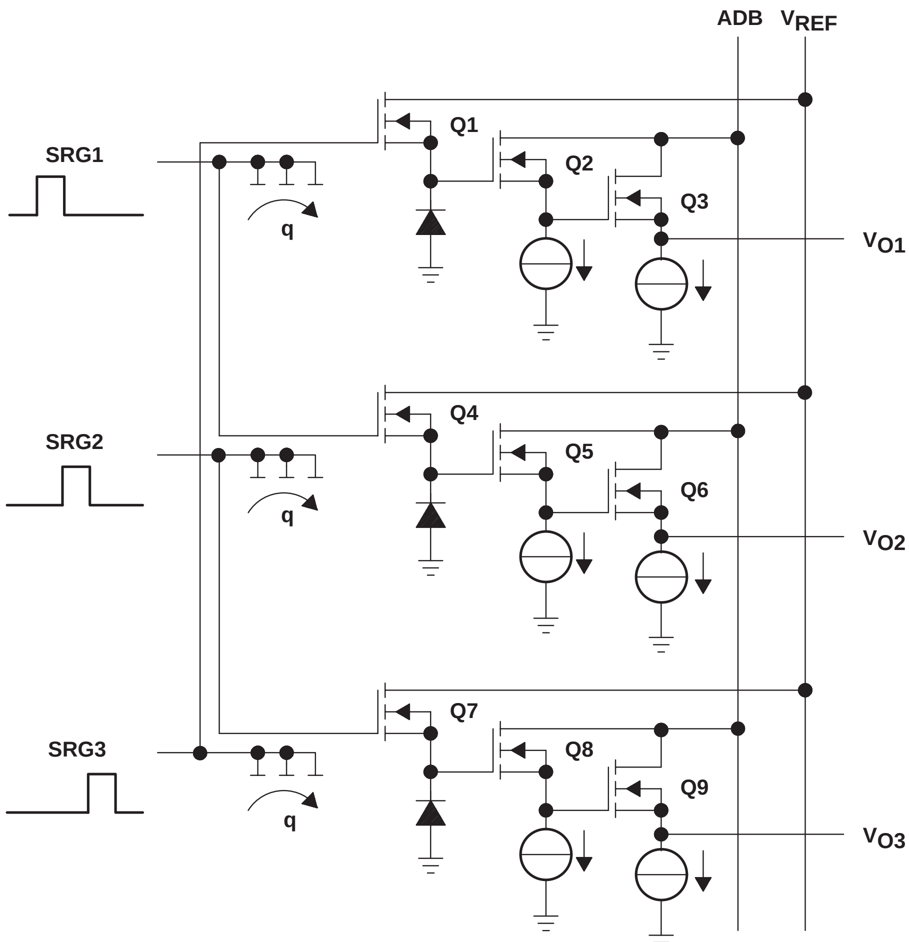


Figure 3. Circuit Diagram – Charge-Detection Amplifiers

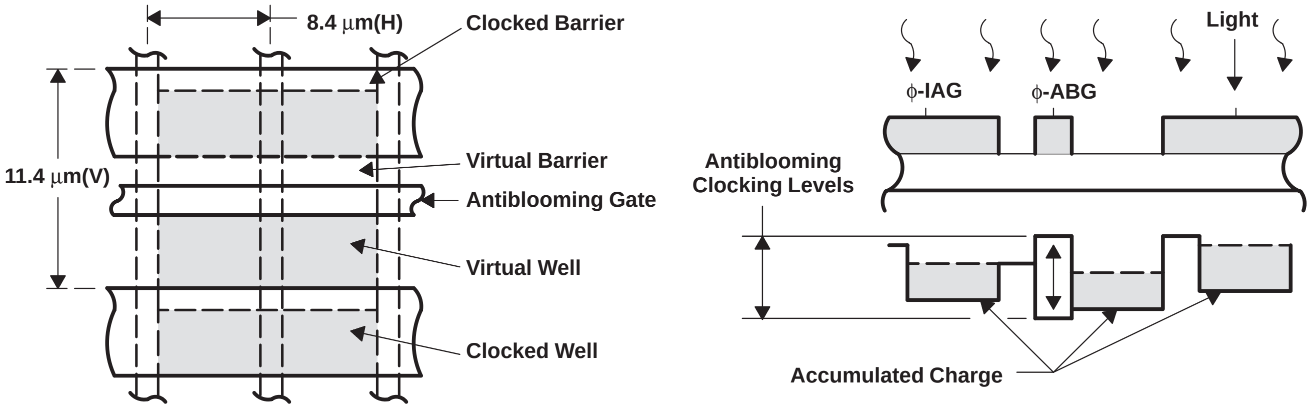


Figure 4. Charge-Accumulation Process

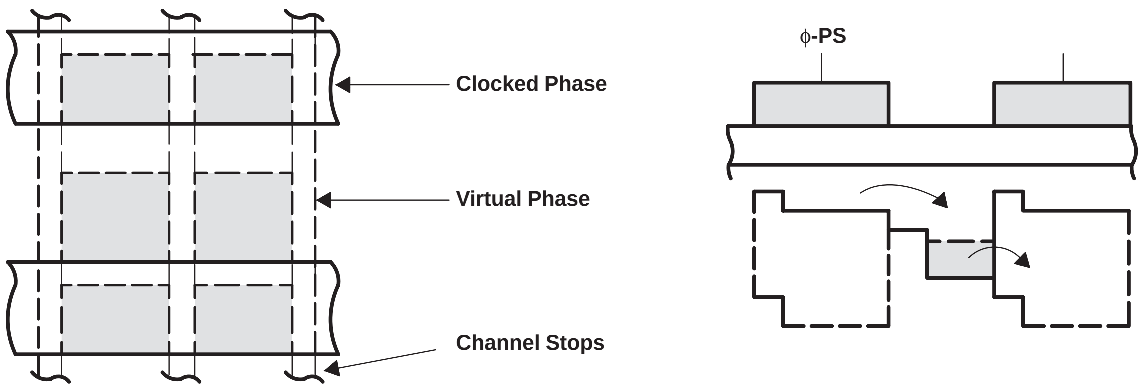


Figure 5. Charge-Transfer Process

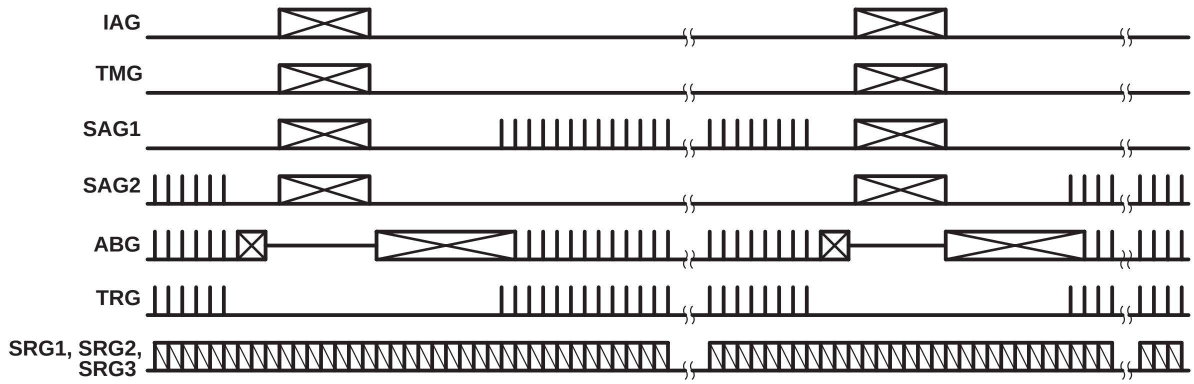


Figure 6. Vertical Timing, Normal-Light Mode

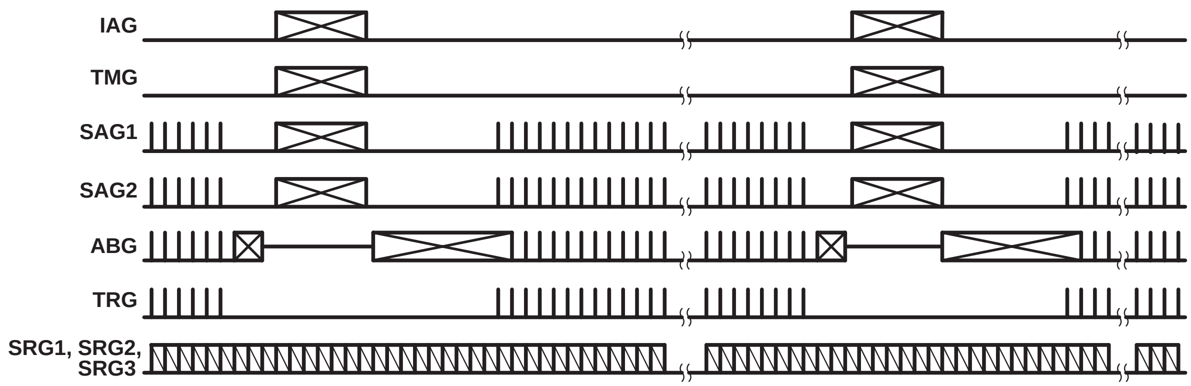


Figure 7. Vertical Timing, Low-Light Mode

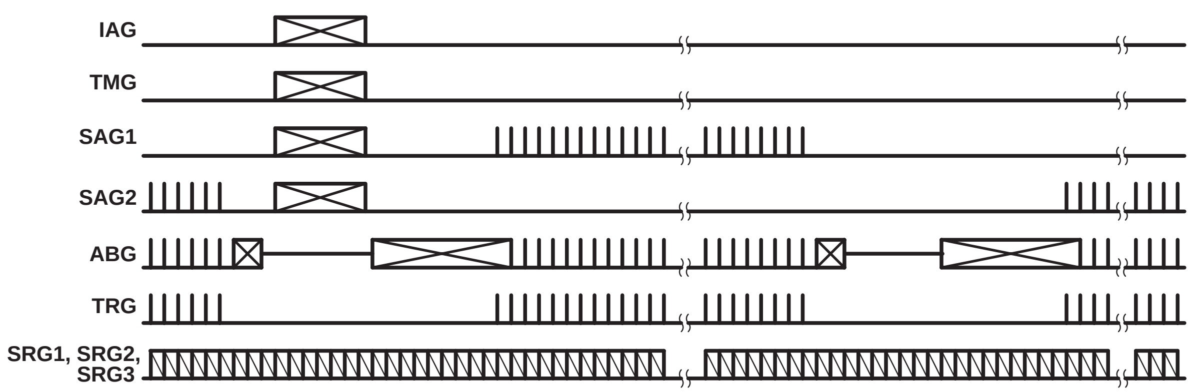


Figure 8. Vertical Timing, Still Mode

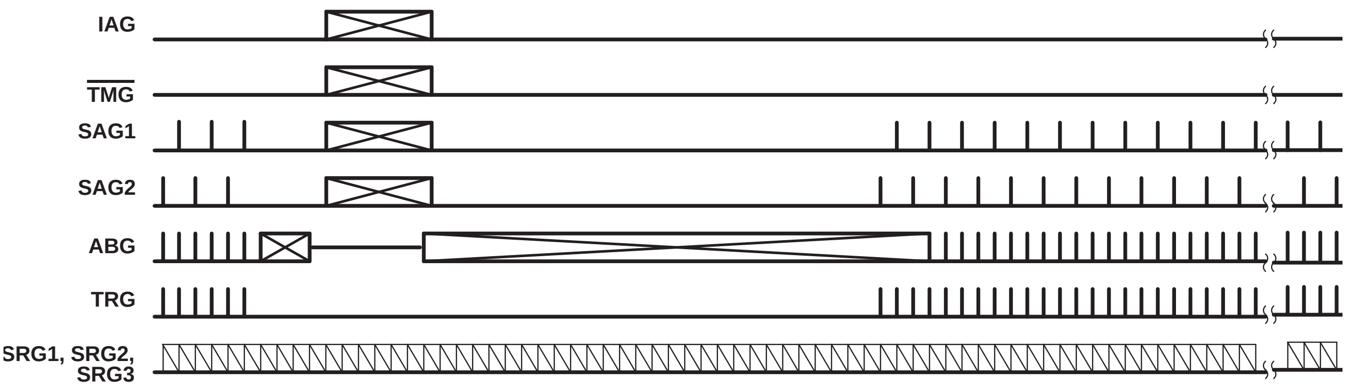


Figure 9. Vertical Timing, Progressive-Scan Mode

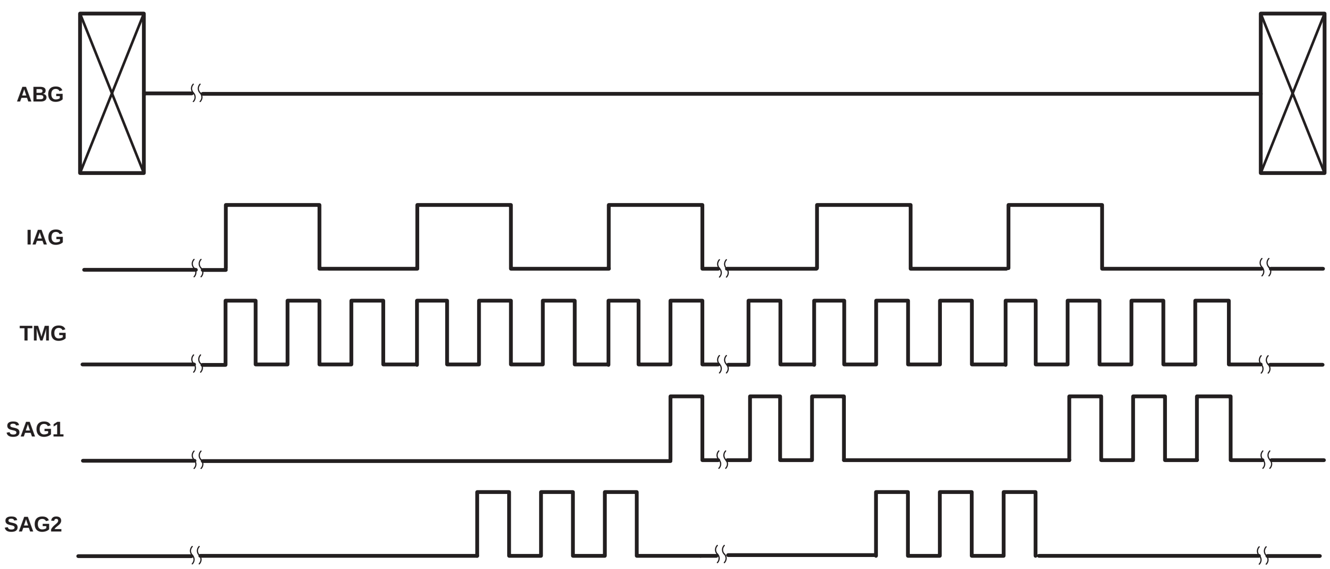
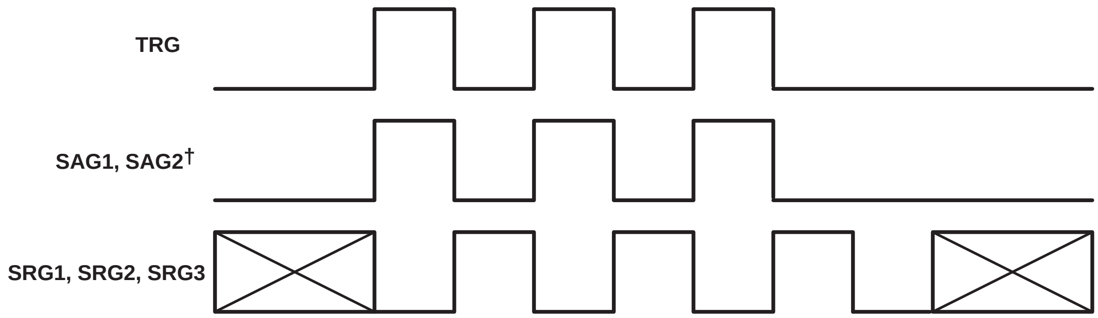


Figure 10. Parallel-Transfer Timing



† These clocks are mode-dependent.

Figure 11. Horizontal Timing

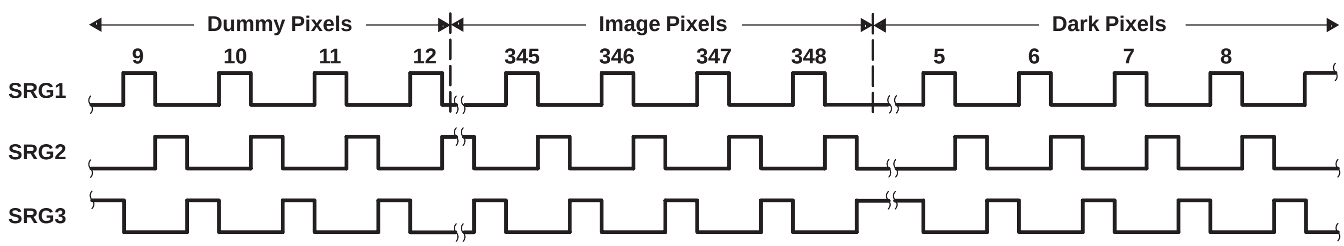
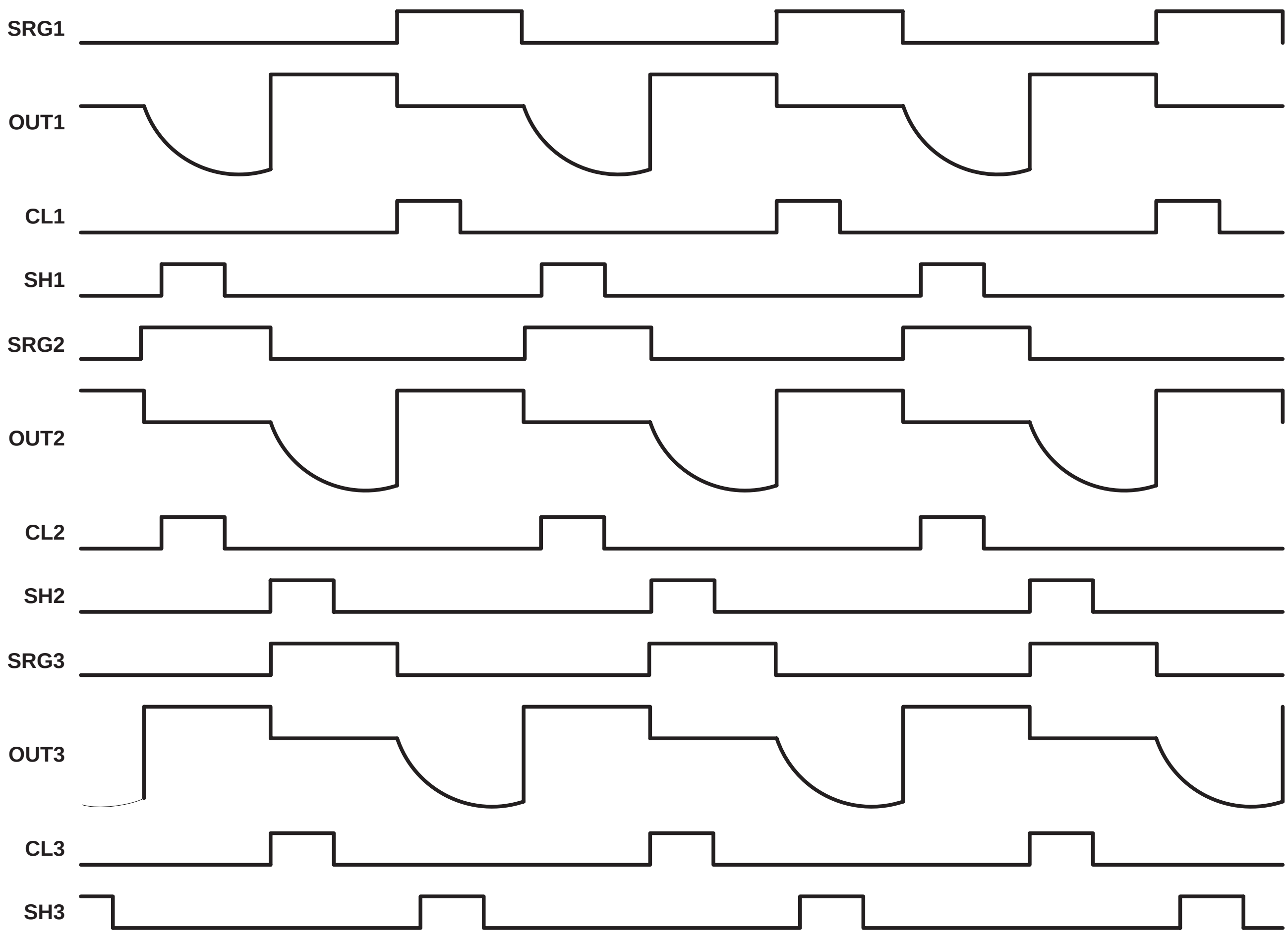


Figure 12. Start of Serial-Transfer Timing



NOTES: A. The video-processing (off-chip) pulses are defined as follows:

CL1 = Clamp pulse for video from OUT1
SH1 = Sample pulse for the sample-and-hold amplifier for video 1
CL2 = Clamp pulse for video from OUT2
SH2 = Sample pulse for the sample-and-hold amplifier for video 2
CL3 = Clamp pulse for video from OUT3
SH3 = Sample pulse for the sample-and-hold amplifier for video 3

B. The signals for channel (n+1) are phase shifted 120° from the signals for channel (n). For example, SRG2 is phase shifted 120° relative to SRG1, SRG3 is phase shifted 120° relative to SRG2, OUT2 is phase shifted 120° relative to OUT1, OUT3 is phase shifted 120° relative to OUT2, and so forth.

Figure 13. Video-Process Timing

spurious-nonuniformity specification

The spurious-nonuniformity specification of the TC271 CCD grades –30 and –40 is based on several sensor characteristics:

- Amplitude of the nonuniform pixel
- Polarity of the nonuniform pixel
  - Black
  - White
- Column amplitude

The CCD sensors are characterized in both an illuminated condition and a dark condition. In the dark condition, the nonuniformity is specified in terms of absolute amplitude as shown in Figure 14. In the illuminated condition, the nonuniformity is specified as a percentage of the total illumination as shown in Figure 15.

The nonuniformity specification for the TC271 is as follows (CCD video-output signal is 50 mV ±10 mV):

PART NUMBER	PIXEL NONUNIFORMITY		COLUMN NONUNIFORMITY
	DARK CONDITION	ILLUMINATED CONDITION	COLUMN AMPLITUDE, x (mV)
	PIXEL AMPLITUDE, x (mV)	% OF TOTAL ILLUMINATION	
TC271-30	x ≤ 12 mV	x ≤ 10	x < 0.5 mV
TC271-40	x ≤ 15 mV	x ≤ 15	x ≤ 1 mV

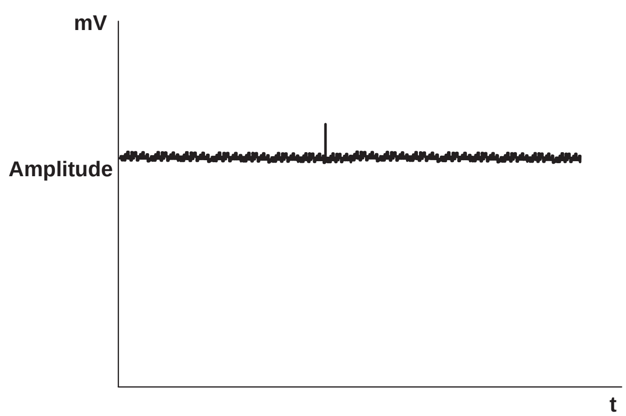


Figure 14. Pixel Nonuniformity, Dark Condition

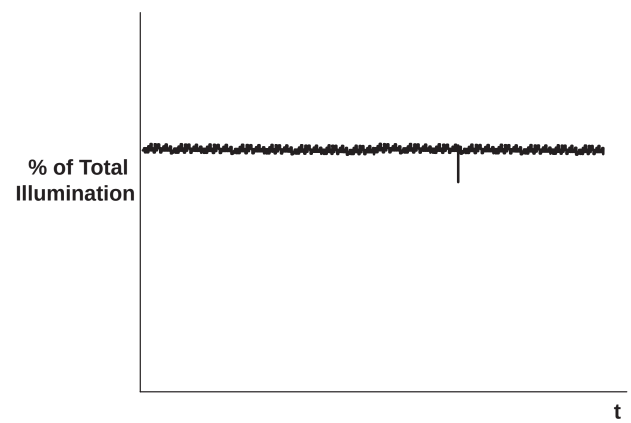


Figure 15. Pixel Nonuniformity, Illuminated Condition

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: ADB, CDB, TDB (see Note 1) . . . . 0 V to 15 V
Input voltage range, V_I: ABG, IAG, SAG1, SAG2, SRG1, SRG2, SRG3, TRG . . . . –15 V to 15 V
Operating free-air temperature range, T_A . . . . –10°C to 40°C
Storage temperature range, T_{STG} . . . . –30°C to 85°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the substrate terminal.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	ADB, CDB, TDB		11	12	13	V
Substrate bias voltage				0		V
Input voltage, V_I‡	IAG	High level	2	2.5	3	V
		Low level	–11		–9	
	SAG1, SAG2	High level	2	2.5	3	
		Low level	–11		–9	
	SRG1, SRG2, SRG3	High level	2	2.5	3	
		Low level	–11		–9	
	TMG	High level	2	2.5	3	
		Low level	–11		–9	
	ABG	High level	4	4.5	5	
		Intermediate level§	–2.85	–2	–1.55	
		Low level	–7.5	–7	–6.5	
	TRG	High level	2	2.5	3	
		Low level	–11		–9	
Clock frequency, f_{clock}	ABG			0.625		MHz
	IAG			1.11		
	SAG1, SAG2, TMG			6.67		
	SRG1, SRG2, SRG3			6.67		
	TRG			1.67		
Load capacitance	OUT1, OUT2, OUT3				8	pF
Operating free-air temperature, T_A			–10		40	°C

‡ The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for clock voltage levels.
§ Adjustment is required for optimal performance.

electrical characteristics over recommended operating ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP†	MAX	UNIT
Dynamic range (see Note 2)			60		dB
Charge-conversion factor			6.5		μV/e
Charge-transfer efficiency (see Note 3)		0.9999	0.99995	1.000	
Signal-response delay time, τ (see Note 4 and Figure 19)		18	20	22	ns
Gamma (see Note 5)		0.89	0.94	0.99	
Output resistance			350		Ω
Noise voltage	1/f noise (5 kHz)		0.1		μV/√Hz
	Random noise (f = 100 kHz)		0.08		
Noise-equivalent signal			15		electrons
Rejection ratio at 4.77 MHz	ADB (see Note 6)		20		dB
	SRGn (see Note 7)		40		
	ABG (see Note 8)		30		
Supply current			4		mA
Input capacitance, C_i	IAG		12000		pF
	SAG1, SAG2		11000		
	ABG		4600		
	TMG		120		
	TRG		160		
	SRG1, SRG2, SRG3		80		

† All typical values are at T_A = 25 °C.

NOTES: 2. Dynamic range is –20 times the logarithm of the mean-noise signal divided by the saturation-output signal.
3. Charge-transfer efficiency is one minus the charge loss per transfer in the output register. The test is performed in the dark using an electrical-input signal.
4. Signal-response delay time is the time between the falling edge of the SRG clock pulse and the output-signal valid state.
5. Gamma (γ) is the value of the exponent in the equation below for two points on the linear portion of the transfer-function curve:

$$\left(\frac{\text{Exposure (2)}}{\text{Exposure (1)}}\right)^{\gamma} = \left(\frac{\text{Output signal (2)}}{\text{Output signal (1)}}\right)$$

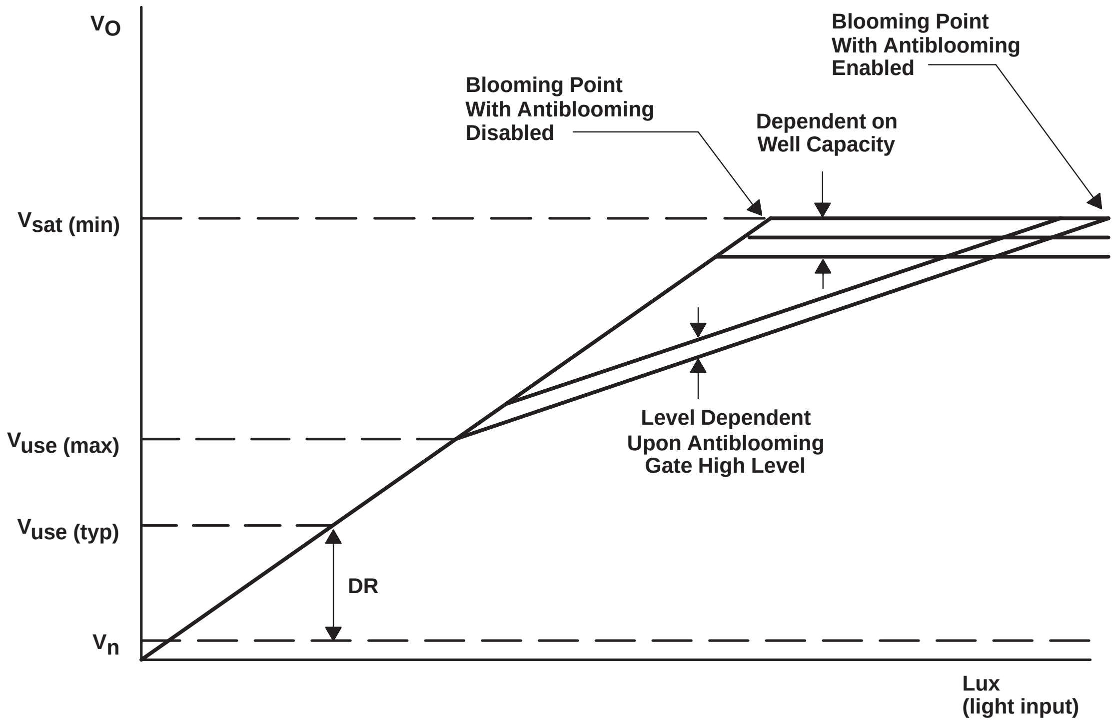
6. ADB rejection ratio is –20 times the logarithm of the ac amplitude on OUTn divided by the ac amplitude on ADB.
7. SRGn rejection ratio is –20 times the logarithm of the ac amplitude on OUTn divided by the ac amplitude on SRGn.
8. ABG rejection ratio is –20 times the logarithm of the ac amplitude on OUTn divided by the ac amplitude on ABG.

optical characteristics, T_A = 25°C, exposure time = 40 ms (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Sensitivity (see Notes 9 and 10)		No IR filter		400		mV/lx
		With IR filter		52		
Saturation signal, V_{sat} (see Note 11)				410		mV
Image-area well capacity				70 x 10^3		electrons
Blooming-overload ratio (see Note 12)	Exposure time = 1/50 second			125		
Smear (see Notes 13 and 14)					0.0014	
Output-signal uniformity	V_O = 1/2 V_U (see Note 10)				1	mV
Dark-signal (see Note 15)		T_A = 40°C		5	6	mV
Dark-signal uniformity		T_A = 40°C			0.3	mV
Dark current		T_A = 21°C		100		pA/cm^2

NOTES: 9. Sensitivity is measured at any illumination level that gives an output voltage level less than V_U. A CM-500 filter is used.
10. V_U is the output voltage that represents the threshold of operation of antiblooming. $V_U \approx$ 1/2 saturation signal.
11. Saturation is the condition in which further increase in exposure does not lead to further increase in output signal.
12. Blooming is the condition in which charge is induced in an element by light incident on another element. Blooming-overload ratio is the ratio of blooming exposure to saturation exposure.
13. Smear is the measure of error induced by transferring charge through an illuminated pixel in shutterless operation. It is equivalent to the ratio of the single-pixel transfer time during a fast dump to the exposure time using an illuminated section that is 1/10 of the image-area vertical height with recommended clock frequencies.
14. The fast-dump clocking rate during vertical timing is 1.0 MHz, and the illuminated section is 1/10 of the height of the image section.
15. Dark-signal level is measured from the dark dummy pixels.

PARAMETER MEASUREMENT INFORMATION



$$\text{DR (dynamic range)} = \frac{\text{camera white-clip voltage}}{V_n}$$

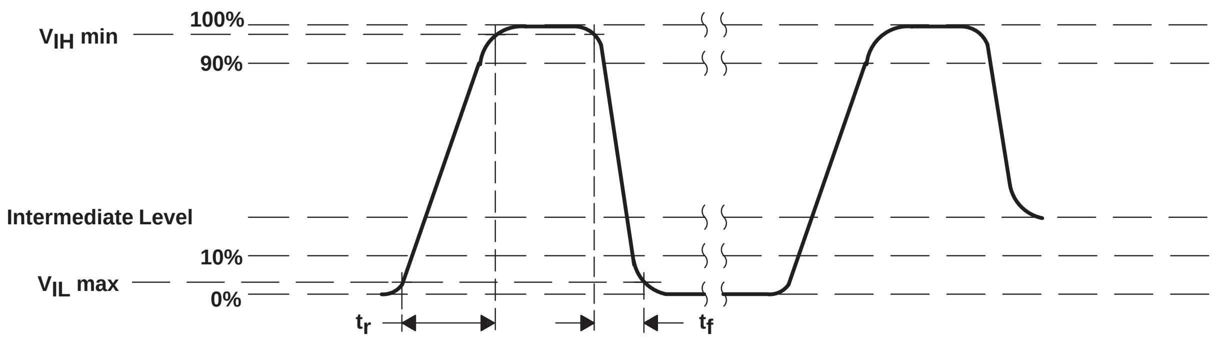
V_n = noise-floor voltage
$V_{sat\ (min)}$ = minimum saturation voltage
$V_{use\ (max)}$ = maximum usable voltage
$V_{use\ (typ)}$ = typical user voltage (camera white clip)

NOTES: A. $V_{use\ (typ)}$ is defined as the voltage determined to equal the camera white clip. This voltage must be less than $V_{use\ (max)}$.

B. A system trade-off is necessary to determine the system light sensitivity versus the signal/noise ratio. By lowering the $V_{use\ (typ)}$, the light sensitivity of the camera is increased; however, this sacrifices the signal/noise ratio of the camera.

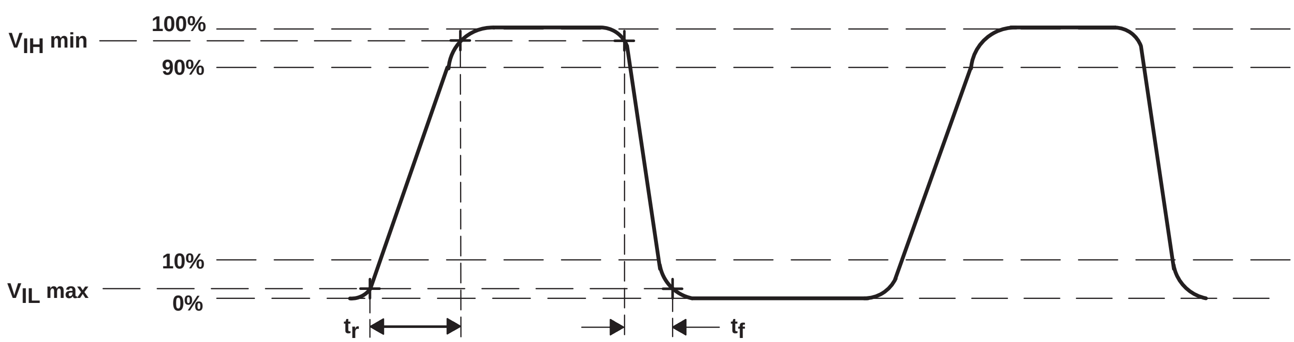
Figure 16. Typical V_{sat}, V_{use} Relationship

PARAMETER MEASUREMENT INFORMATION



Slew rate between 10% and 90% = 70 to 120 V/μs, t_r = 150 ns, t_f = 90 ns

Figure 17. Typical Clock Waveform for ABG, IAG, SAG1, SAG2, AND TMG



Slew rate between 10% and 90% = 300 V/μs, t_r = t_f = 15 ns

Figure 18. Typical Clock Waveform for SRG1, SRG2, SRG3, and TRG

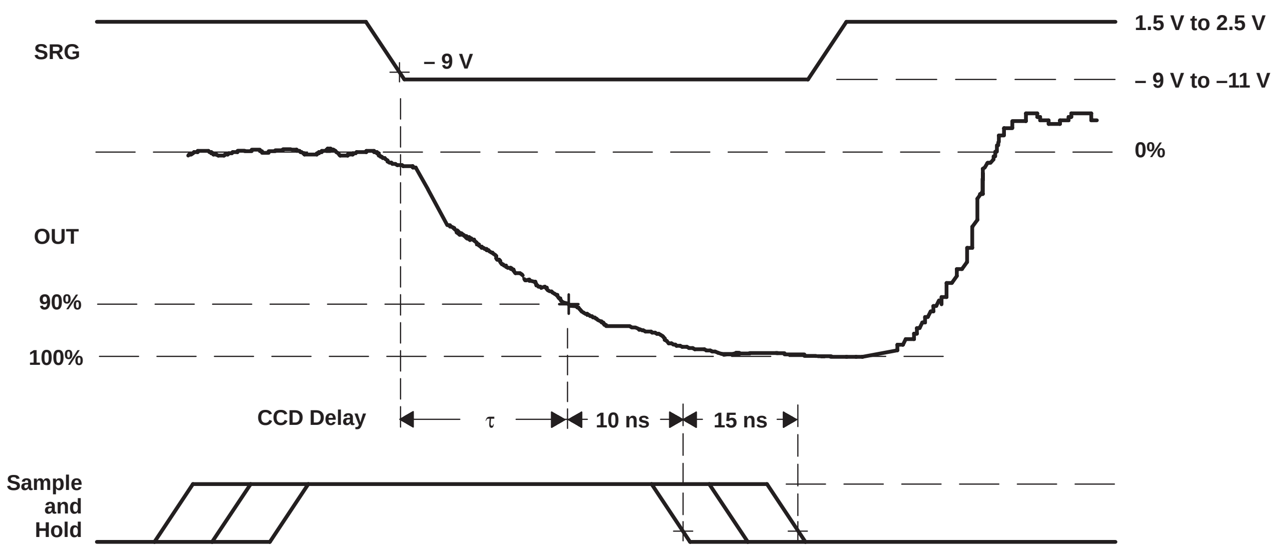
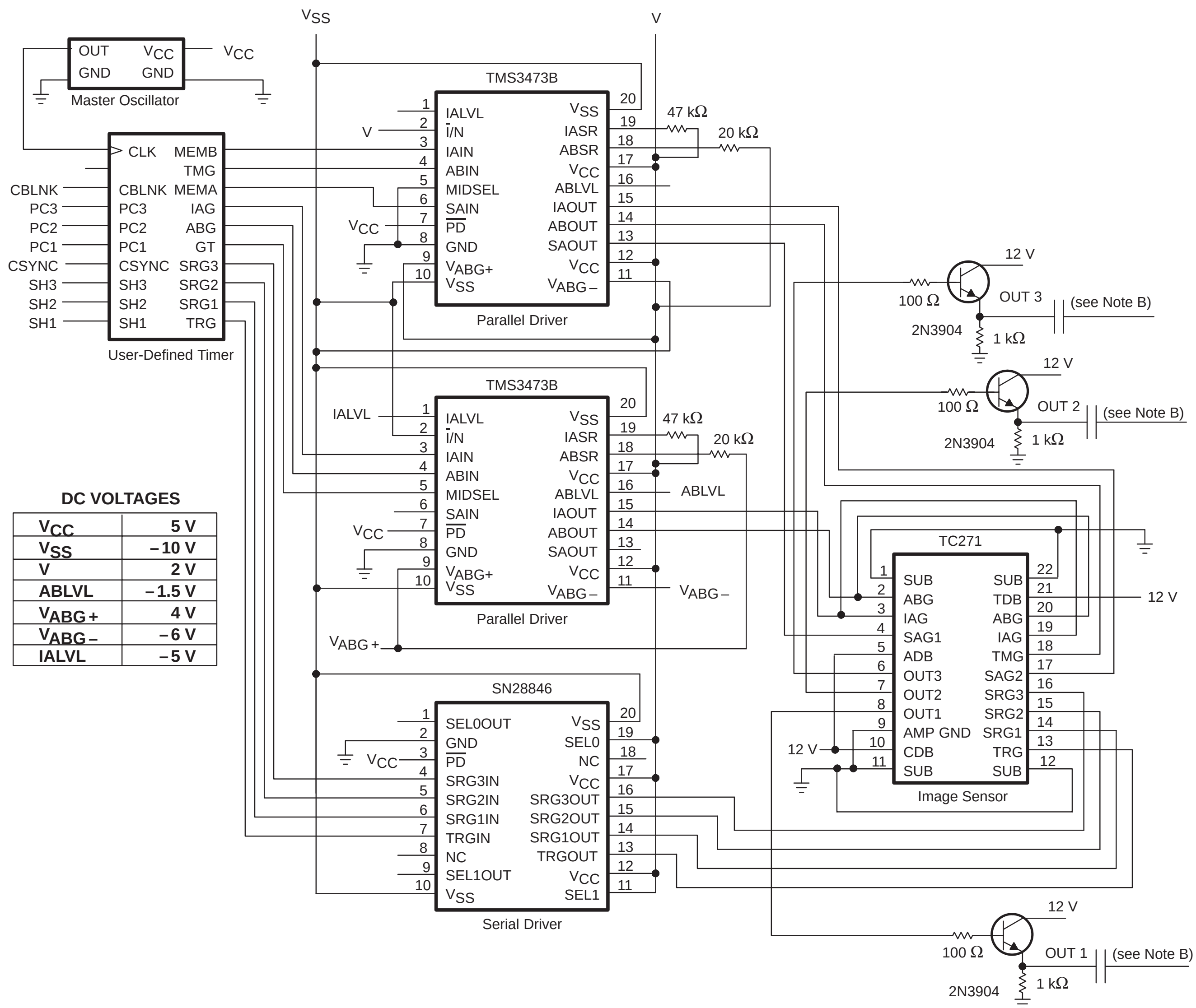


Figure 19. SRG and OUT Waveforms

APPLICATION INFORMATION



DC VOLTAGES

V_{CC}	5 V
V_{SS}	–10 V
V	2 V
ABLVL	–1.5 V
V_{ABG+}	4 V
$V_{ABG–}$	–6 V
IALVL	–5 V

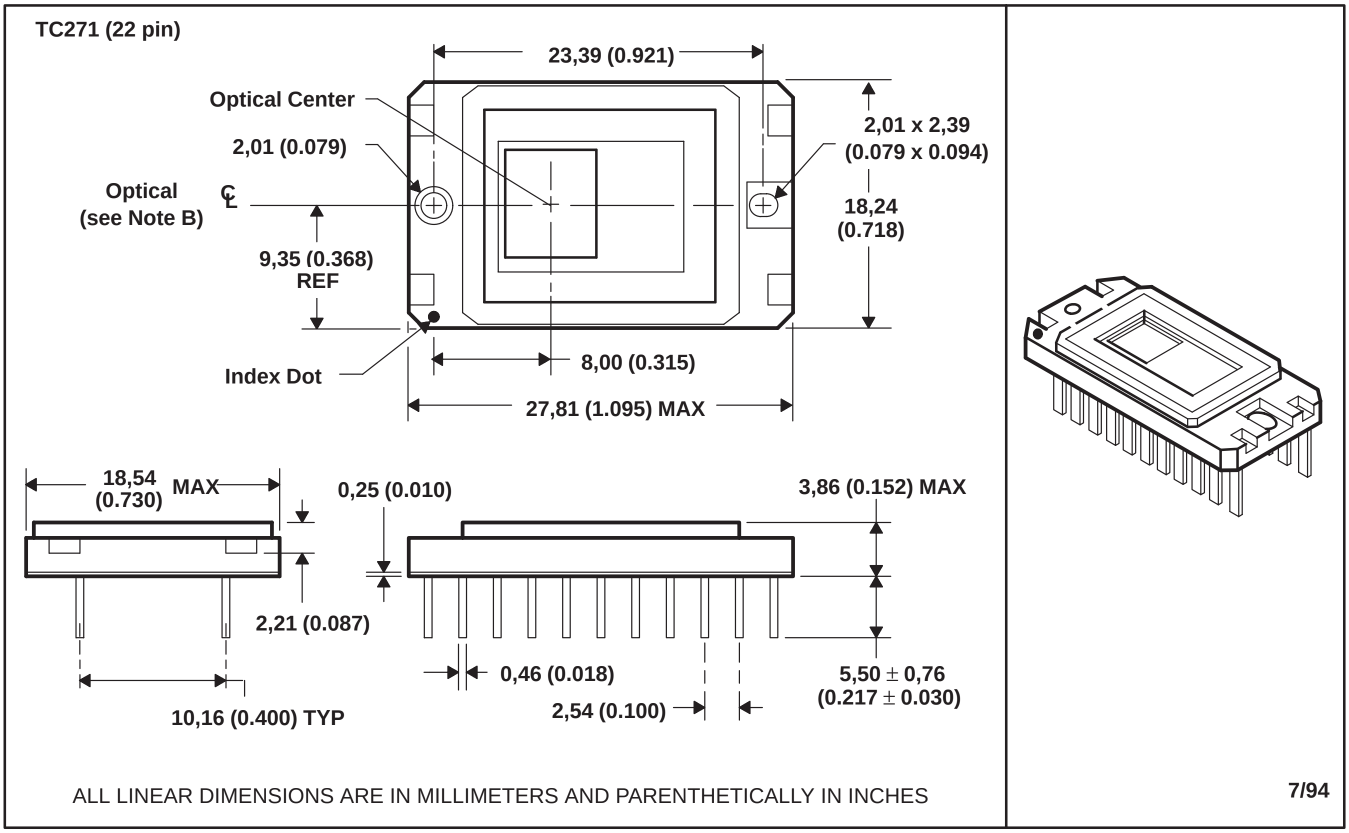
SUPPORT CIRCUITS			
DEVICE	**PACKAGE**	**APPLICATION**	**FUNCTION**
SN28846DW	20 pin small outline	Serial driver	Driver for SRG1, SRG2, SRG3, and TRG
TMS3473BDW	20 pin small outline	Parallel driver	Driver for IAG, SAG1, SAG2, ABG, and TMG

Figure 20. Typical Application Circuit Diagram

NOTES: A. Decoupling capacitors are not shown.
B. TI recommends designing AC coupled systems.

MECHANICAL DATA

The package for the TC271 consists of a ceramic base, a glass window, and a 22-lead frame. The package leads are configured in a dual in-line organization and fit into mounting holes with 2.54 mm (0.10 in) center-to-center spacings. The glass window is sealed to the package by an epoxy adhesive. It can be cleaned by any standard procedure for cleaning optical assemblies or by wiping the surface with a cotton swab moistened with alcohol.



NOTES:
- A. Single dimensions are nominal.
- B. The center of the package and the center of the image area are not coincident.
- C. The distance from the top of the glass to the image-sensor surface is typically 1,46 mm (0.057 in). The glass is 0,95 ±0,08 mm and has an index of refraction of 1.53.
- D. Each pin centerline is located within 0,25 mm (0.010 in) of its true longitudinal position.

IMPORTANT NOTICE