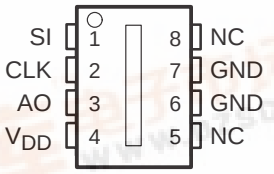
TSL1301
102 × 1 LINEAR SENSOR ARRAY WITH HOLD

SOES031A – NOVEMBER 1996 – REVISED MAY 1997

- 102 × 1 Sensor-Element Organization
- 300 Dots-Per-Inch (DPI) Sensor Pitch
- High Sensitivity
- Output Referenced to Ground
- Excellent High-Temperature Dark Signal Characteristics
- Operation to 2 MHz
- Single 5-V Supply

(TOP VIEW)



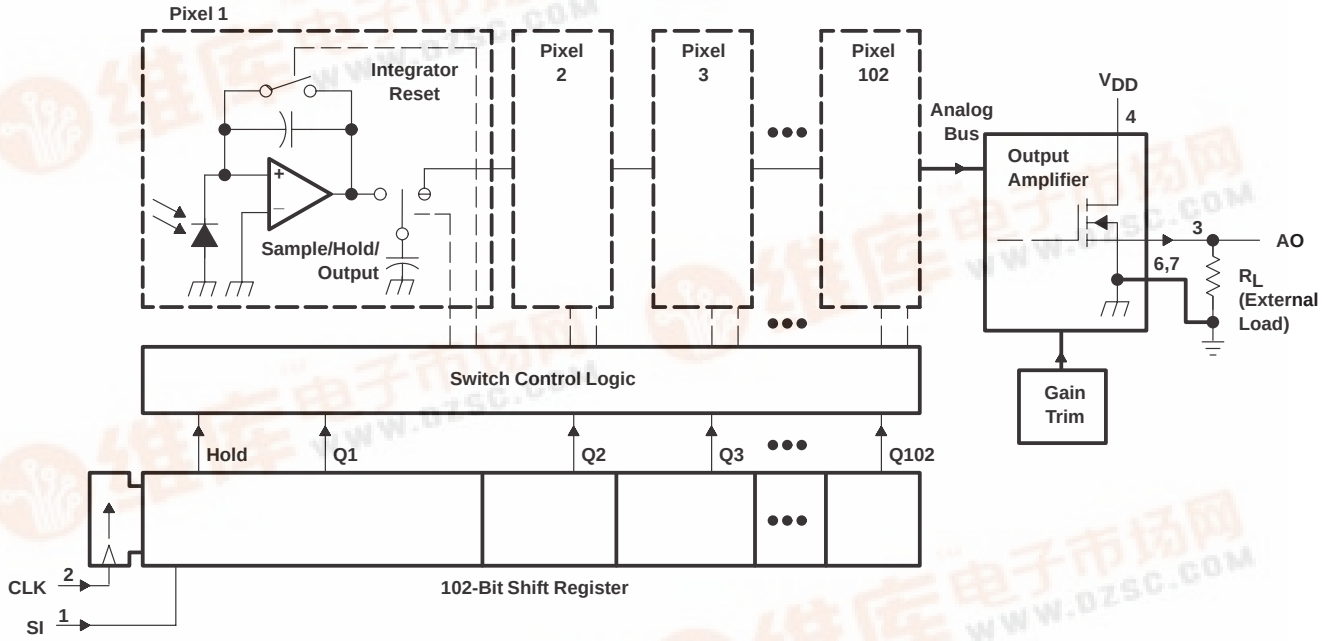
NC – No internal connection

description

The TSL1301 linear sensor array consists of a 102 × 1 array of photodiodes, associated charge amplifier circuitry, and a pixel data-hold function that provides simultaneous-integration start and stop times for all pixels. The pixels measure 85 µm by 77 µm with 85-µm center-to-center spacing and 8-µm spacing between pixels. Operation is simplified by internal control logic that requires only a serial-input pulse (SI) and a clock.

The TSL1301 is intended for use in a wide variety of applications including mark and code reading, OCR and contact imaging, edge detection and positioning, and optical encoding.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AO	3	Analog output
CLK	2	Clock. The clock controls charge transfer, pixel output, and reset.
GND	6, 7	Ground (substrate). All voltages are referenced to the substrate.
NC	5, 8	No internal connection
SI	1	Serial input. SI defines the start of the data-out sequence.
V_{DD}	4	Supply voltage. Supply voltage for both analog and digital circuits.

detailed description

The sensor consists of 102 photodiodes, also called pixels, arranged in a linear array. Light energy impinging on a pixel generates photocurrent, which is then integrated by the active integration circuitry associated with that pixel.

During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity and the integration time.

The output and reset of the integrators is controlled by a 102-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI. This causes all 102 sampling capacitors to be disconnected from their respective integrators and starts an integrator reset period. As the SI pulse is clocked through the shift register, the charge stored on the sampling capacitors is sequentially connected to a charge-coupled output amplifier that generates a voltage on analog output AO. The integrator reset period ends 18 clock cycles after the SI pulse is clocked in. Then the next integration period begins. Note that a total 103 clock cycles are required, the 103rd cycle being necessary to terminate the output of pixel 102 and return the output to a high-impedance state, and to clear the internal shift register.

AO is driven by a source follower that requires an external pulldown resistor. When the output is not in the output phase, it is in a high-impedance state. The output is nominally 0 V for no light input and 2 V for a nominal full-scale output.

absolute maximum ratings†

Supply voltage, V_{DD} . . . . . 7 V
Digital input current range, I_I . . . . . –20 mA to 20 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Figure 1 and Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	$V_{DD} \times 0.7$		V_{DD}	V
Low-level input voltage, V_{IL}	0		$V_{DD} \times 0.3$	V
Wavelength of light source, λ	400		700	nm
Clock frequency, f_{clock}	5		2000	kHz
Sensor integration time, t_{int}	0.0515	5	100	ms
Setup time, serial input, $t_{su(SI)}$	20			ns
Hold time, serial input, $t_{h(SI)}$ (see Note 1)	0			ns
Operating free-air temperature, T_A	0		70	°C

NOTE 1: SI must go low before the rising edge of the next clock pulse.

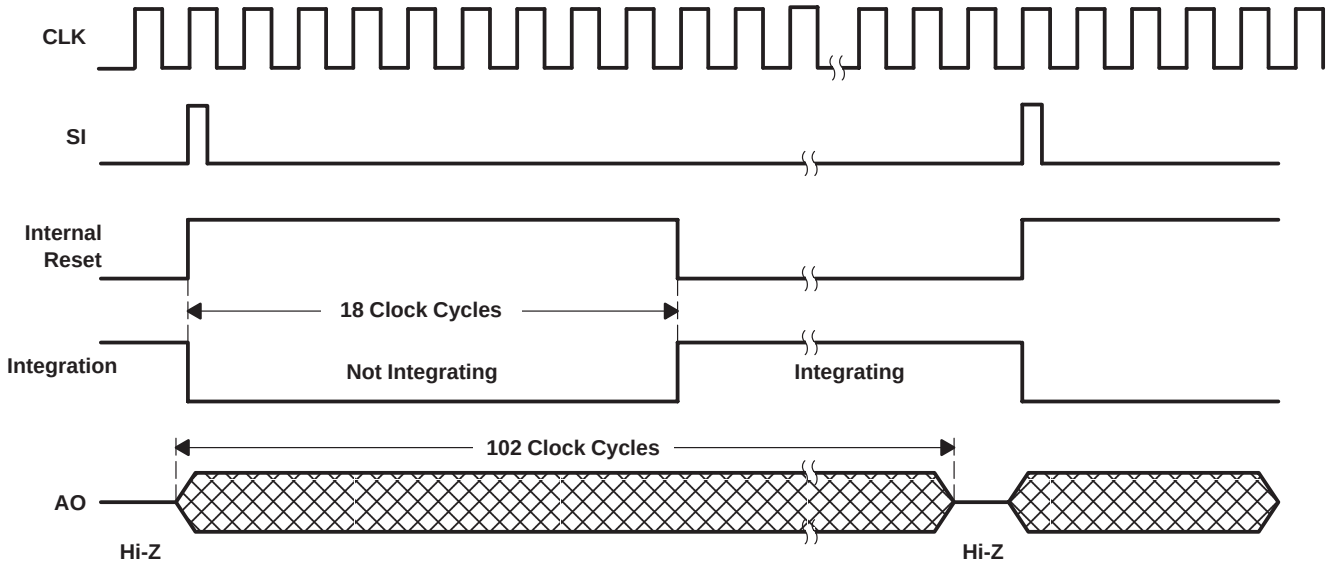


Figure 1. Timing Waveforms

electrical characteristics at f_{clock} = 200 kHz, V_{DD} = 5 V, T_A = 25°C, λ_p = 565 nm, t_{int} = 5 ms, R_L = 330 Ω, E_e = 800 nW/cm^2 (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Analog output voltage (white, average over 102 pixels)			1.8	2	2.2	V
	Analog output voltage (dark, average over 102 pixels)	E_e = 0		0	0.3	0.4	V
PRNU	Pixel response nonuniformity	Pixels 2–101,	See Note 3			±10%	
	Nonlinearity of analog output voltage	See Note 4			±0.5%		
	Output noise voltage	E_e = 0,	See Note 5		3		mVrms
	Saturation exposure	V_{DD} = 4.5 V		5.45	7		nJ/cm^2
	Analog output saturation voltage	V_{DD} = 4.5 V,	R_L = 330 Ω	3	3.5		V
DSNU	Dark signal nonuniformity	All pixels, See Note 6	E_e = 0		0.04	0.12	V
IL	Image lag	See Note 7			1%		
I_{DD}	Supply current	R_L = 330 Ω			2.5	4	mA
I_{IH}	High-level input current	$V_I = V_{DD}$				10	µA
I_{IL}	Low-level input current	V_I = 0				10	µA
C_i	Input capacitance				5		pF

NOTES: 2. Clock duty cycle is assumed to be 50%.
3. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated.
4. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
5. RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
6. DNSU is the difference between the maximum and minimum of dark-current voltage.
7. Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$IL = \frac{V_{AO} - V_{AO(dark)}}{V_{AO(white)} - V_{AO(dark)}} \times 100$$

operating characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{w(H)}$	Clock pulse duration (high)		50			ns
$t_{w(L)}$	Clock pulse duration (low)		50			ns
t_s	Analog output settling time to ±1%	R_L = 330 Ω, C_L = 50 pF		350		ns

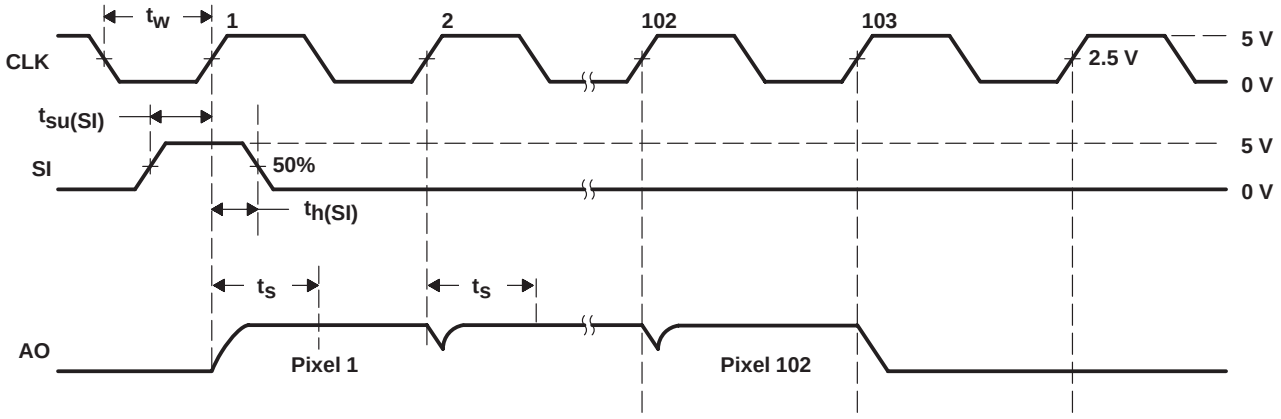


Figure 2. Operational Waveforms

APPLICATIONS INFORMATION

This clear-plastic dual-in-line package consists of a circuit mounted on a lead frame and encapsulated with an electrically nonconductive clear plastic compound.

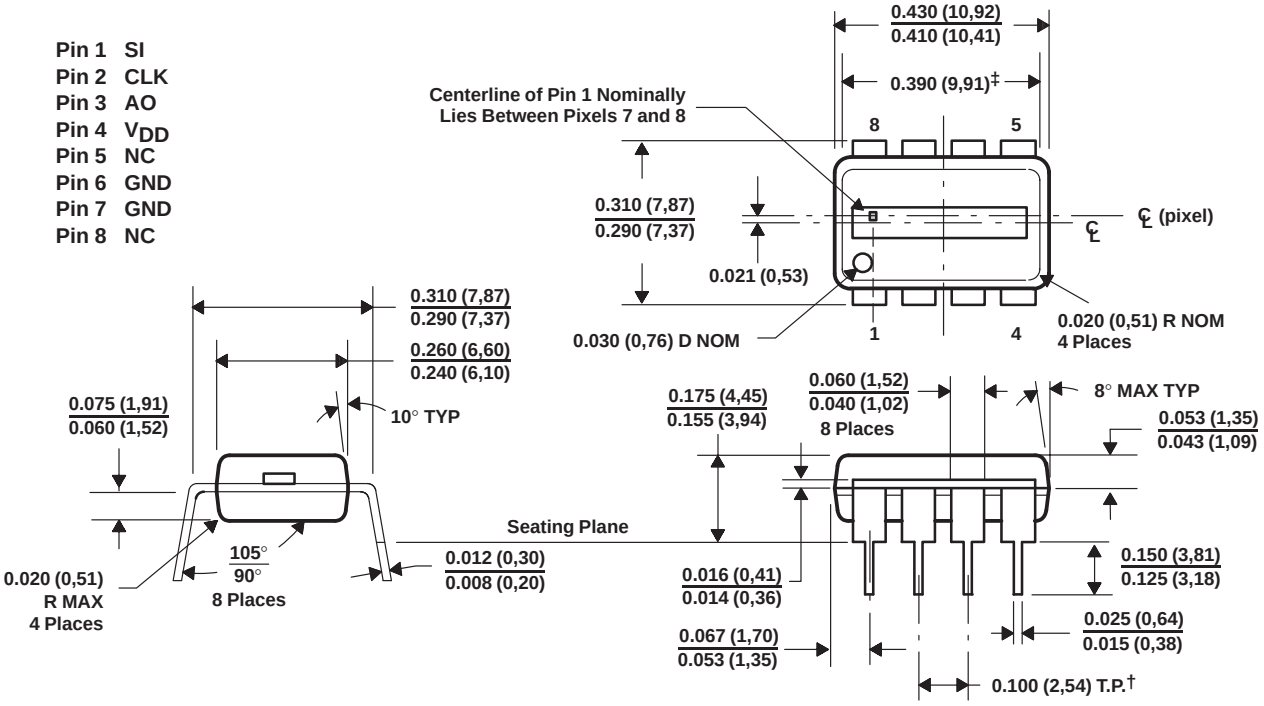


Figure 3. Packaging Configuration

† True position when unit is installed
‡ Minimum flat-optical-surface length
NOTES: A. All linear dimensions are in inches and parenthetically in millimeters.
B. This drawing is subject to change without notice.

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