

## MOS FIELD EFFECT TRANSISTOR

# 2SK3356

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### DESCRIPTION

The 2SK3356 is N-channel MOS Field Effect Transistor designed for high current switching applications.

#### FEATURES

- Super low on-state resistance:
- ★  $R_{DS(on)1} = 8.0 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, \text{ ID} = 38 \text{ A})$
- ★  $R_{DS(on)2} = 12 \text{ m}\Omega \text{ MAX.} (V_{GS} = 4 \text{ V}, \text{ ID} = 38 \text{ A})$
- ★ Low Ciss: Ciss = 6300 pF TYP.
  - Built-in gate protection diode

#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

		• •		
	Drain to Source Voltage	VDSS	60	V
	Gate to Source Voltage	VGSS(AC)	±20	V
	Drain Current (DC)	D(DC)	±75	А
	Drain Current (pulse) Note1	D(pulse)	±300	А
$\star$	Total Power Dissipation (Tc = $25^{\circ}$ C)	Рт	130	W
	Total Power Dissipation ( $T_A = 25^{\circ}C$ )	Рт	3.0	W
	Channel Temperature	Tch	150	°C
	Storage Temperature	Tstg	–55 to +150	°C
$\star$	Single Avalanche Current Note2	las	55	А
$\star$	Single Avalanche Energy Note2	Eas	302	mJ
		- <i>i</i>		

Notes 1.  $PW \leq$  10  $\mu s,$  Duty cycle  $\leq$  1 %

★ 2. Starting Tch = 25 °C, RG = 25  $\Omega$ , VGS = 20 V  $\rightarrow$  0 V

THERMAL RESISTANCE			
Channel to Case	Rth(ch-C)	0.93	°C/W
Channel to Ambient	Rth(ch-A)	41.7	°C/W

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#### **ORDERING INFORMATION**

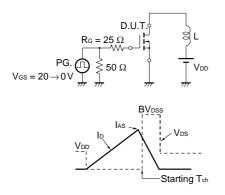
PART NUMBER	PACKAGE		
2SK3356	TO-3P		

#### \* ELECTRICAL CHARACTERISTICS (TA = 25 °C)

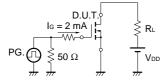
NEC

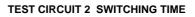
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	$V_{GS} = 10 V, I_D = 38 A$		6.3	8.0	mΩ
	RDS(on)2	Vgs = 4 V, Id = 38 A		8.0	12	mΩ
Gate to Source Cut-off Voltage	VGS(off)	$V_{DS} = 10 V, I_{D} = 1 mA$	1.5	2.0	2.5	V
Forward Transfer Admittance	yfs	$V_{DS} = 10 V, I_{D} = 38 A$	35	57		S
Drain Leakage Current	loss	$V_{DS} = 60 V, V_{GS} = 0 V$			10	μA
Gate to Source Leakage Current	lgss	$V_{GS} = \pm 20 V$ , $V_{DS} = 0 V$			±10	μA
Input Capacitance	Ciss	$V_{DS} = 10 V$ , $V_{GS} = 0 V$ , $f = 1 MHz$		6300		pF
Output Capacitance	Coss			1000		pF
Reverse Transfer Capacitance	Crss			490		pF
Turn-on Delay Time	td(on)	$I_{D} = 38  A,  V_{GS(on)} = 10  V,  V_{DD} = 30  V,$		90		ns
Rise Time	tr	$R_G = 10 \Omega$		1100		ns
Turn-off Delay Time	td(off)			300		ns
Fall Time	tr			400		ns
Total Gate Charge	QG	$I_{\text{D}}$ = 75 A , $V_{\text{DD}}$ = 48 V, $V_{\text{GS}}$ = 10 V		106		nC
Gate to Source Charge	Q <sub>GS</sub>			20		nC
Gate to Drain Charge	Qgd			30		nC
Body Diode Forward Voltage	VF(S-D)	IF = 75 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 75 A, VGS = 0 V,		55		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/µs		100		nC

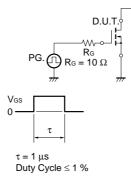
#### TEST CIRCUIT 1 AVALANCHE CAPABILITY

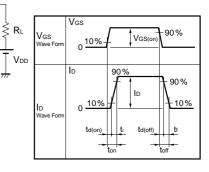


#### TEST CIRCUIT 3 GATE CHARGE



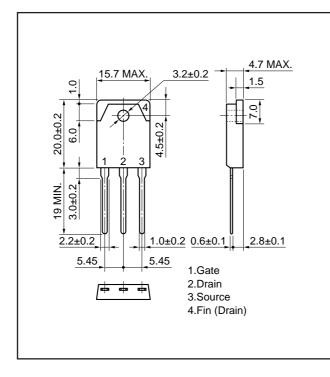






#### PACKAGE DRAWING (Unit: mm)

#### TO-3P (MP-88)



Gate Gate Protection Diode

**EQUIVALENT CIRCUIT** 

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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