

MOS FIELD EFFECT TRANSISTOR

2SK3435

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK3435 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super low on-state resistance:
- $R_{DS(on)1} = 14 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, \text{ ID} = 40 \text{ A})$
- RDS(on)2 = $22 \text{ m}\Omega \text{ MAX}$. (VGS = 4.0 V, ID = 40 A)
- ★ Low Ciss: Ciss = 3200 pF TYP.
 - Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

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	Drain to Source Voltage	VDSS	60	V
	Gate to Source Voltage	Vgss	±20	V
	Drain Current (DC)	ID(DC)	±80	А
	Drain Current (pulse) Note1	D(pulse)	±320	А
★	Total Power Dissipation ($Tc = 25^{\circ}C$)	Рт	84	W
	Total Power Dissipation ($T_A = 25^{\circ}C$)	Р⊤	1.5	W
	Channel Temperature	Tch	150	°C
	Storage Temperature	Tstg	-55 to +150	°C
★	Single Avalanche Current Note2	las	31	А
★	Single Avalanche Energy Note2	Eas	96	mJ

Notes 1. PW \leq 10 μ s, Duty cycle \leq 1 %

2. Starting T_{ch} = 25 °C, R_G = 25 Ω , V_{GS} = 20 V \rightarrow 0 V

ORDERING INFORMATION

PART NUMBER	PACKAGE		
2SK3435	TO-220AB		
2SK3435-S	TO-262		
2SK3435-Z	TO-220SMD		



(TO-220AB)







THERMAL RESISTANCE

\star	Channel to Case	Rth(ch-C)	1.49	°C/W
	Channel to Ambient	Rth(ch-A)	83.3	°C/W

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Document No. D14604EJ1V0DS00 (1st edition) Date Published March 2000 NS CP(K) Printed in Japan The mark \star shows major revised points.

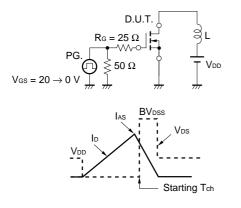
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, Id = 40 A		11	14	mΩ
	RDS(on)2	Vgs = 4.0 V, Id = 40 A		16	22	mΩ
Gate to Source Cut-off Voltage	VGS(off)	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	Vds = 10 V, Id = 40 A	21	43		S
Drain Leakage Current	IDSS	$V_{DS} = 60 V, V_{GS} = 0 V$			10	μA
Gate to Source Leakage Current	lgss	$V_{GS} = \pm 20 V$, $V_{DS} = 0 V$			±10	μA
Input Capacitance	Ciss	$V_{DS} = 10 V$, $V_{GS} = 0 V$, $f = 1 MHz$		3200		pF
Output Capacitance	Coss			520		pF
Reverse Transfer Capacitance	Crss			260		pF
Turn-on Delay Time	td(on)	$I_{D} = 40 \text{ A}, \text{ V}_{GS(on)} = 10 \text{ V}, \text{ V}_{DD} = 30 \text{ V},$		80		ns
Rise Time	tr	R _G = 10 Ω		1200		ns
Turn-off Delay Time	t _{d(off)}			200		ns
Fall Time	tr			350		ns
Total Gate Charge	QG	$I_D = 80 \text{ A}$, $V_{DD} = 48 \text{ V}$, $V_{GS} = 10 \text{ V}$		60		nC
Gate to Source Charge	Q _{GS}			10		nC
Gate to Drain Charge	Qgd			16		nC
Body Diode Forward Voltage	VF(S-D)	IF = 80 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 80 A, VGs = 0 V,		46		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/µs		66		nC

ELECTRICAL CHARACTERISTICS (TA = 25 °C)

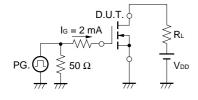
NEC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

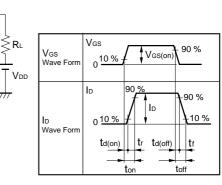
TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



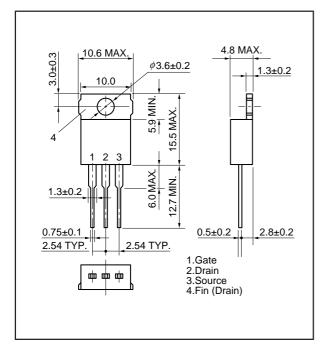
D.U.T. ١ΛΛ Rg PG. Vgs 0 · τ $\tau = 1 \,\mu s$ Duty Cycle $\leq 1 \%$



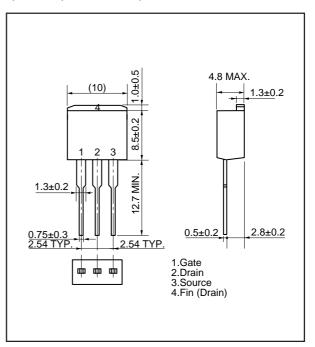
Preliminary Data Sheet D14604EJ1V0DS00

PACKAGE DRAWINGS (Unit: mm)

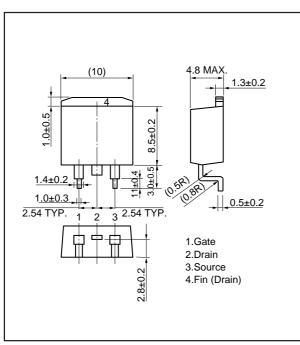
1) TO-220AB (MP-25)



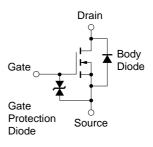
2) TO-262 (MP-25 Fin Cut)



3) TO-220SMD (MP-25Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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