

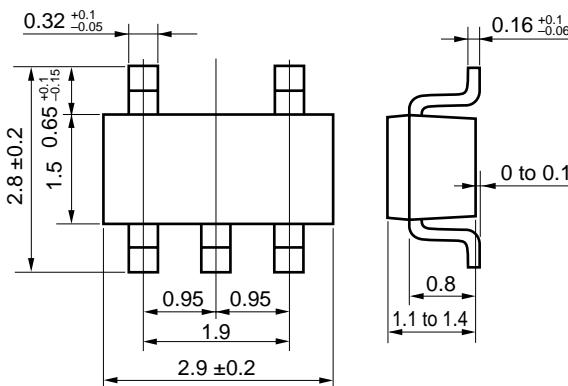
N-CHANNEL/P-CHANNEL MOS FET (5-PIN 2 CIRCUITS)

The μ PA505T is a mini-mold device provided with two MOS FET circuits. It achieves high-density mounting and saves mounting costs.

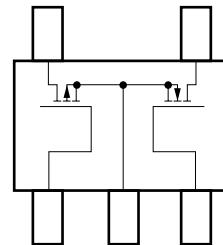
FEATURES

- Two source common MOS FET circuits in package the same size as SC-59
- Complementary MOS FETs are provided in one package.
- Automatic mounting supported

PACKAGE DIMENSIONS (in millimeters)



PIN CONNECTION (Top View)



Marking: FA

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain to Source Voltage	V_{DSS}	50/-50	V
Gate to Source Voltage	V_{GSS}	$\pm 20/\mp 16$	V
Drain Current (DC)	$I_D(\text{DC})$	$\pm 100/\mp 100$	mA
Drain Current (pulse)	$I_D(\text{pulse})^*$	$\pm 200/\mp 200$	mA
Total Power Dissipation	P_T	300 (TOTAL)	mW
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

* $PW \leq 10$ ms, Duty Cycle $\leq 50\%$

Note The left and right values in the ratings column are correspond to N-ch and P-ch FETs, respectively.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$)

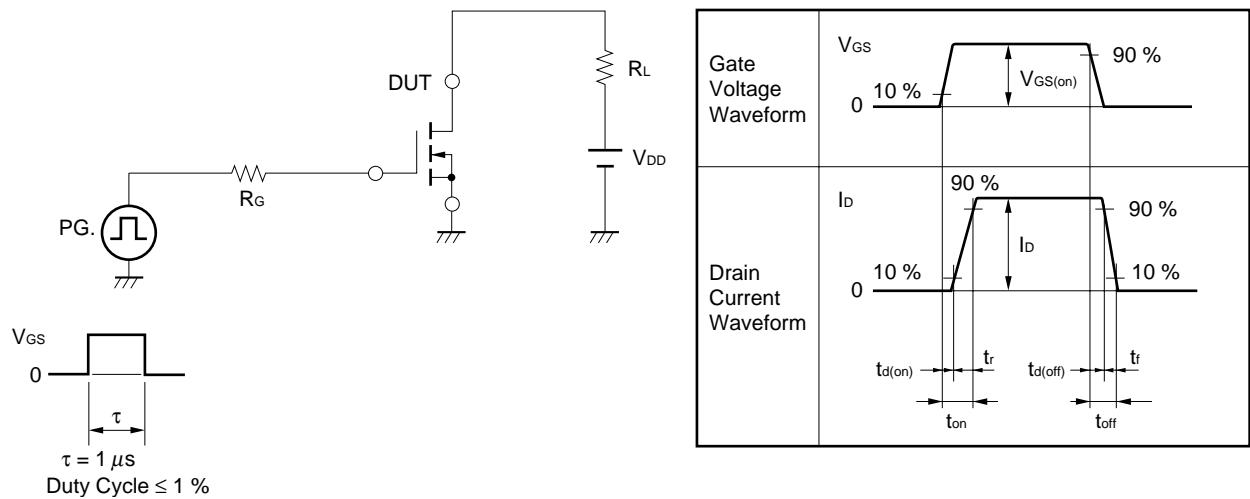
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Cut-off Current	I_{DS}	$V_{DS} = 50/-50 V, V_{GS} = 0$	—	—	1.0 —1.0	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 20/\mp 16 V, V_{DS} = 0$	—	—	±1.0 ±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = 5.0/-5.0 V, I_D = 1/-1 \mu A$	0.8 —1.5	1.4 —1.9	1.8 —2.5	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = 5.0/-5.0 V, I_D = 10/-10 mA$	20 15	—	—	mS
Drain to Source On-State Resistance	$R_{DS(on)1}$	$V_{GS} = 4/-4 V, I_D = 10/-10 mA$	—	19 60	30 100	Ω
Drain to Source On-State Resistance	$R_{DS(on)2}$	$V_{GS} = 10/-10 V, I_D = 10/-10 mA$	—	15 40	25 60	Ω
Input Capacitance	C_{iss}	$V_{DS} = 5.0/-5.0 V$ $V_{GS} = 0, f = 1.0 \text{ MHz}$	—	16 10	—	pF
Output Capacitance	C_{oss}		—	12 4	—	pF
Reverse Transfer Capacitance	C_{rss}		—	3 4	—	pF
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 5.0/-5.0 V, I_D = 10/-10 mA$ $V_{GS(on)} = 5.0/-5.0 V$ $R_G = 10 \Omega, R_L = 500 \Omega$	—	17 40	—	ns
Rise Time	t_r	—	10 40	—	ns	
Turn-Off Delay Time	$t_{d(off)}$	—	68 100	—	ns	
Fall Time	t_f	—	38 80	—	ns	

Marking: FA

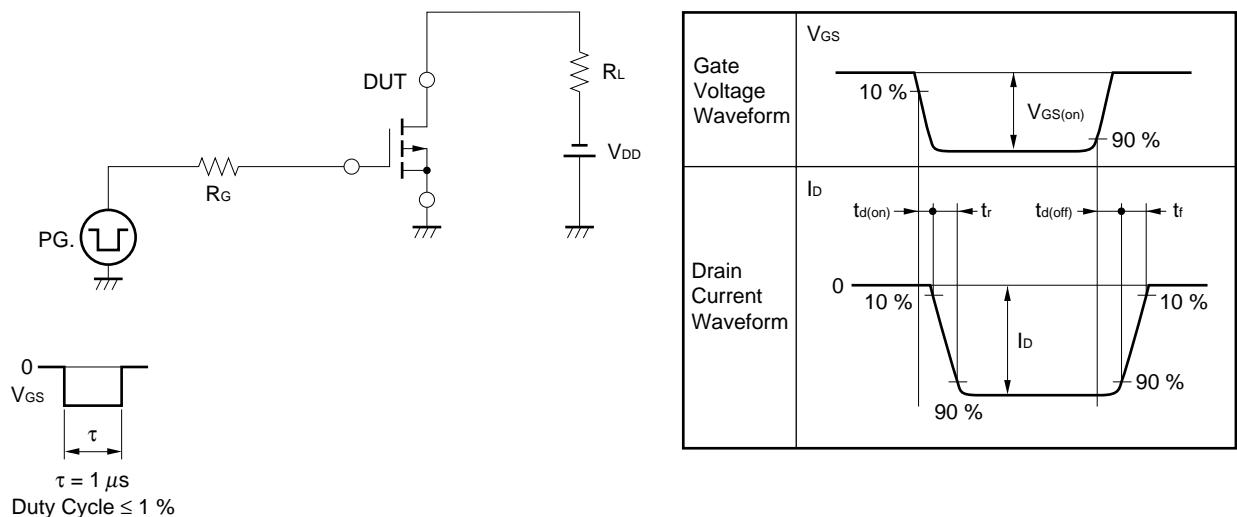
Note The left and right values in above table represent the N-ch and P-ch characteristics, respectively.

**SWITCHING TIME MEASUREMENT CIRCUIT AND MEASUREMENT CONDITIONS
(RESISTANCE LOADED)**

- N-ch part

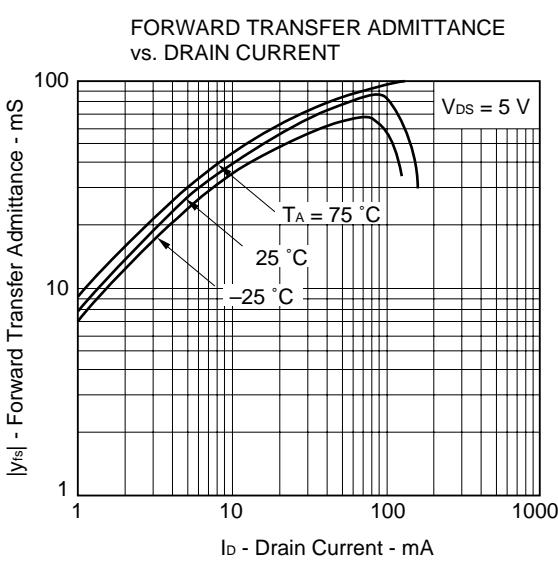
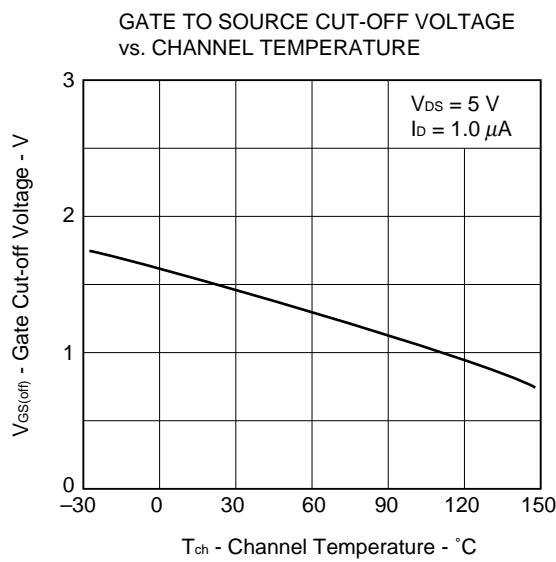
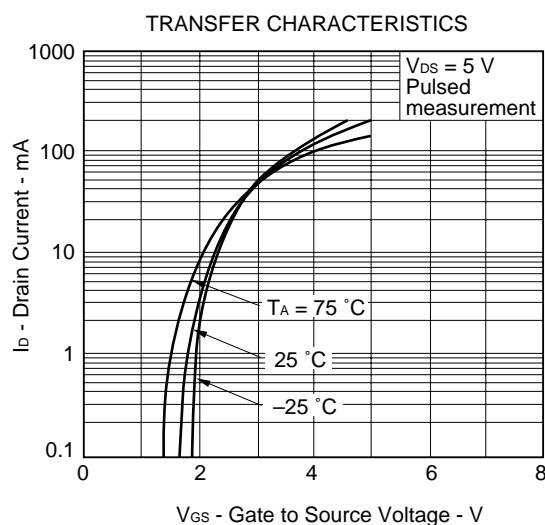
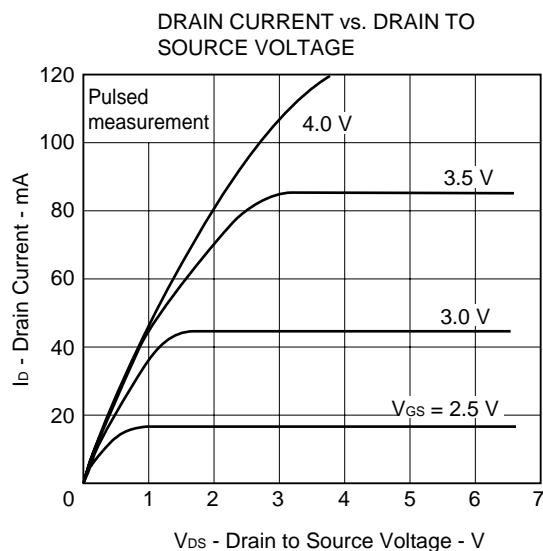
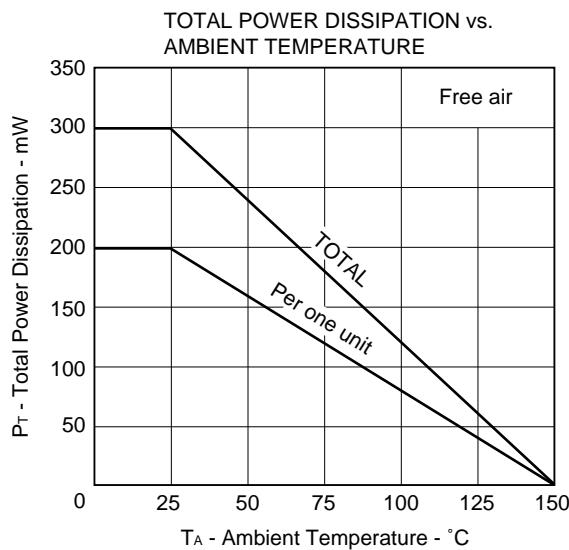
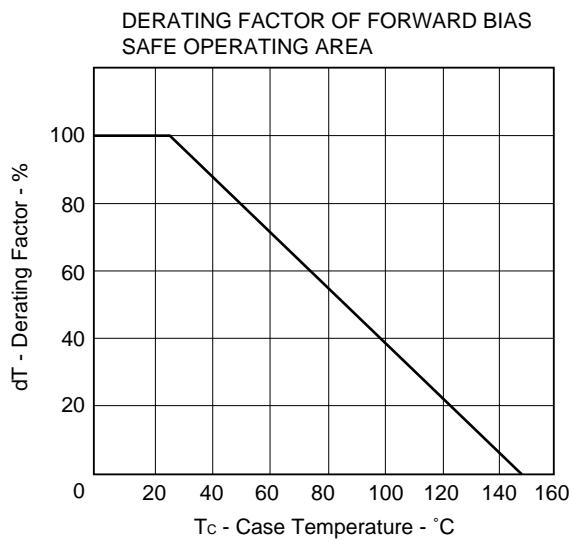


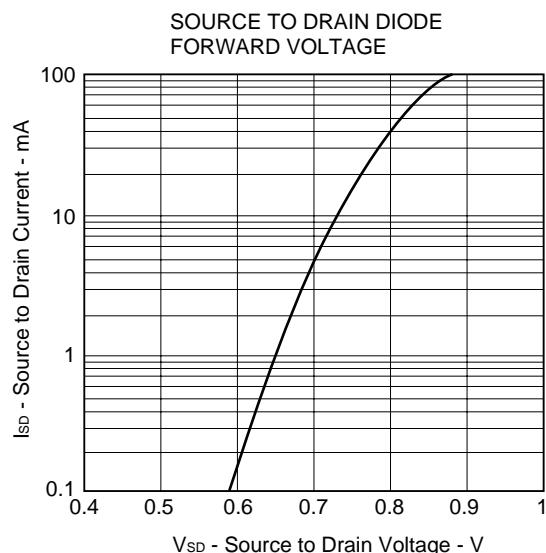
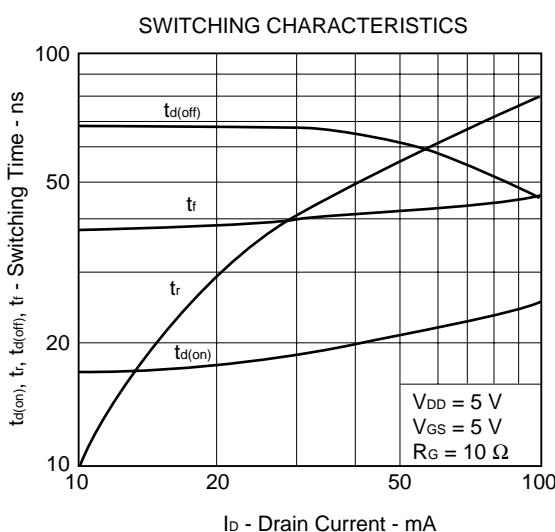
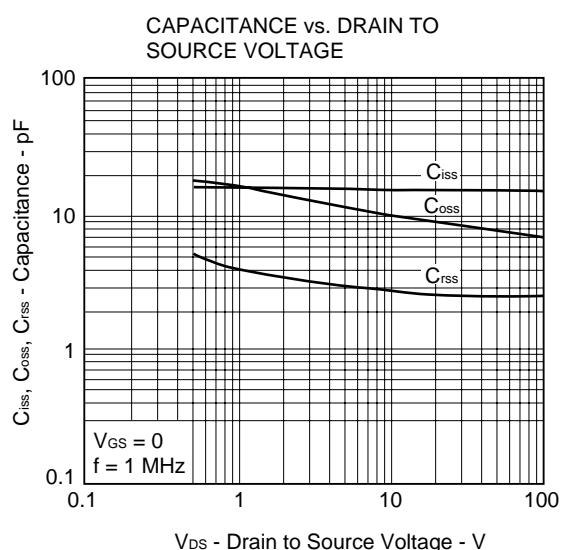
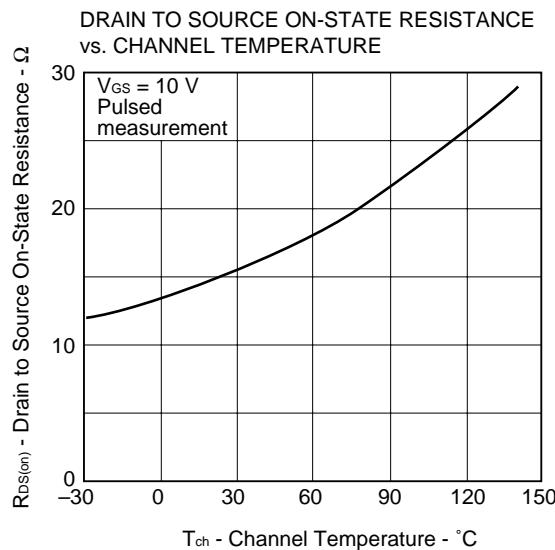
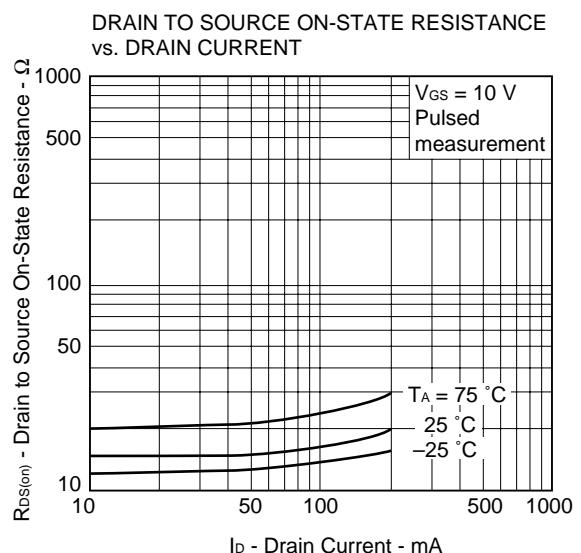
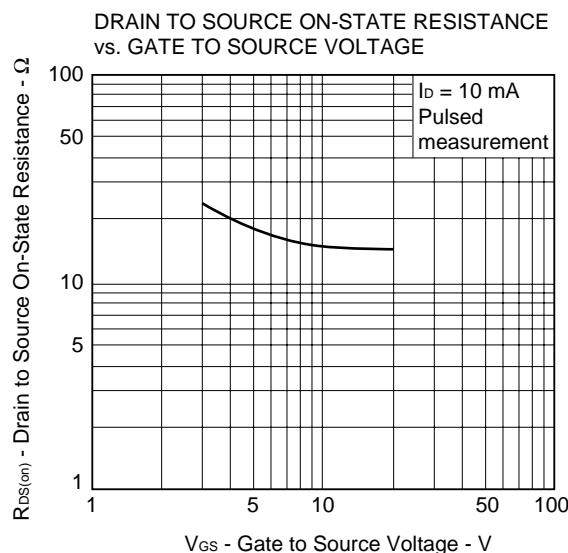
- P-ch part



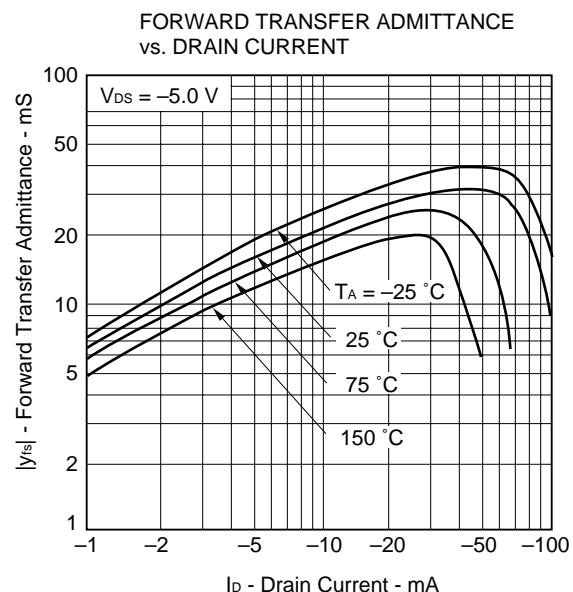
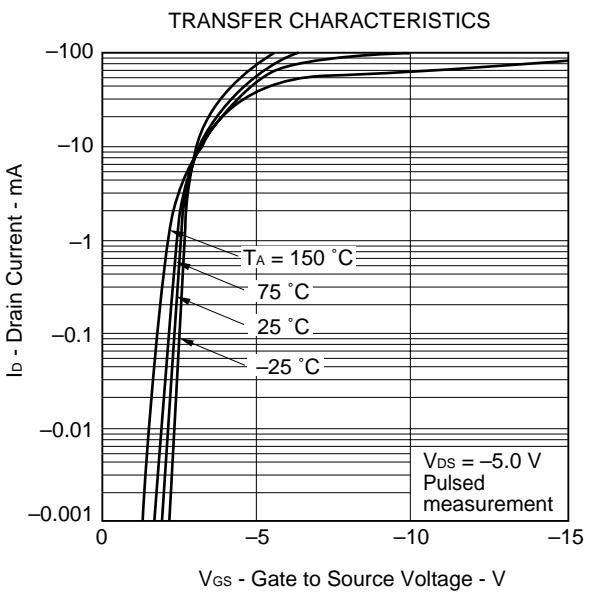
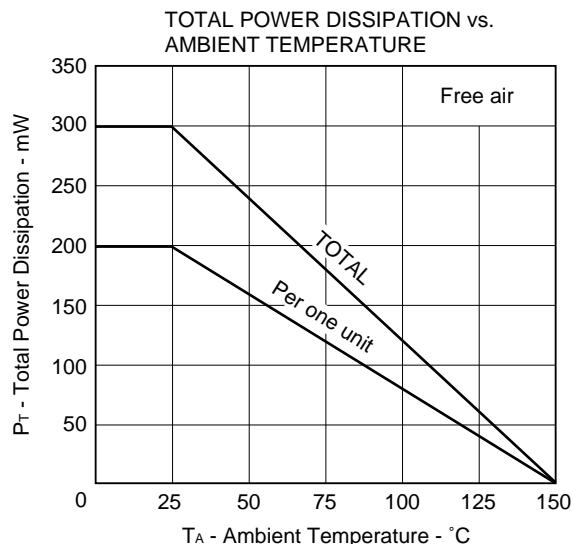
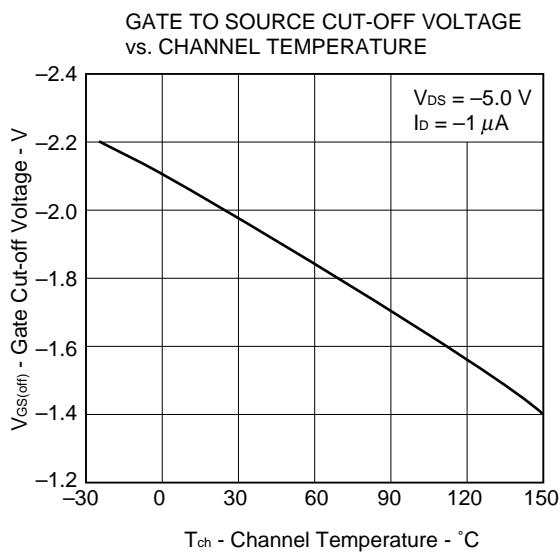
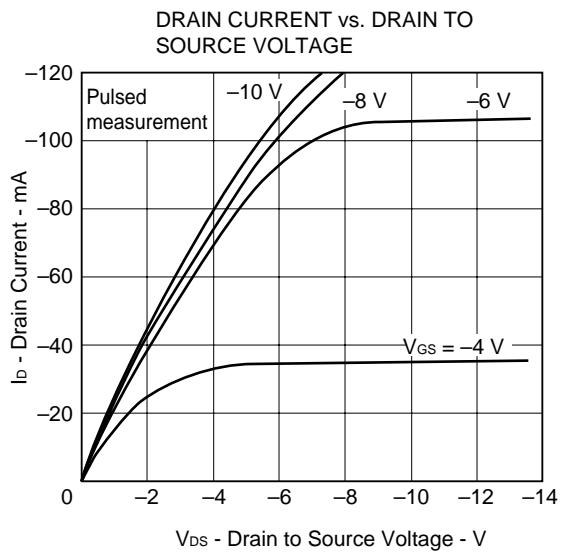
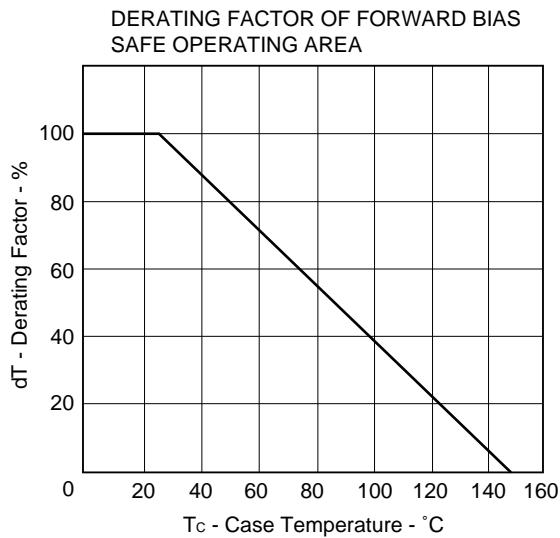
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

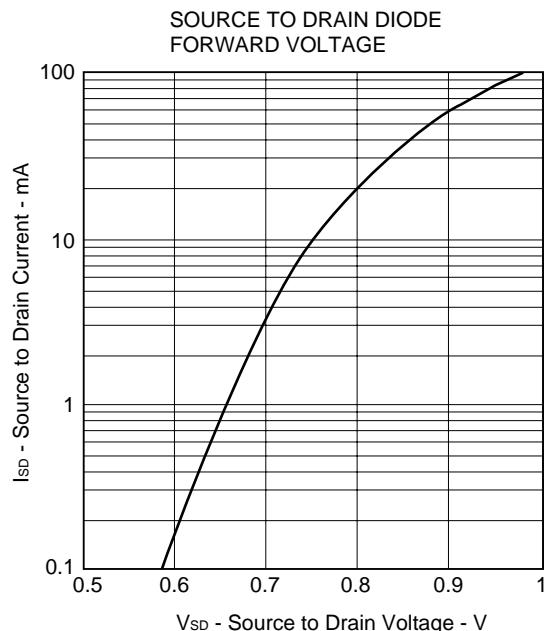
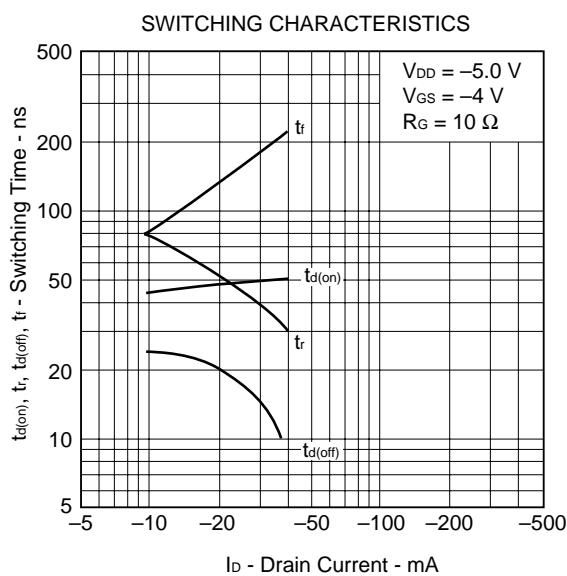
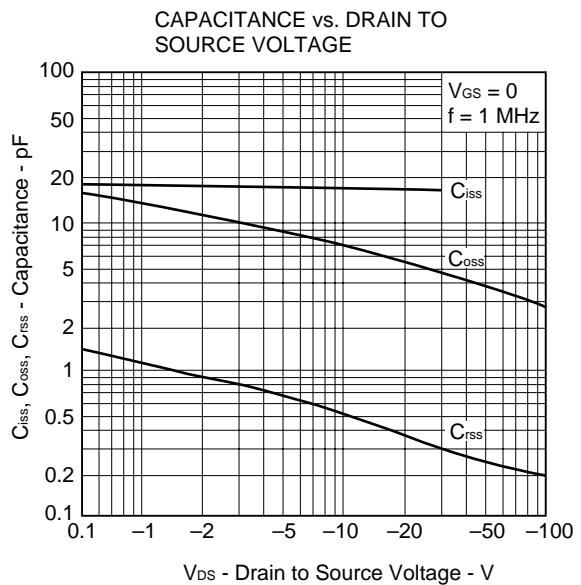
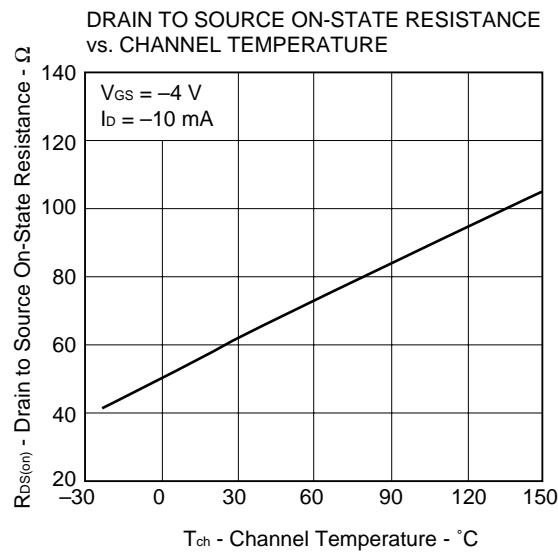
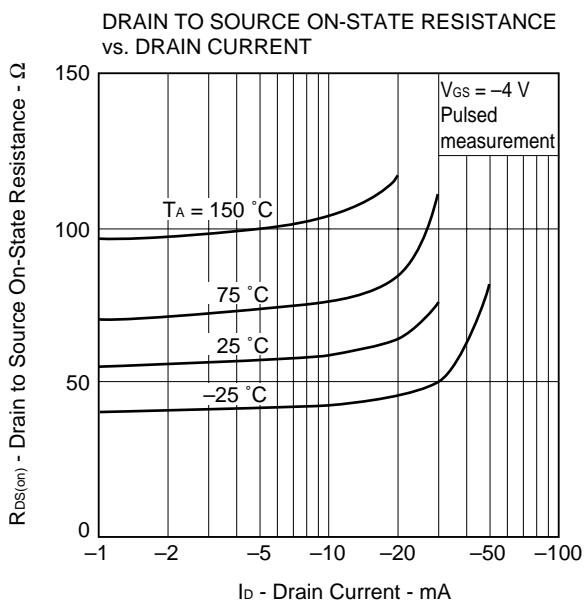
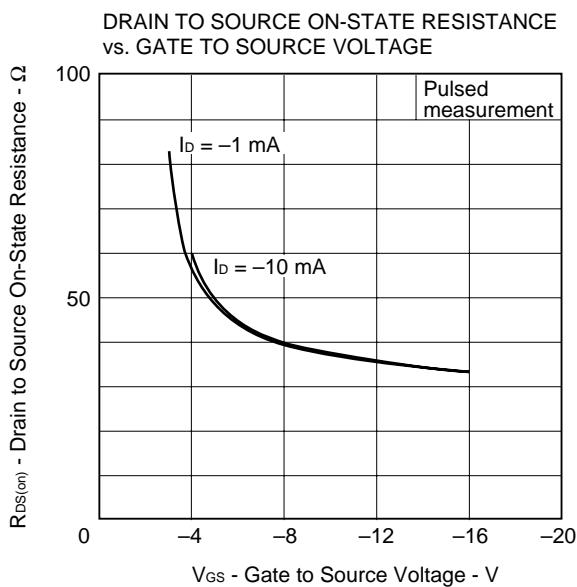
- N-ch part





- P-ch part





REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E

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Anti-radioactive design is not implemented in this product.