

**PRELIMINARY**

Notice: This is not a final specification.  
Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS  
**M37273MF-XXXSP**  
**M37273EFSP**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
and ON-SCREEN DISPLAY CONTROLLER

**DESCRIPTION**

The M37273MF-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 52-pin shrink plastic molded DIP.

In addition to their simple instruction sets, the ROM, RAM and I/O addresses are placed on the same memory map to enable easy programming.

The M37273MF-XXXSP has a OSD function and a data slicer function, so it is useful for a channel selection system for TV with a closed caption decoder. The features of the M37273EFSP are similar to those of the M37273MF-XXXSP except that these chips have a built-in PROM which can be written electrically.

**FEATURES**

- Number of basic instructions ..... 71
- Memory size
  - ROM ..... 60 K bytes
  - RAM ..... 1472 bytes  
(including ROM correction memory: 64 bytes)
  - ROM for OSD ..... 10 K bytes
  - RAM for OSD ..... 128 bytes
- Minimum instruction execution time  
..... 0.5  $\mu$ s (at 8 MHz oscillation frequency)
- Power source voltage ..... 5 V  $\pm$  10 %
- Subroutine nesting ..... 128 levels (Max.)
- Interrupts ..... 17 types, 16 vectors
- 8-bit timers ..... 6
- Programmable I/O ports (Ports P0, P1, P2, P30, P31) ..... 26
- Input ports (Ports P50, P51) ..... 2
- Output ports (Ports P52–P57, P6) ..... 14
- 12 V withstand ports ..... 6
- LED drive ports ..... 4
- Serial I/O ..... 8-bit X 1 channel
- Multi-master I<sup>2</sup>C-BUS interface ..... 1 (2 systems)
- A-D comparator (6-bit resolution) ..... 6 channels
- PWM output circuit (8-bit) ..... 8-bit X 6
- ROM correction function ..... 32 bytes X 2
- Power dissipation
  - In high-speed mode ..... 165mW  
(at Vcc = 5.5V, 8MHz oscillation frequency, CRT on, and Data slicer on)
  - In low-speed mode ..... 0.33mW  
(at Vcc = 5.5V, 32 kHz oscillation frequency)
- Data slicer

● OSD function

- Display characters ..... 32 characters X 2 lines  
(16 lines maximum)
- Kinds of characters ..... 254 kinds
- Character display area ..... CC mode : 16 X 26 dots  
OSD mode : 16 X 20 dots
- Kinds of character sizes ..... CC mode : 1 type  
OSD mode : 8 types
- Kinds of character colors (It can be specified by the character)  
maximum 7 kinds
- Kings of character background colors ... CC mode : 1 type (black)  
OSD mode : 7 types  
(It can be specified by the character)
- Display position
  - Horizontal ..... 128 levels
  - Vertical ..... 512 levels
- Attribute ..... CC mode : smooth italic, underline, flash  
OSD mode : border
- Kinds of raster colors (maximum 7 kinds)
- Smooth roll-up function
- Window function
- Automatic solid space

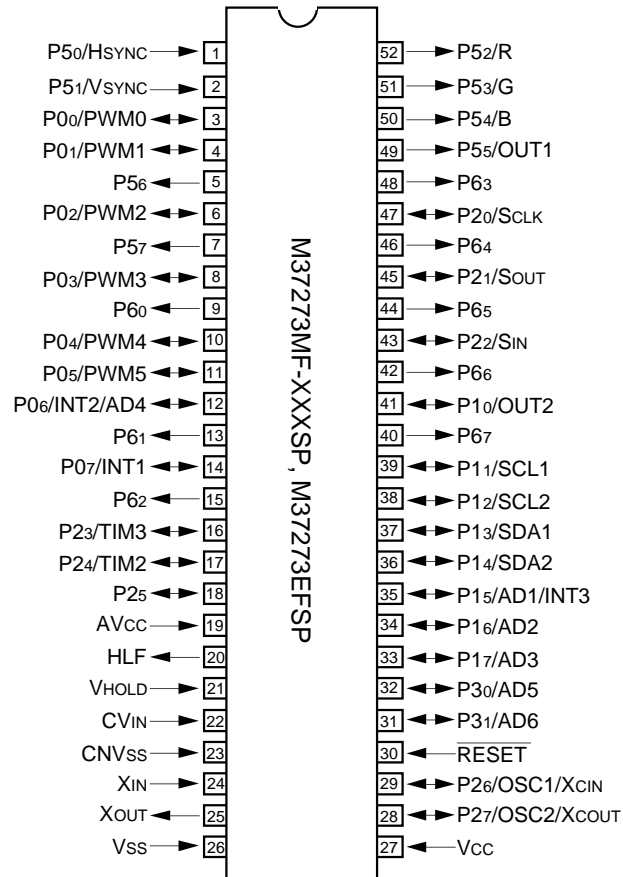
**APPLICATION**

TV with a closed caption decoder

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**PIN CONFIGURATION (TOP VIEW)**

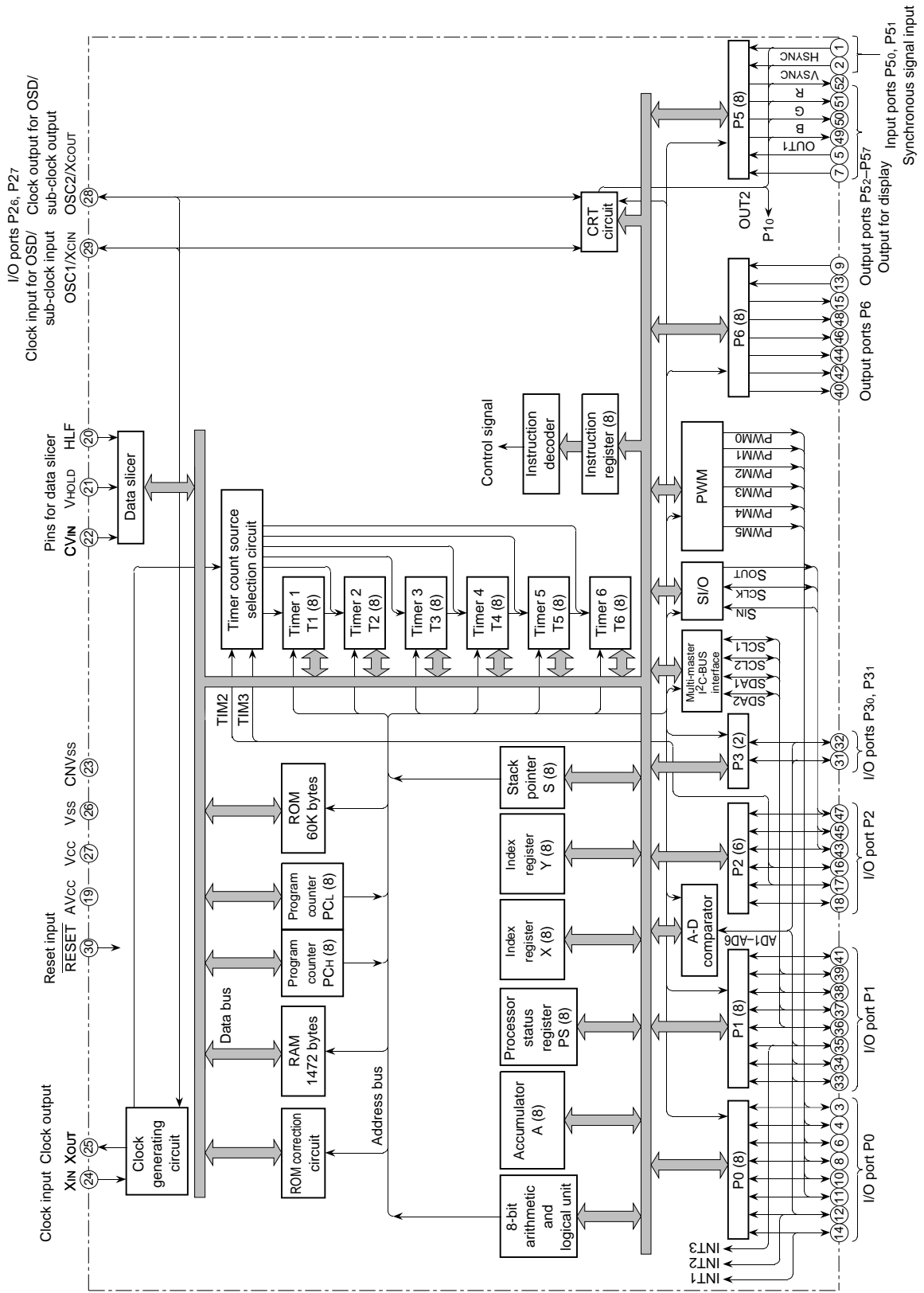


**Outline 52P4B**

# M37273MF-XXXSP M37273EFSP

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## FUNCTIONAL BLOCK DIAGRAM of M37273MF-XXXSP



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**FUNCTIONS**

Parameter		Functions
Number of basic instructions		71
Instruction execution time		0.5 $\mu$ s (the minimum instruction execution time, at 8 MHz oscillation frequency)
Clock frequency		8 MHz (maximum)
Memory size	ROM	60 K bytes
	RAM	1472 bytes (including ROM correction memory : 64 bytes)
	OSD ROM	10 K bytes
	OSD RAM	128 bytes
Input/Output ports	P0	I/O 8-bit X 1 (N-channel open-drain output structure, can be used as PWM output pins, INT input pins, AD input pin)
	P10–P17	I/O 8-bit X 1 (P10 and P15–P17: CMOS input/output structure, P11–P14: CMOS input/output or N-channel open-drain output structure, can be used as OSD output pin, AD input pins, INT input pin, multi-master I <sup>2</sup> C-BUS interface)
	P20–P27	I/O 8-bit X 1 (P20 and P21: CMOS input/output or N-channel open-drain output structure, P22–P27: CMOS input/output structure, can be used as serial input/output pins, external clock input pins)
	P30, P31	I/O 2-bit X 1 (CMOS input/output or N-channel open-drain output structure, can be used as AD input pins)
	P50, P51	Input 2-bit X 1 (can be used as OSD input pins)
	P52–P57, P6	Output 14-bit X 1 (CMOS output structure, can be used as OSD output pins)
Serial I/O		8-bit X 1
Multi-master I <sup>2</sup> C-BUS interface		1 (2 systems)
A-D comparator		6 channels (6-bit resolution)
PWM output circuit		8-bit X 6
Timers		8-bit timer X 6
ROM correction function		32 bytes X 2
Subroutine nesting		128 levels (maximum)
Interrupt		External interrupt X 3, Internal timer interrupt X 6, Serial I/O interrupt X 1, OSD interrupt X 1, Multi-master I <sup>2</sup> C-BUS interface interrupt X 1, Data slicer interrupt X 1, f(XIN)/4096 interrupt X 1, VSYNC interrupt X 1, BRK interrupt X 1
Clock generating circuit		2 built-in circuits (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Data slicer		Built-in
OSD function	Number of display characters	32 characters X 2 lines (maximum 16 lines by software)
	Character display area	CC mode: 16 X 26 dots (character dot structure : 16 X 20 dots) OSD mode: 16 X 20 dots
	Kinds of characters	254 kinds
	Kinds of character sizes	CC mode: 1 kinds OSD mode: 8 kinds
	Kinds of character colors	Maximum 7 kinds (R, G, B)
	Display position (horizontal, vertical)	128 levels (horizontal) X 512 levels (vertical)

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**FUNCTIONS (continued)**

Parameter				Functions
Power source voltage				5 V ± 10 %
Power dissipation	In high-speed mode	OSD ON	Data slicer ON	165 mW typ. (at oscillation frequency f(XIN) = 8 MHz, fosc = 27 MHz)
		OSD OFF	Data slicer OFF	82.5 mW typ. (at oscillation frequency f(XIN) = 8 MHz)
	In low-speed mode	OSD OFF	Data slicer OFF	0.33mW typ. (at oscillation frequency f(XCIN) = 32 kHz, f(XIN) = stopped)
		In stop mode		0.055 mW (maximum)
Operating temperature range				-10 °C to 70 °C
Device structure				CMOS silicon gate process
Package				52-pin shrink plastic molded DIP

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## PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
Vcc, AVcc Vss	Power source		Apply voltage of $5\text{ V} \pm 10\%$ (typical) to Vcc and AVcc, and 0 V to Vss.
CNVss	CNVss		Connected to Vss.
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for $2\ \mu\text{s}$ or more (under normal Vcc conditions) If more time is needed for the quartz-crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
XIN	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic resonator or a quartz-crystal oscillator is connected between pins XIN and XOUT. If an external clock is used, the clock source should be connected to the XIN pin and the XOUT pin should be left open.
XOUT	Clock output	Output	
P00/PWM0– P05/PWM5, P06/INT2/ AD4, P07/INT1	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open-drain output. See note 1 at end of Table for full details of port P0 functions.
	PWM output	Output	Pins P00–P05 are also used as PWM output pins PWM0–PWM5 respectively. The output structure is N-channel open-drain output.
	External interrupt input	Input	Pins P06, P07 are also used as external interrupt input pins INT2, INT1 respectively.
	Analog input	Input	P06 pin is also used as analog input pin AD4.
P10/OUT2, P11/SCL1, P12/SCL2, P13/SDA1, P14/SDA2, P15/AD1/ INT3, P16/AD2, P17/AD3	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
	OSD output	Output	P10 pin is also used as OSD output pin OUT2. The output structure is CMOS output.
	Multi-master I <sup>2</sup> C-BUS interface	I/O	Pins P11–P14 are used as SCL1, SCL2, SDA1 and SDA2 respectively, when multi-master I <sup>2</sup> C-BUS interface is used. The output structure is N-channel open-drain output.
	Analog input	Input	Pins P15–P17 are also used as analog input pins AD1 to AD3 respectively.
P20/SCLK, P21/SOUT, P22/SIN, P23/TIM3, P24/TIM2, P25, P26/OSC1/ XCIN, P27/OSC2/ XCOUT	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
	Serial I/O synchronous clock input/output	I/O	P20 pin is also used as serial I/O synchronous clock input/output pin SCLK. When using serial I/O, the output structure is N-channel open-drain output.
	Serial I/O data input	Input	P22 pin is also used as serial I/O data input pin SIN.
	Serial I/O data output	Output	P21 pin is also used as serial I/O data output pin SOUT. When using serial I/O, the output structure is N-channel open-drain output.
	External clock input	Input	Pins P23, P24 are also used as external clock input pins TIM3, TIM2 respectively.
	Clock input for OSD	Input	P26 pin is also used as OSD clock input pin OSC1. (See note 2)
	Clock output for OSD	Output	P27 pin is also used as OSD clock output pin OSC2. The output structure is CMOS output. (See note 2)
	Sub-clock input	Input	P26 pin is also used as sub-clock input pin XCIN.
Sub-clock output	Output	P27 pin is also used as sub-clock output pin XCOUT.	
P30/AD5, P31/AD6	I/O port P3	I/O	Ports P30, P31 are 2-bit I/O ports and have basically the same functions as port P0. Either CMOS output or N-channel open-drain output structure can be selected. (See note 3)
	Analog input	Input	Pins P30, P31 are also used as analog input pins AD5, AD6 respectively.

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**PIN DESCRIPTION (continued)**

Pin	Name	Input/ Output	Functions
P50/HSYNC P51/VSYNC	Input port P5	Input	Ports P50 and P51 are 2-bit input ports.
	Hsync input	Input	Pin P50 is also used as HSYNC input. This is a horizontal synchronous signal input for OSD.
	Vsync input	Input	Pin P51 is also used as VSYNC input. This is a vertical synchronous signal input for OSD.
P52/R, P53/G P54/B P55/OUT1, P56, P57	Output port P5	Output	Ports P52–P57 are 6-bit output ports. The output structure is CMOS output.
	OSD output	Output	Pins P52–P55 are also used as OSD output pins R, G, B, OUT1 respectively. The output structure is CMOS output.
P60–P67	Output port P6	Output	Port P6 is an 8-bit output port. The output structure is CMOS output.
CVIN	I/O for data slicer	Input	Input composite video signal through a capacitor.
VHOLD		Input	Connect a capacitor between VHOLD and VSS.
HLF			Connect a filter using of a capacitor and a resistor between HLF and Vss.

- Notes 1 :** As shown in the memory map (Figure 5), port P0 is accessed as a memory at address 00C0<sub>16</sub> of zero page. Port P0 has the port P0 direction register (address 00C1<sub>16</sub> of zero page) which can be used to program each bit as an input ("0") or an output ("1"). The pins programmed as "1" in the direction register are output pins. When pins are programmed as "0," they are input pins. When pins are programmed as output pins, the output data are written into the port latch and then output. When data is read from the output pins, the output pin level is not read but the data of the port latch is read. This allows a previously-output value to be read correctly even if the output "L" voltage has risen, for example, because a light emitting diode was directly driven. The input pins float, so the values of the pins can be read. When data is written into the input pin, it is written only into the port latch, while the pin remains in the floating state.
- 2 :** To switch pin functions, set the raster color register and OSD control register. When pins P26 and P27 are used as the OSD clock input/output pins, set the corresponding bits of the port P2 direction register to "0" (input mode).
- 3 :** To switch output structures, set bits 2 and 3 of the port P3 direction register. When "0," CMOS output ; when "1," N-channel open-drain output.

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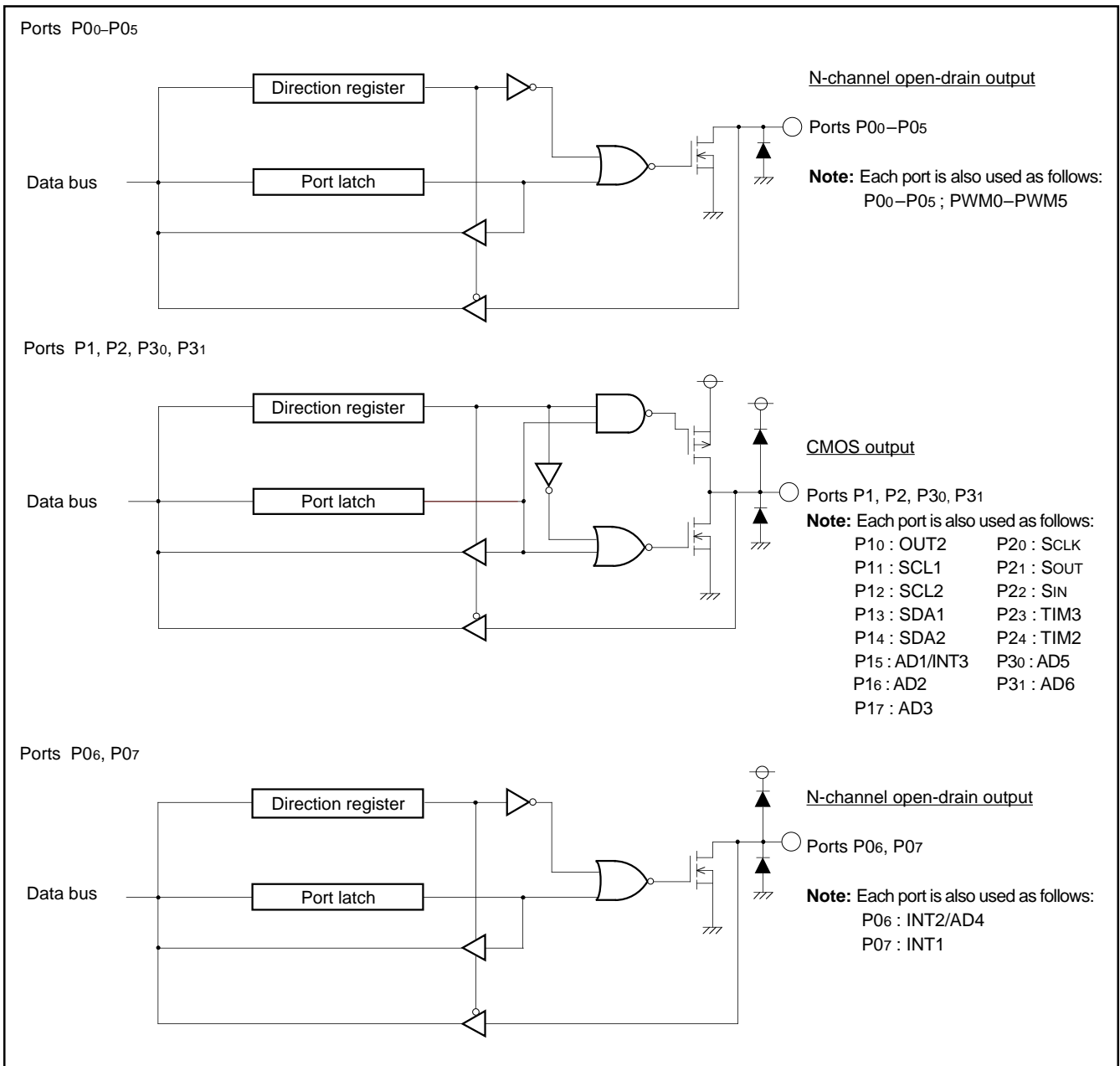


Fig. 1. I/O Pin Block Diagram (1)



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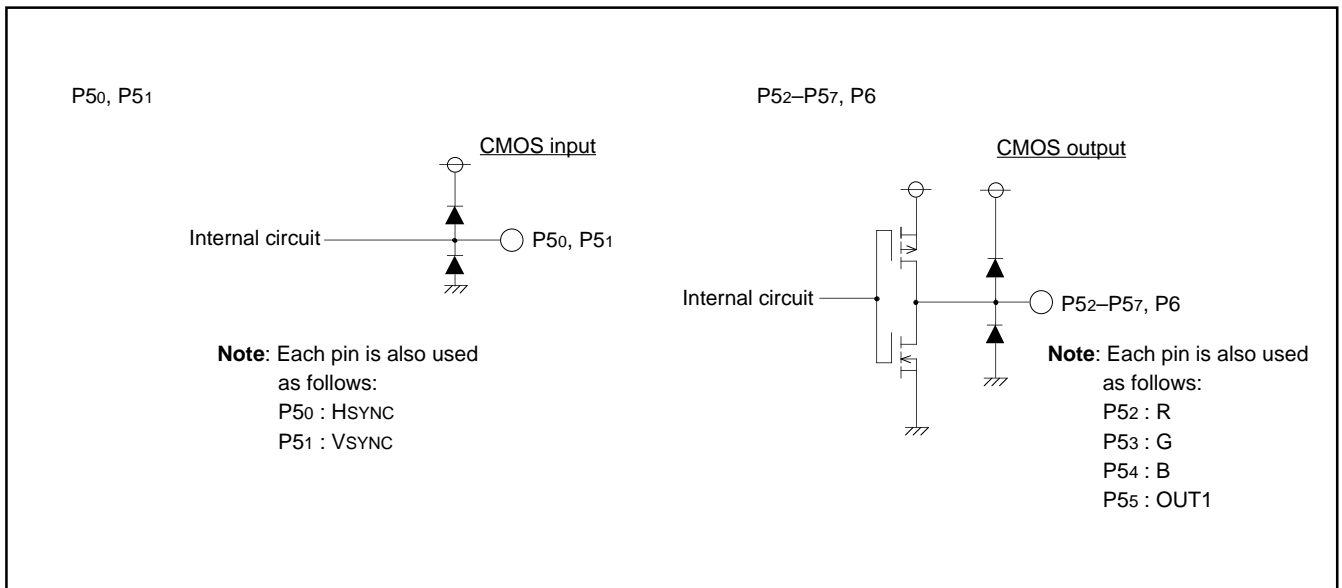


Fig. 2. I/O Pin Block Diagram (2)

# M37273MF-XXXSP M37273EFSP

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## FUNCTIONAL DESCRIPTION Central Processing Unit (CPU)

The M37273MF-XXXSP uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST, SLW instruction cannot be used.

The MUL, DIV, WIT and STP instructions can be used.

## CPU Mode Register

The CPU mode register contains the stack page selection bit and internal system clock selection bit. The CPU mode register is allocated at address 00FB16.

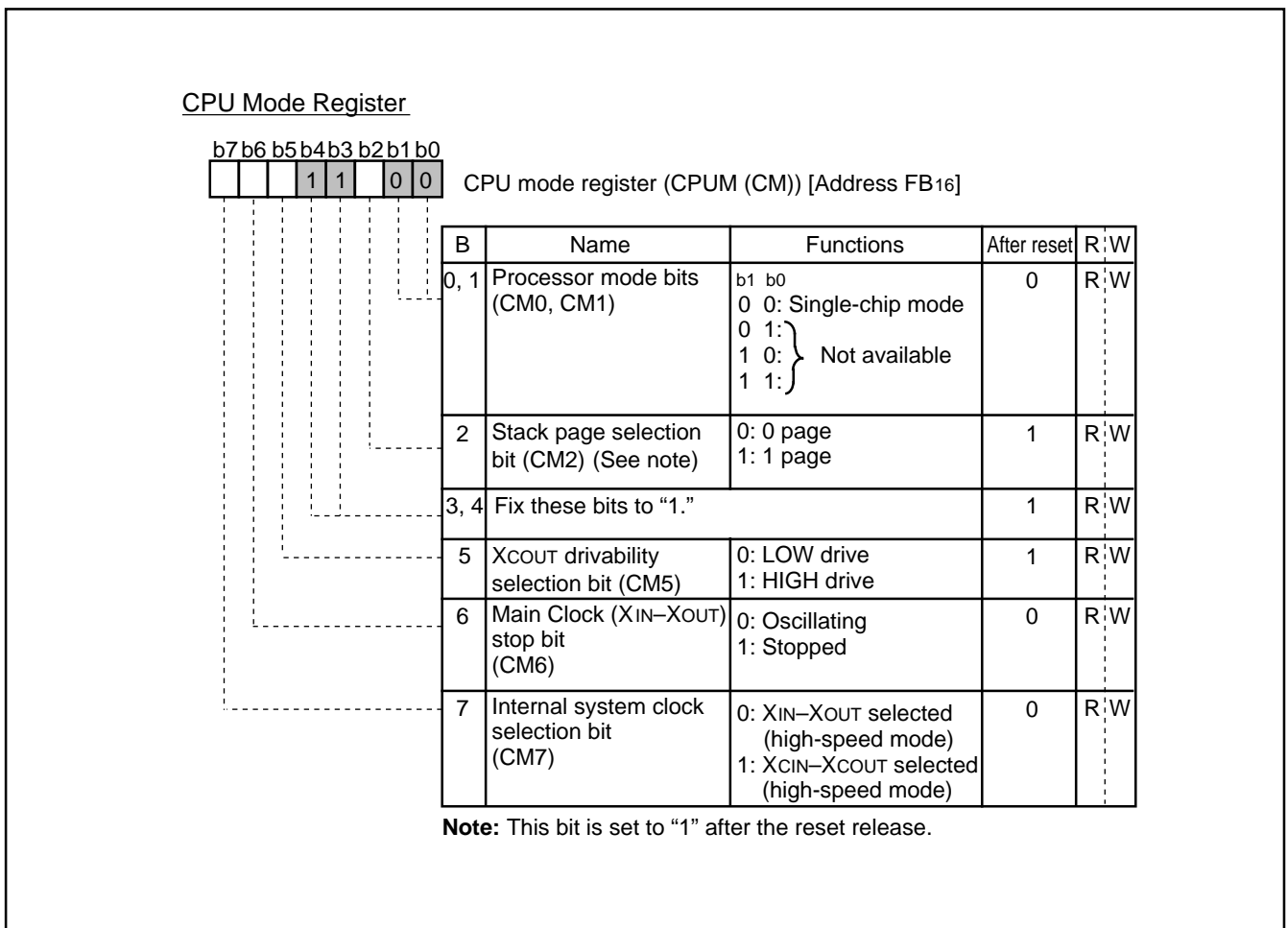


Fig. 3. CPU Mode Register

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**MEMORY**

**Special Function Register (SFR) Area**

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

**RAM**

RAM is used for data storage, for stack area of subroutine calls and interrupts, and for ROM memory for correction.

**ROM**

ROM is used for storing user programs as well as the interrupt vector area.

**RAM for OSD**

RAM for display is used for specifying the character codes and colors to display.

**ROM for OSD**

ROM for display is used for storing character data.

**Interrupt Vector Area**

The interrupt vector area contains reset and interrupt vectors.

**Zero Page**

The 256 bytes from addresses 0000<sub>16</sub> to 00FF<sub>16</sub> are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

**Special Page**

The 256 bytes from addresses FF00<sub>16</sub> to FFFF<sub>16</sub> are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

**ROM Correction Memory (RAM)**

This is used as the program area for ROM correction.

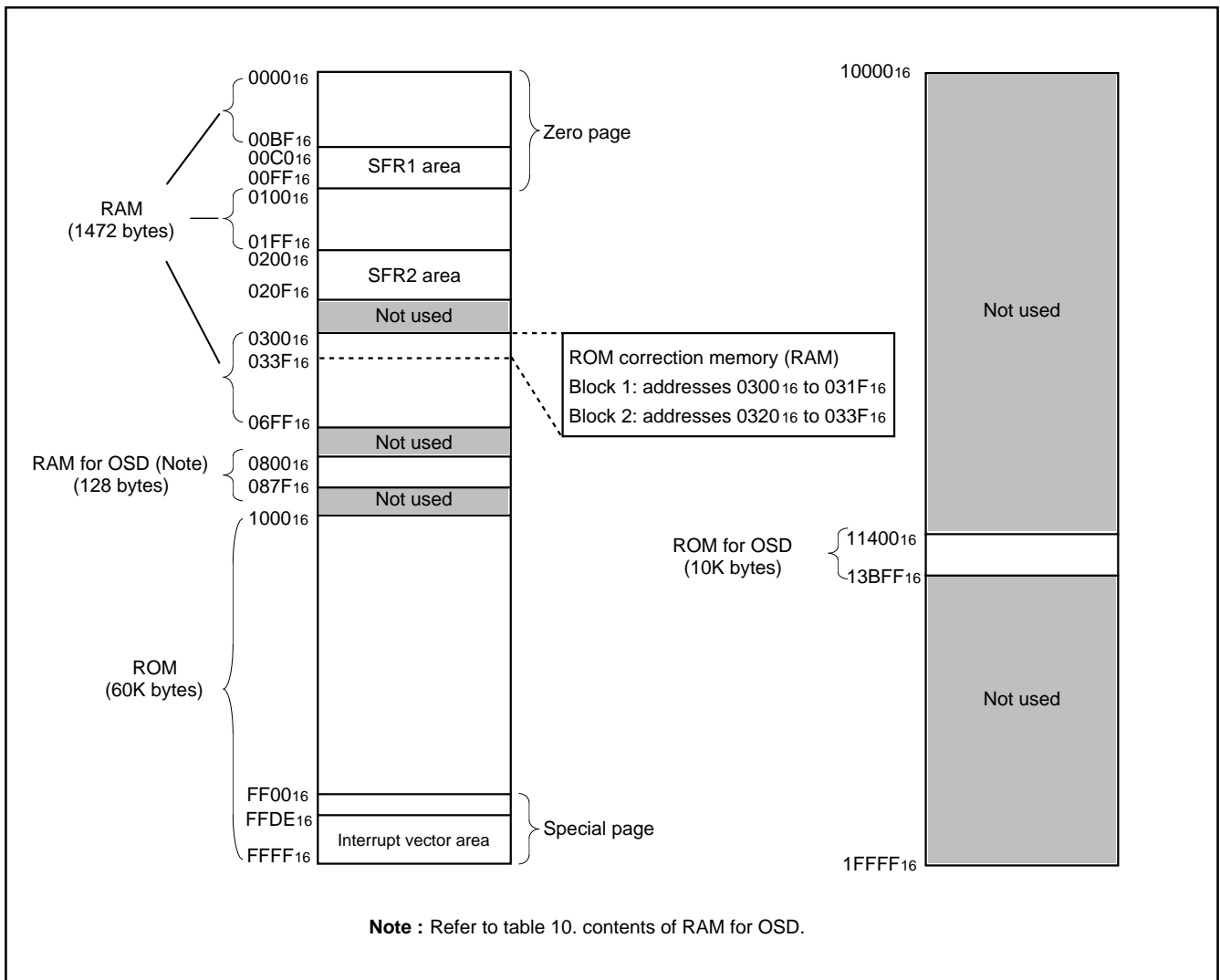


Fig. 4. Memory Map

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■ SFR1 Area (addresses C0<sub>16</sub> to DF<sub>16</sub>)

<Bit allocation>



: No function bit

0 : Fix this bit to "0"  
(do not write "1")

1 : Fix this bit to "1"  
(do not write "0")

<State immediately after reset>

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Undefined immediately after reset

Address	Register	Bit allocation								State immediately after reset								
		b7						b0		b7						b0		
C0 <sub>16</sub>	Port P0 (P0)																	?
C1 <sub>16</sub>	Port P0 direction register (D0)																	00 <sub>16</sub>
C2 <sub>16</sub>	Port P1 (P1)																	?
C3 <sub>16</sub>	Port P1 direction register (D1)																	00 <sub>16</sub>
C4 <sub>16</sub>	Port P2 (P2)																	?
C5 <sub>16</sub>	Port P2 direction register (D2)																	00 <sub>16</sub>
C6 <sub>16</sub>	Port P3 (P3)							P31	P30									0 0 0 0 0 0 ? ?
C7 <sub>16</sub>	Port P3 direction register (D3)		T3SC					P31C	P30C									00 <sub>16</sub>
C8 <sub>16</sub>																		?
C9 <sub>16</sub>																		?
CA <sub>16</sub>	Port P5 (P5)																	?
CB <sub>16</sub>	OSD port control register (PF)		PF7		PF5	PF4	PF3	PF2	0	0								00 <sub>16</sub>
CC <sub>16</sub>	Port P6 (P6)																	00 <sub>16</sub>
CD <sub>16</sub>																		?
CE <sub>16</sub>	Caption data register 3 (CD3)	CDL27	CDL26	CDL25	CDL24	CDL23	CDL22	CDL21	CDL20									?
CF <sub>16</sub>	Caption data register 4 (CD4)	CDH27	CDH26	CDH25	CDH24	CDH23	CDH22	CDH21	CDH20									?
D0 <sub>16</sub>	OSD control register (OC)	0	OC6	OC5	OC4	OC3	OC2	OC1	OC0									00 <sub>16</sub>
D1 <sub>16</sub>	Horizontal position register (HP)		HP6	HP5	HP4	HP3	HP2	HP1	HP0									00 <sub>16</sub>
D2 <sub>16</sub>	Block control register 1 (BC1)	BC17	BC16	BC15	BC14	BC13	BC12	BC11	BC10									?
D3 <sub>16</sub>	Block control register 2 (BC2)	BC27	BC26	BC25	BC24	BC23	BC22	BC21	BC20									?
D4 <sub>16</sub>	Vertical position register 1 (VP1)	VP17	VP16	VP15	VP14	VP13	VP12	VP11	VP10									?
D5 <sub>16</sub>	Vertical position register 2 (VP2)	VP27	VP26	VP25	VP24	VP23	VP22	VP21	VP20									?
D6 <sub>16</sub>	Window register 1 (WN1)	WN17	WN16	WN15	WN14	WN13	WN12	WN11	WN10									?
D7 <sub>16</sub>	Window register 2 (WN2)	WN27	WN26	WN25	WN24	WN23	WN22	WN21	WN20									?
D8 <sub>16</sub>	I/O polarity control register (PC)	0	PC6	PC5	PC4	PC3	PC2	PC1	PC0									40 <sub>16</sub>
D9 <sub>16</sub>	Raster color register (RC)	RC7	0	0	RC4	RC3	RC2	RC1	RC0									00 <sub>16</sub>
DA <sub>16</sub>																		?
DB <sub>16</sub>																		?
DC <sub>16</sub>	Interrupt input polarity control register (RE)							INT3	INT2	INT1								00 <sub>16</sub>
DD <sub>16</sub>																		00 <sub>16</sub>
DE <sub>16</sub>																		00 <sub>16</sub>
DF <sub>16</sub>																		00 <sub>16</sub>

Fig. 5. Memory Map of Special Function Register 1 (SFR1) (1)

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■ SFR1 Area (addresses E0<sub>16</sub> to FF<sub>16</sub>)

<Bit allocation>



☐ : No function bit

0 : Fix this bit to "0" (do not write "1")

1 : Fix this bit to "1" (do not write "0")

<State immediately after reset>

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Undefined immediately after reset

Address	Register	Bit allocation								State immediately after reset							
		b7						b0		b7						b0	
E0 <sub>16</sub>	Data slicer control register 1 (DSC1)	0	1	1	0	0	DSC12	DSC11	DSC10	0	0	0	0	0	0	0	0
E1 <sub>16</sub>	Data slicer control register 2 (DSC2)		0		DSC25	DSC24	DSC23		1		DSC20	? 0 ? 0 ? ? 0 ?					
E2 <sub>16</sub>	Caption data register 1 (CD1)	CDL17	CDL16	CDL15	CDL14	CDL13	CDL12	CDL11	CDL10	0	0	0	0	0	0	0	
E3 <sub>16</sub>	Caption data register 2 (CD2)	CDH17	CDH16	CDH15	CDH14	CDH13	CDH12	CDH11	CDH10	0	0	0	0	0	0	0	
E4 <sub>16</sub>	Clock run-in detect register (CRD)	CRD7	CRD6	CRD5	CRD4	CRD3				0	0	0	0	1	0	0	1
E5 <sub>16</sub>	Data clock position register (DPS)	DPS7	DPS6	DPS5	DPS4	DPS3	0	1	0	0	0	?	0	0	0	0	0
E6 <sub>16</sub>	Caption position register (CPS)	CPS7	CPS6	CPS5	CPS4	CPS3	CPS2	CPS1	CPS0	0	0	?	0	0	0	0	0
E7 <sub>16</sub>	Data slicer test register 2									0	0	0	0	0	0	0	0
E8 <sub>16</sub>	Data slicer test register 1									0	0	0	0	0	0	0	0
E9 <sub>16</sub>	Synchronous signal counter register (HC)			HC5	HC4	HC3	HC2	HC1	HC0	0	0	0	?	0	0	0	0
EA <sub>16</sub>	Serial I/O register (SIO)									?							
EB <sub>16</sub>	Serial I/O mode register (SM)	0	SM6	SM5	0	SM3	SM2	SM1	SM0	0	0	0	?	0	0	0	0
EC <sub>16</sub>	A-D control register 1 (AD1)				ADC14		ADC12	ADC11	ADC10	0	0	0	?	0	0	0	0
ED <sub>16</sub>	A-D control register 2 (AD2)			ADC25	ADC24	ADC23	ADC22	ADC21	ADC20	0	0	0	?	0	0	0	0
EE <sub>16</sub>	Timer 5 (T5)									0	7	1	6				
EF <sub>16</sub>	Timer 6 (T6)									FF	1	6					
F0 <sub>16</sub>	Timer 1 (T1)									FF	1	6					
F1 <sub>16</sub>	Timer 2 (T2)									0	7	1	6				
F2 <sub>16</sub>	Timer 3 (T3)									FF	1	6					
F3 <sub>16</sub>	Timer 4 (T4)									0	7	1	6				
F4 <sub>16</sub>	Timer mode register 1 (TM1)	TM17	TM16	TM15	TM14	TM13	TM12	TM11	TM10	0	0	1	1	1	1	0	0
F5 <sub>16</sub>	Timer mode register 2 (TM2)	TM27	TM26	TM25	TM24	TM23	TM22	TM21	TM20	0	0	1	1	1	1	0	0
F6 <sub>16</sub>	I <sup>2</sup> C data shift register (S0)	D7	D6	D5	D4	D3	D2	D1	D0	?							
F7 <sub>16</sub>	I <sup>2</sup> C address register (S0D)	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	RBW	0	0	1	6				
F8 <sub>16</sub>	I <sup>2</sup> C status register (S1)	MST	TRX	BB	PIN	AL	AAS	AD0	LRB	0	0	0	1	0	0	0	?
F9 <sub>16</sub>	I <sup>2</sup> C control register (S1D)	BSEL1	BSELO	<sup>10</sup> BIT SAD	ALS	ESO	BC2	BC1	BC0	0	0	1	6				
FA <sub>16</sub>	I <sup>2</sup> C clock control register (S2)	ACK	ACK BIT	FAST MODE	CCR4	CCR3	CCR2	CCR1	CCR0	0	0	1	6				
FB <sub>16</sub>	CPU mode register (CPUM)	CM7	CM6	CM5	1	1	CM2	0	0	0	0	1	1	1	1	0	0
FC <sub>16</sub>	Interrupt request register 1 (IREQ1)		IN3R	VSCR	OSDR	TM4R	TM3R	TM2R	TM1R	0	0	1	6				
FD <sub>16</sub>	Interrupt request register 2 (IREQ2)	0	TM56R	IICR	IN2R	CKR	SIR	DSR	IN1R	0	0	1	6				
FE <sub>16</sub>	Interrupt control register 1 (ICON1)		IN3E	VSCE	OSDE	TM4E	TM3E	TM2E	TM1E	0	0	1	6				
FF <sub>16</sub>	Interrupt control register 2 (ICON2)	TM56C	TM56E	IICE	IN2E	CKE	SIE	DSE	IN1E	0	0	1	6				

Fig. 6. Memory Map of Special Function Register 1 (SFR1) (2)

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■ SFR2 Area (addresses 200<sub>16</sub> to 20F<sub>16</sub>)

Address	Register	Bit allocation								State immediately after reset							
		b7							b0	b7							b0
200 <sub>16</sub>	PWM0 register (PWM0)																?
201 <sub>16</sub>	PWM1 register (PWM1)																?
202 <sub>16</sub>	PWM2 register (PWM2)																?
203 <sub>16</sub>	PWM3 register (PWM3)																?
204 <sub>16</sub>	PWM4 register (PWM4)																?
205 <sub>16</sub>	PWM5 register (PWM5)																?
206 <sub>16</sub>		00 <sub>16</sub>															?
207 <sub>16</sub>		00 <sub>16</sub>															?
208 <sub>16</sub>	PWM mode register 1 (PM1)						PM13										?
209 <sub>16</sub>	PWM mode register 2 (PM2)	0	0			PM25	PM24	PM23	PM22								?
20A <sub>16</sub>	ROM correction address 1 (high-order)					ADH17	ADH16	ADH15	ADH14								?
20B <sub>16</sub>	ROM correction address 1 (low-order)					ADL17	ADL16	ADL15	ADL14								?
20C <sub>16</sub>	ROM correction address 2 (high-order)					ADH27	ADH26	ADH25	ADH24								?
20D <sub>16</sub>	ROM correction address 2 (low-order)					ADL27	ADL26	ADL25	ADL24								?
20E <sub>16</sub>	ROM correction enable register (RCR)															RC1	RC0
20F <sub>16</sub>																	?

Fig. 7. Memory Map of Special Function Register 2 (SFR2) (1)

Register	Bit allocation								State immediately after reset							
	b7							b0	b7							b0
Processor status register (PS)	N	V	T	B	D	I	Z	C	?	?	?	?	?	?	1	?
Program counter (PCH)									Contents of address FFFF <sub>16</sub>							
Program counter (PCL)									Contents of address FFFE <sub>16</sub>							

Fig. 8. Internal State of Processor Status Register and Program Counter at Reset

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## INTERRUPTS

Interrupts can be caused by 17 different sources consisting of 4 external, 11 internal, 1 software, and reset. Interrupts are vectored interrupts with priorities as shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted,

- (1) The contents of the program counter and processor status register are automatically stored into the stack.
- (2) The interrupt disable flag I is set to "1" and the corresponding interrupt request bit is set to "0."
- (3) The jump destination address stored in the vector address enters the program counter.

Other interrupts are disabled when the interrupt disable flag is set to "1."

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 10 to 14 shows the interrupt-related registers.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1," interrupt request bit is "1," and the interrupt disable flag is "0." The interrupt request bit can be set to "0" by a program, but not set to "1." The interrupt enable bit can be set to "0" and "1" by a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 10 shows interrupt control.

## Interrupt Causes

- (1) VSYNC and OSD Interrupts  
The VSYNC interrupt is an interrupt request synchronized with the vertical sync signal.  
The OSD interrupt occurs after character block display to the CRT is completed.
- (2) INT1, INT2, INT3 Interrupts  
With an external interrupt input, the system detects that the level of a pin changes from "L" to "H" or from "H" to "L," and generates an interrupt request. The input active edge can be selected by bits 0, 1 and 2 of the interrupt input polarity register (address 00DC16) : when this bit is "0," a change from "L" to "H" is detected; when it is "1," a change from "H" to "L" is detected. Note that all bits are cleared to "0" at reset.
- (3) Timer 1, 2, 3 and 4 Interrupts  
An interrupt is generated by an overflow of timer 1, 2, 3 or 4.
- (4) Serial I/O Interrupt  
This is an interrupt request from the clock synchronous serial I/O function.
- (5) f(XIN)/4096 Interrupt  
This interrupt occurs regularly with a f(XIN)/4096 period. Clear bit 0 of the PWM mode register 1 to "0."
- (6) Data slicer Interrupt  
An interrupt occurs when slicing data is completed.
- (7) Multi-master I<sup>2</sup>C-BUS Interface Interrupt  
This is an interrupt request related to the multi-master I<sup>2</sup>C-BUS interface.
- (8) Timer 5 · 6 Interrupt  
An interrupt is generated by an overflow of timer 5 or 6. Their priorities are same, and can be switched by software.
- (9) BRK Instruction Interrupt  
This software interrupt has the least significant priority. It does not have a corresponding interrupt enable bit, and it is not affected by the interrupt disable flag I (non-maskable).

**Table 1. Interrupt Vector Addresses and Priority**

Interrupt Source	Priority	Vector Addresses	Remarks
Reset	1	FFFF16, FFFE16	Non-maskable
OSD interrupt	2	FFFD16, FFFC16	
INT1 interrupt	3	FFFB16, FFFA16	Active edge selectable
Data slicer interrupt	4	FFF916, FFF816	
Serial I/O interrupt	5	FFF716, FFF616	
Timer 4 interrupt	6	FFF516, FFF416	
f(XIN)/4096 interrupt	7	FFF316, FFF216	
VSYNC interrupt	8	FFF116, FFF016	Active edge selectable
Timer 3 interrupt	9	FFEF16, FFEE16	
Timer 2 interrupt	10	FFED16, FFEC16	
Timer 1 interrupt	11	FFEB16, FFEA16	
INT3 interrupt	12	FFE916, FFE816	Active edge selectable
INT2 interrupt	13	FFE716, FFE616	Active edge selectable
Multi-master I <sup>2</sup> C-BUS interface interrupt	14	FFE516, FFE416	
Timer 5 · 6 interrupt	15	FFE316, FFE216	Source switch by software (Note)
BRK instruction interrupt	16	FFDF16, FFDE16	Non-maskable (software interrupt)

**Note :** Switching a source during a program causes an unnecessary interrupt. Therefore, set a source at initializing of program.

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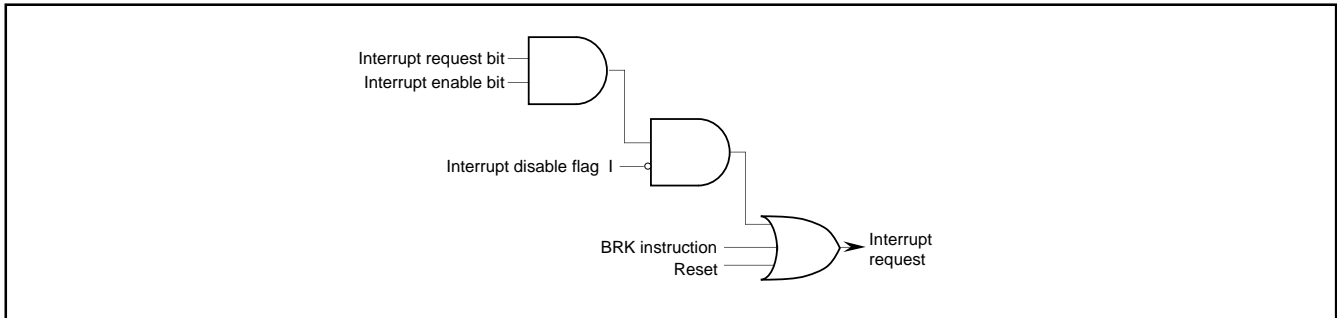


Fig. 9. Interrupt Control

Interrupt Request Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [Address 00FC<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
4	OSD interrupt request bit (OSDR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
6	INT3 interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

\*: "0" can be set by software, but "1" cannot be set.

Fig. 10. Interrupt Request Register 1

Interrupt Request Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 2 (IREQ2) [Address 00FD<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	INT1 interrupt request bit (INIR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	Data slicer interrupt request bit (DSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Serial I/O interrupt request bit (S1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3	f(X <sub>IN</sub> )/4096 interrupt request bit (CKR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
4	INT2 interrupt request bit (IN2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	Multi-master I <sup>2</sup> C-BUS interrupt request bit (IICR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
6	Timer 5 • 6 interrupt request bit (TM56R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Fix this bit to "0."		0	R	W

\*: "0" can be set by software, but "1" cannot be set.

Fig. 11. Interrupt Request Register 2



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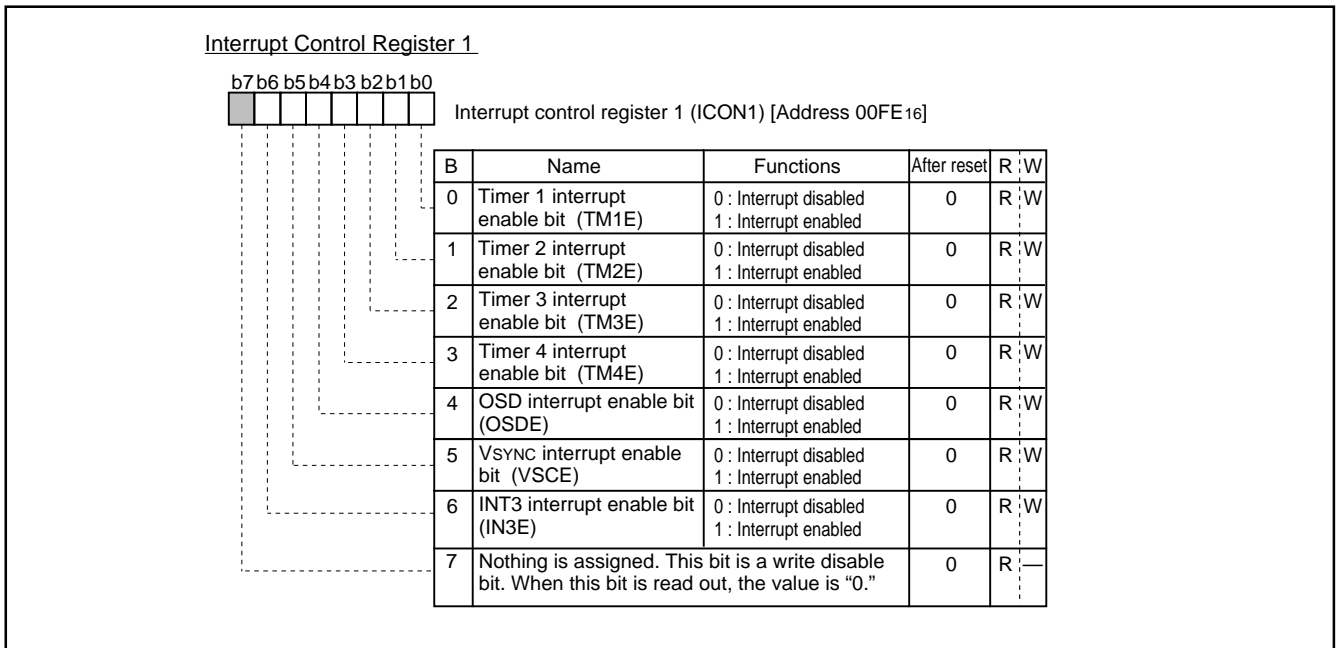


Fig. 12. Interrupt Control Register 1

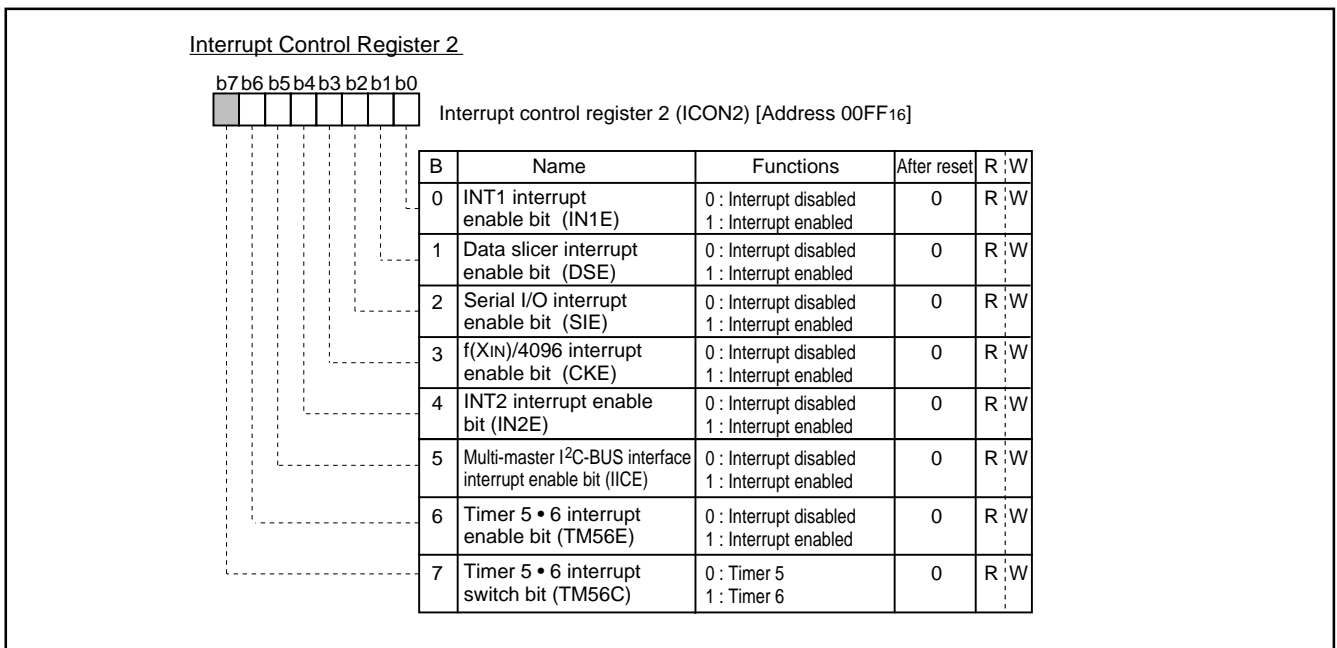
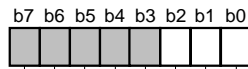


Fig. 13. Interrupt Control Register 2

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Interrupt Input Polarity Register



Interrupt input polarity register (RE) [Address 00DC<sub>16</sub>]

B	Name	Functions	After reset	R : W
0	INT1 polarity switch bit (INT1)	0 : Positive polarity 1 : Negative polarity	0	R : W
1	INT2 polarity switch bit (INT2)	0 : Positive polarity 1 : Negative polarity	0	R : W
2	INT3 polarity switch bit (INT3)	0 : Positive polarity 1 : Negative polarity	0	R : W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R : —

Fig. 14. Interrupt Input Polarity Register

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## TIMERS

The M37273MF-XXXSP has 6 timers: timer 1, timer 2, timer 3, timer 4, timer 5, and timer 6. All timers are 8-bit timers with the 8-bit timer latch. The timer block diagram is shown in Figure 17.

All of the timers count down and their divide ratio is  $1/(n+1)$ , where  $n$  is the value of timer latch. By writing a count value to the corresponding timer latch (addresses 00F0<sub>16</sub> to 00F3<sub>16</sub>: timers 1 to 4, addresses 00EE<sub>16</sub> and 00EF<sub>16</sub>: timers 5 and 6), the value is also set to a timer, simultaneously.

The count value is decremented by 1. The timer interrupt request bit is set to "1" by a timer overflow at the next count pulse, after the count value reaches "00<sub>16</sub>".

### (1) Timer 1

Timer 1 can select one of the following count sources:

- $f(X_{IN})/16$  or  $f(X_{CIN})/16$
- $f(X_{IN})/4096$  or  $f(X_{CIN})/4096$
- External clock from the TIM2 pin

The count source of timer 1 is selected by setting bits 5 and 0 of timer mode register 1 (address 00F4<sub>16</sub>). Either  $f(X_{IN})$  or  $f(X_{CIN})$  is selected by bit 7 of the CPU mode register.

Timer 1 interrupt request occurs at timer 1 overflow.

### (2) Timer 2

Timer 2 can select one of the following count sources:

- $f(X_{IN})/16$  or  $f(X_{CIN})/16$
- Timer 1 overflow signal
- External clock from the TIM2 pin

The count source of timer 2 is selected by setting bits 4 and 1 of timer mode register 1 (address 00F4<sub>16</sub>). Either  $f(X_{IN})$  or  $f(X_{CIN})$  is selected by bit 7 of the CPU mode register. When timer 1 overflow signal is a count source for the timer 2, the timer 1 functions as an 8-bit prescaler.

Timer 2 interrupt request occurs at timer 2 overflow.

### (3) Timer 3

Timer 3 can select one of the following count sources:

- $f(X_{IN})/16$  or  $f(X_{CIN})/16$
- $f(X_{CIN})$
- External clock from the TIM3 pin

The count source of timer 3 is selected by setting bit 0 of timer mode register 2 (address 00F5<sub>16</sub>) and bit 6 at address 00C7<sub>16</sub>. Either  $f(X_{IN})$  or  $f(X_{CIN})$  is selected by bit 7 of the CPU mode register.

Timer 3 interrupt request occurs at timer 3 overflow.

### (4) Timer 4

Timer 4 can select one of the following count sources:

- $f(X_{IN})/16$  or  $f(X_{CIN})/16$
- $f(X_{IN})/2$  or  $f(X_{CIN})/2$
- $f(X_{CIN})$

The count source of timer 3 is selected by setting bits 1 and 4 of the timer mode register 2 (address 00F5<sub>16</sub>). Either  $f(X_{IN})$  or  $f(X_{CIN})$  is selected by bit 7 of the CPU mode register. When timer 3 overflow signal is a count source for the timer 4, the timer 3 functions as an 8-bit prescaler.

Timer 4 interrupt request occurs at timer 4 overflow.

### (5) Timer 5

Timer 5 can select one of the following count sources:

- $f(X_{IN})/16$  or  $f(X_{CIN})/16$
- Timer 2 overflow signal
- Timer 4 overflow signal

The count source of timer 3 is selected by setting bit 6 of timer mode register 1 (address 00F4<sub>16</sub>) and bit 7 of the timer mode register 2 (address 00F5<sub>16</sub>). When overflow of timer 2 or 4 is a count source for timer 5, either timer 2 or 4 functions as an 8-bit prescaler. Either  $f(X_{IN})$  or  $f(X_{CIN})$  is selected by bit 7 of the CPU mode register.

Timer 5 interrupt request occurs at timer 5 overflow.

### (6) Timer 6

Timer 6 can select one of the following count sources:

- $f(X_{IN})/16$  or  $f(X_{CIN})/16$
- Timer 5 overflow signal

The count source of timer 6 is selected by setting bit 7 of the timer mode register 1 (address 00F4<sub>16</sub>). Either  $f(X_{IN})$  or  $f(X_{CIN})$  is selected by bit 7 of the CPU mode register. When timer 5 overflow signal is a count source for timer 6, the timer 5 functions as an 8-bit prescaler. Timer 6 interrupt request occurs at timer 6 overflow.

At reset, timers 3 and 4 are connected by hardware and "FF<sub>16</sub>" is automatically set in timer 3; "07<sub>16</sub>" in timer 4. The  $f(X_{IN})^*/16$  is selected as the timer 3 count source. The internal reset is released by timer 4 overflow in this state and the internal clock is connected.

At execution of the STP instruction, timers 3 and 4 are connected by hardware and "FF<sub>16</sub>" is automatically set in timer 3; "07<sub>16</sub>" in timer 4. However, the  $f(X_{IN})^*/16$  is not selected as the timer 3 count source. So set both bit 0 of timer mode register 2 (address 00F5<sub>16</sub>) and bit 6 at address 00C7<sub>16</sub> to "0" before the execution of the STP instruction ( $f(X_{IN})^*/16$  is selected as timer 3 count source). The internal STP state is released by timer 4 overflow in this state and the internal clock is connected.

As a result of the above procedure, the program can start under a stable clock.

\* : When bit 7 of the CPU mode register (CM7) is "1,"  $f(X_{IN})$  becomes  $f(X_{CIN})$ .

The timer-related registers is shown in Figure 15 and 16.

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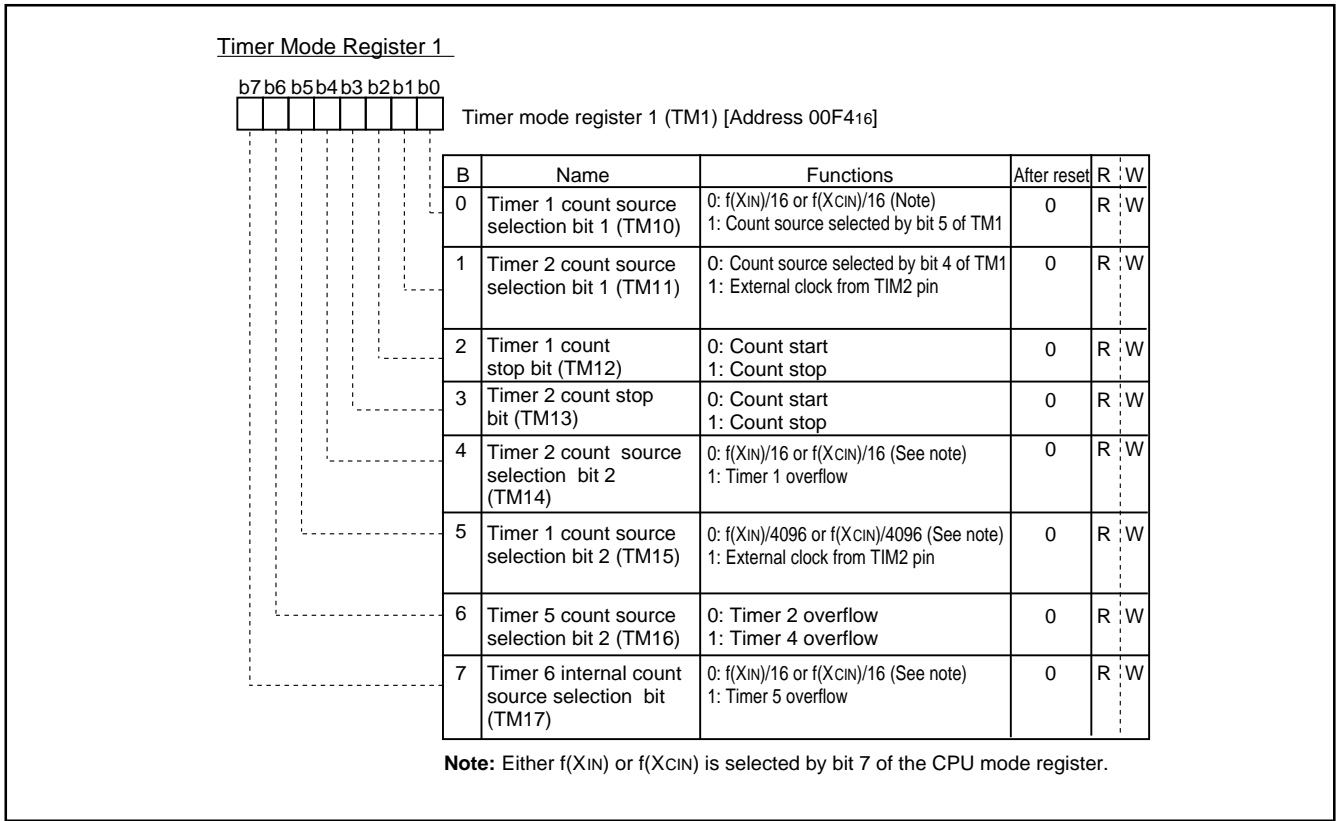


Fig. 15. Timer Mode Register 1

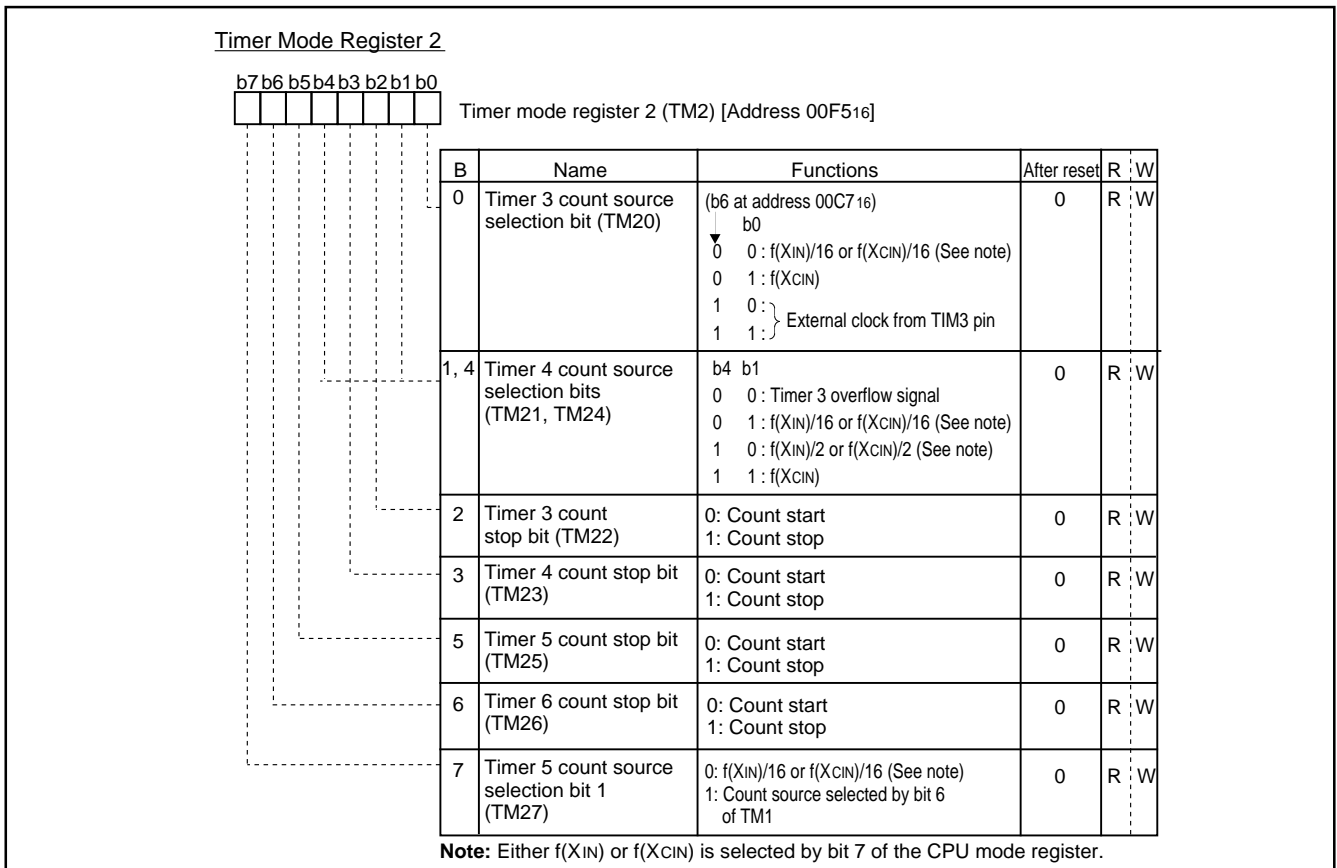


Fig. 16. Timer Mode Register 2

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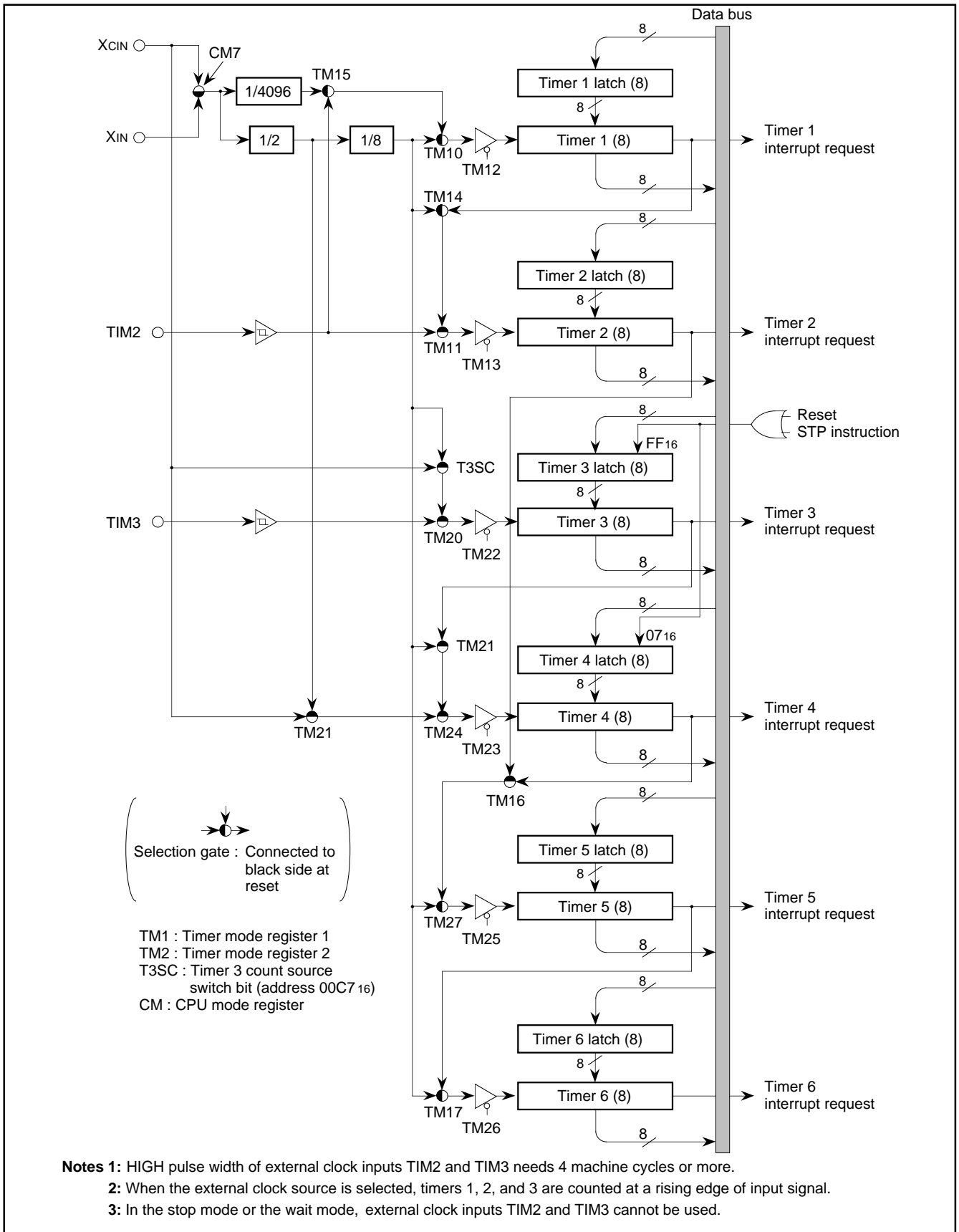


Fig. 17. Timer Block Diagram

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**SERIAL I/O**

The M37273MF-XXXSP has a built-in serial I/O which can either transmit or receive 8-bit data serially in the clock synchronous mode.

The serial I/O block diagram is shown in Figure 18. The synchronous clock I/O pin (SCLK), and data output pin (SOUT), data input pin (SIN) also functions as port P20, P21, P22 respectively.

Bit 2 of the serial I/O mode register (address 00EB16) selects whether the synchronous clock is supplied internally or externally (from the SCLK pin). When an internal clock is selected, bits 1 and 0 select whether  $f(XIN)$  or  $f(XCIN)$  is divided by 8, 16, 32, or 64. To use SOUT, SCLK, and SIN pins for serial I/O, set the corresponding bits of the port P2 direction register to "0."

The operation of the serial I/O is described below. The operation differs depending on the clock source; external clock or internal clock.

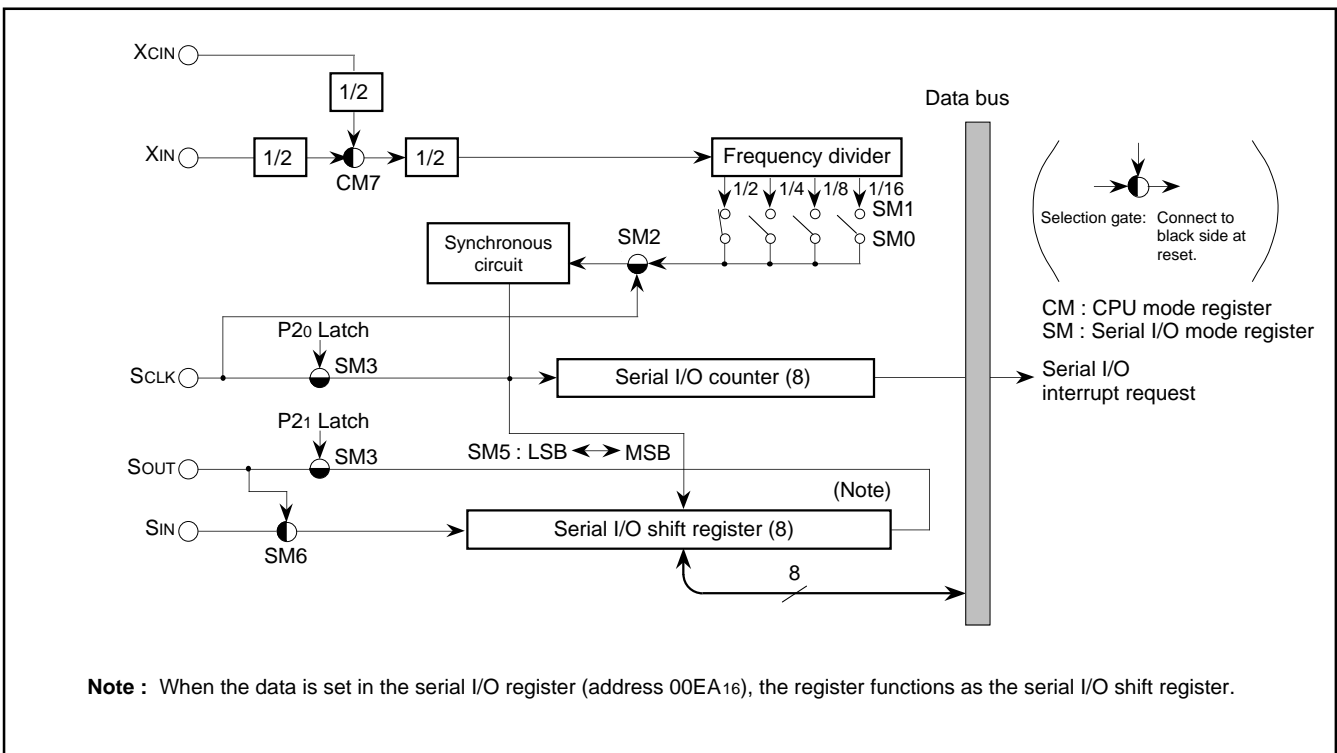


Fig. 18. Serial I/O Block Diagram

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Internal clock: The serial I/O counter is set to "7" during the write cycle into the serial I/O register (address 00EA16), and the transfer clock goes HIGH forcibly. At each falling edge of the transfer clock after the write cycle, serial data is output from the SOUT pin. Transfer direction can be selected by bit 5 of the serial I/O mode register. At each rising edge of the transfer clock, data is input from the SIN pin and data in the serial I/O register is shifted 1 bit.

After the transfer clock has counted 8 times, the serial I/O counter becomes "0" and the transfer clock stops at HIGH. At this time the interrupt request bit is set to "1."

External clock: When an external clock is selected as the clock source, the interrupt request is set to "1" after the transfer clock has been counted 8 counts. However, transfer operation does not stop, so the clock should be controlled externally. Use the external clock of 500kHz or less with a duty cycle of 50%.

The serial I/O timing is shown in Figure 19. When using an external clock for transfer, the external clock must be held at HIGH for initializing the serial I/O counter. When switching between an internal clock and an external clock, do not switch during transfer. Also, be sure to initialize the serial I/O counter after switching.

- Notes 1:** On programming, note that the serial I/O counter is set by writing to the serial I/O register with the bit managing instructions, such as SEB and CLB.
- 2:** When an external clock is used as the synchronous clock, write transmit data to the serial I/O register when the transfer clock input level is HIGH.

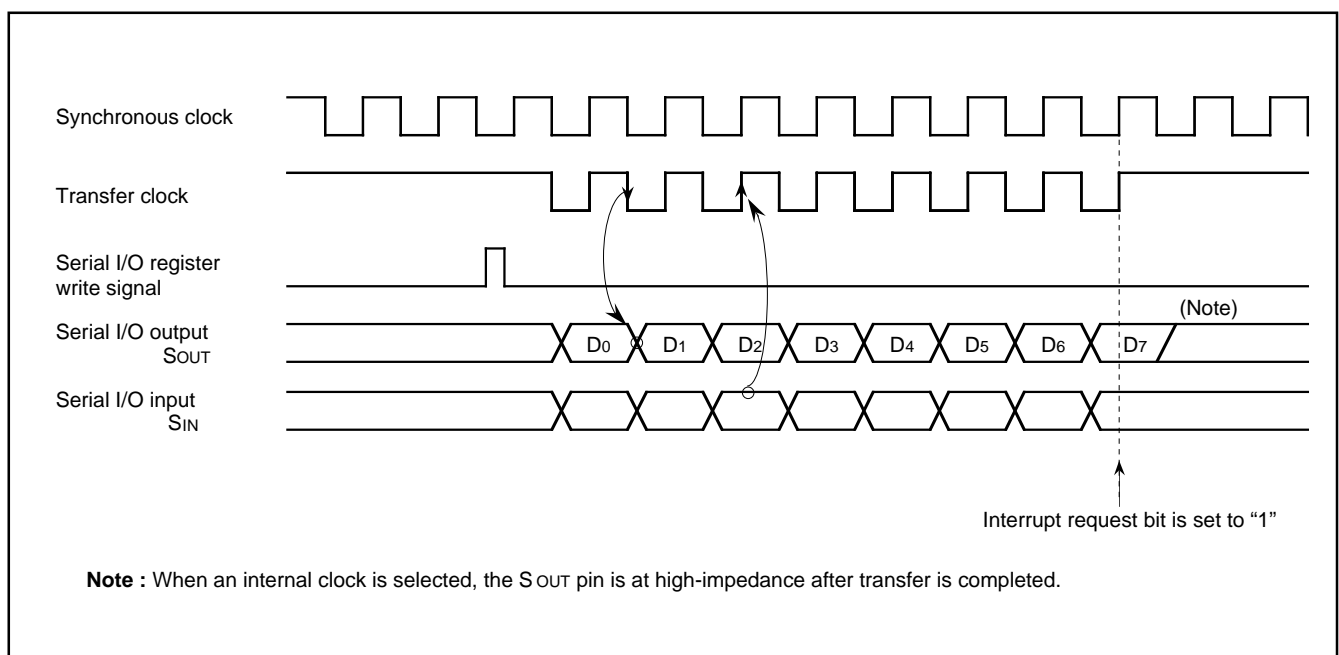
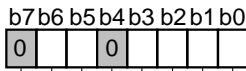


Fig. 19. Serial I/O Timing (for LSB first)

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Serial I/O Mode Register



Serial I/O mode register (SM) [Address 00EB16]

B	Name	Functions	After reset	R	W
0, 1	Internal synchronous clock selection bits (SM0, SM1)	b1 b0 0 0: f(X <sub>IN</sub> )/4 or f(X <sub>CIN</sub> )/4 0 1: f(X <sub>IN</sub> )/16 or f(X <sub>CIN</sub> )/16 1 0: f(X <sub>IN</sub> )/32 or f(X <sub>CIN</sub> )/32 1 1: f(X <sub>IN</sub> )/64 or f(X <sub>CIN</sub> )/64	0	R	W
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R	W
3	Port function selection bit (SM3)	0: P2 <sub>0</sub> , P2 <sub>1</sub> 1: SCLK, SOUT	0	R	W
4, 7	Fix these bits to "0."		0	R	W
5	Transfer direction selection bit (SM5)	0: LSB first 1: MSB first	0	R	W
6	Transfer clock input pin selection bit (SM6)	0: Input signal from S <sub>IN</sub> pin 1: Input signal from S <sub>OUT</sub> pin	0	R	W

Fig. 20. Serial I/O Mode Register



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## PWM OUTPUT FUNCTION

The M37273MF-XXXSP is equipped with six 8-bit PWMs (PWM0–PWM5). PWM0–PWM5 have the same circuit structure and an 8-bit resolution with minimum resolution bit width of 4  $\mu$ s (for  $f(X_{IN}) = 8$  MHz) and repeat period of 1024  $\mu$ s (for  $f(X_{IN}) = 8$  MHz).

Figure 21 shows the PWM block diagram. The PWM timing generating circuit applies individual control signals to PWM0–PWM5 using  $f(X_{IN})$  divided by 2 as a reference signal.

### (1) Data Setting

When outputting PWM0–PWM5, set 8-bit output data to the PWM $i$  register ( $i$  means 0 to 5; addresses 0200<sub>16</sub> to 0205<sub>16</sub>).

### (2) Transmitting Data from Register to PWM circuit

Data transfer from the 8-bit PWM register to the 8-bit PWM circuit is executed at writing data to the register.

The signal output from the 8-bit PWM output pin corresponds to the contents of this register.

### (3) Operating of 8-bit PWM

The following explains PWM operation.

First, set the bit 0 of PWM mode register 1 (address 0208<sub>16</sub>) to “0” (at reset, bit 0 is already set to “0” automatically), so that the PWM count source is supplied.

PWM0–PWM5 are also used as pins P00–P05. Set the corresponding bits of the port P0 direction register to “1” (output mode). And select each output polarity by bit 3 of PWM mode register 1 (address 0208<sub>16</sub>). Then, set bits 5 to 0 of PWM mode register 2 (address 0209<sub>16</sub>) to “1” (PWM output).

The PWM waveform is output from the PWM output pins by setting these registers.

Figure 22 shows the 8-bit PWM timing. One cycle ( $T$ ) is composed of 256 ( $2^8$ ) segments. The 8 kinds of pulses relative to the weight of each bit (bits 0 to 7), are output inside the circuit during 1 cycle. Refer to Figure 22 (a). The 8-bit PWM outputs waveform which is the logical sum (OR) of pulses corresponding to the contents of bits 0 to 7 of the 8-bit PWM register. Several examples are shown in Figure 22 (b). 256 kinds of output (HIGH area: 0/256 to 255/256) are selected by changing the contents of the PWM register. A length of entirely HIGH cannot be output, i.e. 256/256.

### (4) Output after Reset

At reset, the output of ports P00–P05 is in the high-impedance state, and the contents of the PWM register and the PWM circuit are undefined. Note that after reset, the PWM output is undefined until setting the PWM register.

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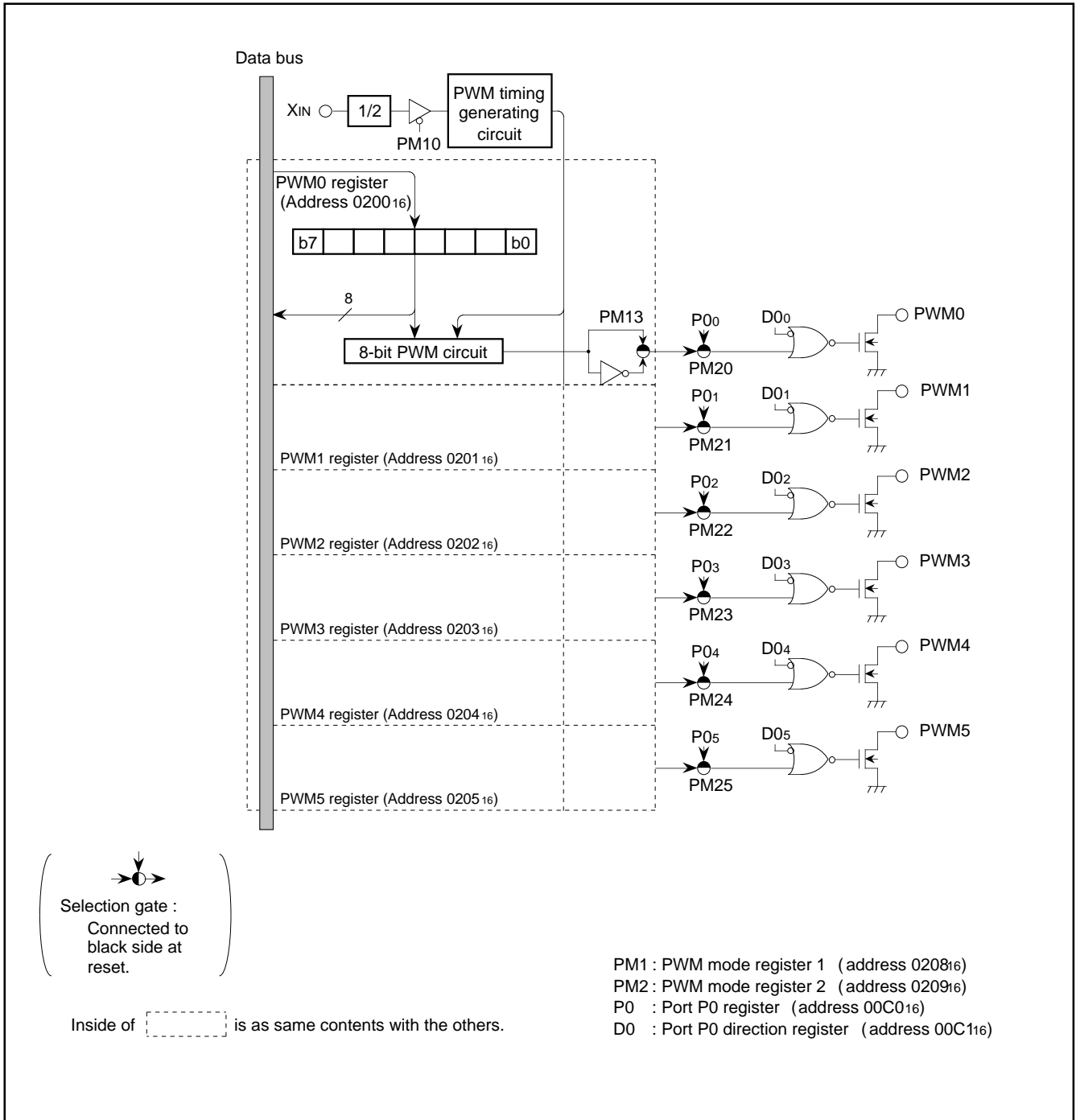


Fig. 21. PWM Block Diagram

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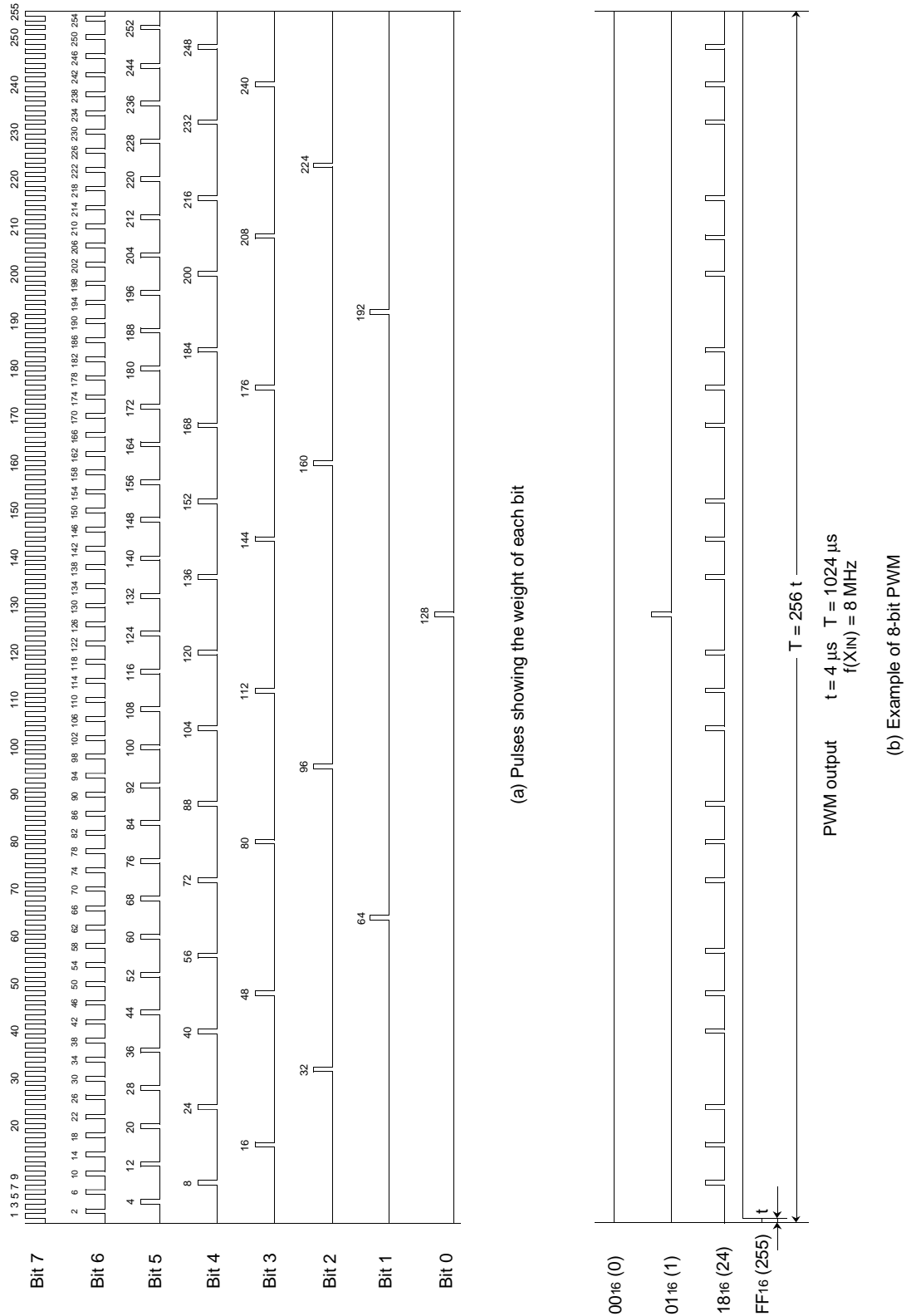
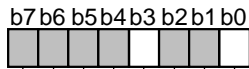


Fig. 22. 8-bit PWM Timing

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PWM Mode Register 1

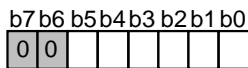


PWM mode register 1 (PM1) [Address 020816]

B	Name	Functions	After reset	R	W
0	PWM counts source selection bit (PM10)	0 : Count source supply 1 : Count source stop	0	R	W
1, 2 4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		Indeterminate	R	—
3	PWM output polarity selection bit (PM13)	0 : Positive polarity 1 : Negative polarity	0	R	W

Fig. 23. PWM Mode Register 1

PWM Mode Register 2



PWM mode register 2 (PM2) [Address 020916]

B	Name	Functions	After reset	R	W
0	P00/PWM0 output selection bit (PM20)	0 : P00 output 1 : PWM0 output	0	R	W
1	P01/PWM1 output selection bit (PM21)	0 : P01 output 1 : PWM1 output	0	R	W
2	P02/PWM2 output selection bit (PM22)	0 : P02 output 1 : PWM2 output	0	R	W
3	P03/PWM3 output selection bit (PM23)	0 : P03 output 1 : PWM3 output	0	R	W
4	P04/PWM4 output selection bit (PM24)	0 : P04 output 1 : PWM4 output	0	R	W
5	P05/PWM5 output selection bit (PW25)	0 : P05 output 1 : PWM5 output	0	R	W
6, 7	Fix these bits to "0."		0	R	W

Fig. 24. PWM Mode Register 2

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**A-D COMPARATOR**

A-D comparator consists of 6-bit D-A converter and comparator. A-D comparator block diagram is shown in Figure 25.

The reference voltage "V<sub>ref</sub>" for D-A conversion is set by bits 0 to 5 of the A-D control register 2 (address 00ED16).

The comparison result of the analog input voltage and the reference voltage "V<sub>ref</sub>" is stored in bit 4 of the A-D control register (address 00EC16).

For A-D comparison, set "0" to corresponding bits of the direction register to use ports as analog input pins. Write the data for select of analog input pins to bits 0 to 2 of the A-D control register 1 and write the digital value corresponding to V<sub>ref</sub> to be compared to the bits 0 to 5 A-D control register 2. The voltage comparison starts by writing to the A-D control register 2, and it is completed after 16 machine cycles (NOP instruction X 8).

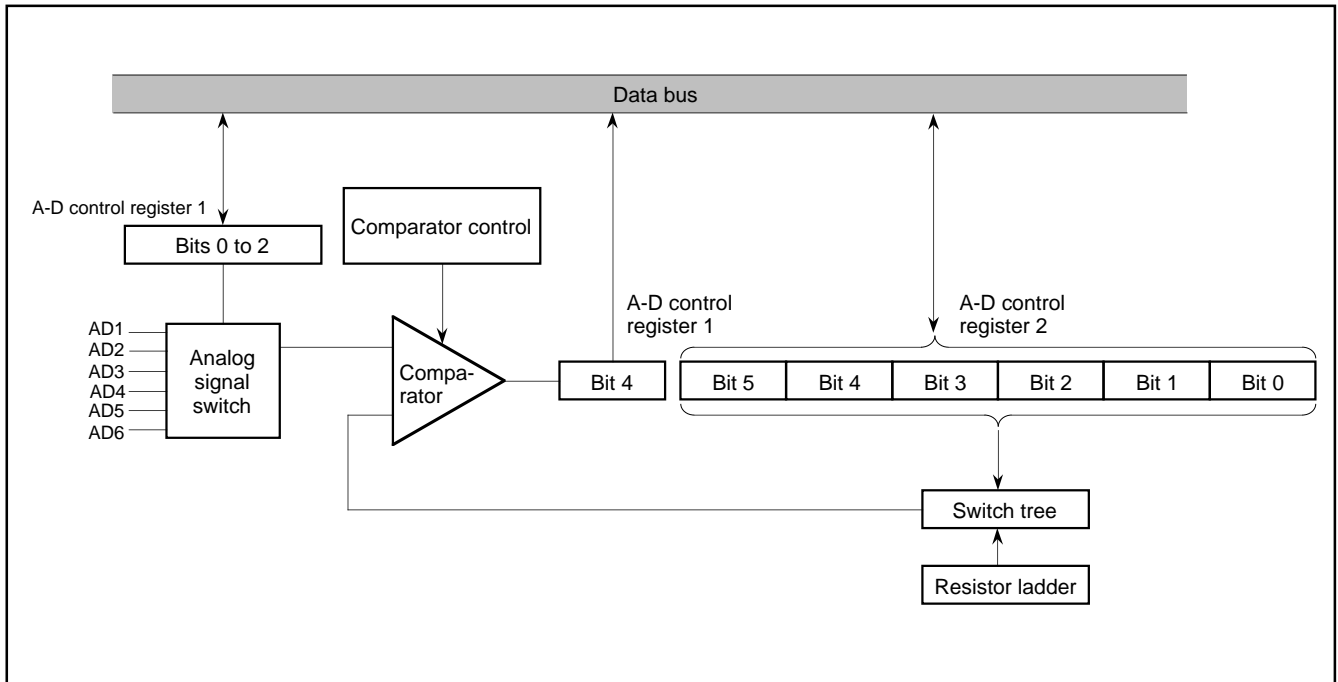


Fig. 25. A-D Comparator Block Diagram

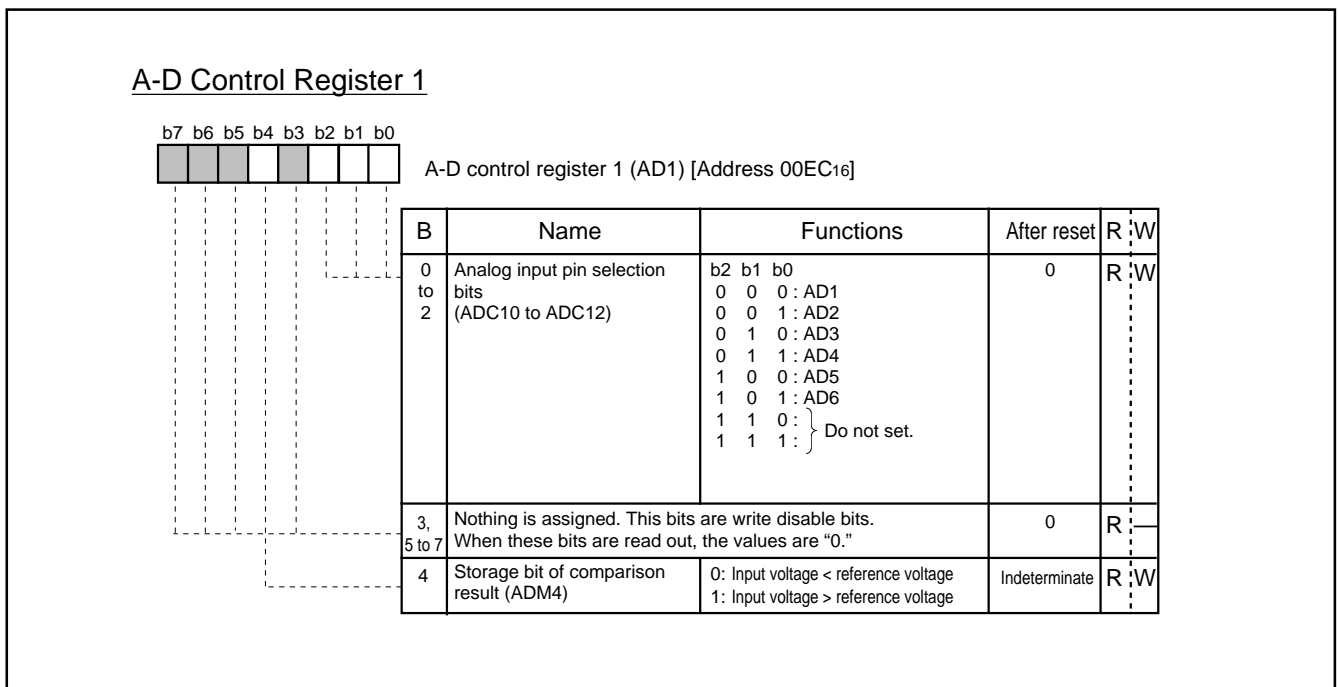


Fig. 26. A-D Control Register 1

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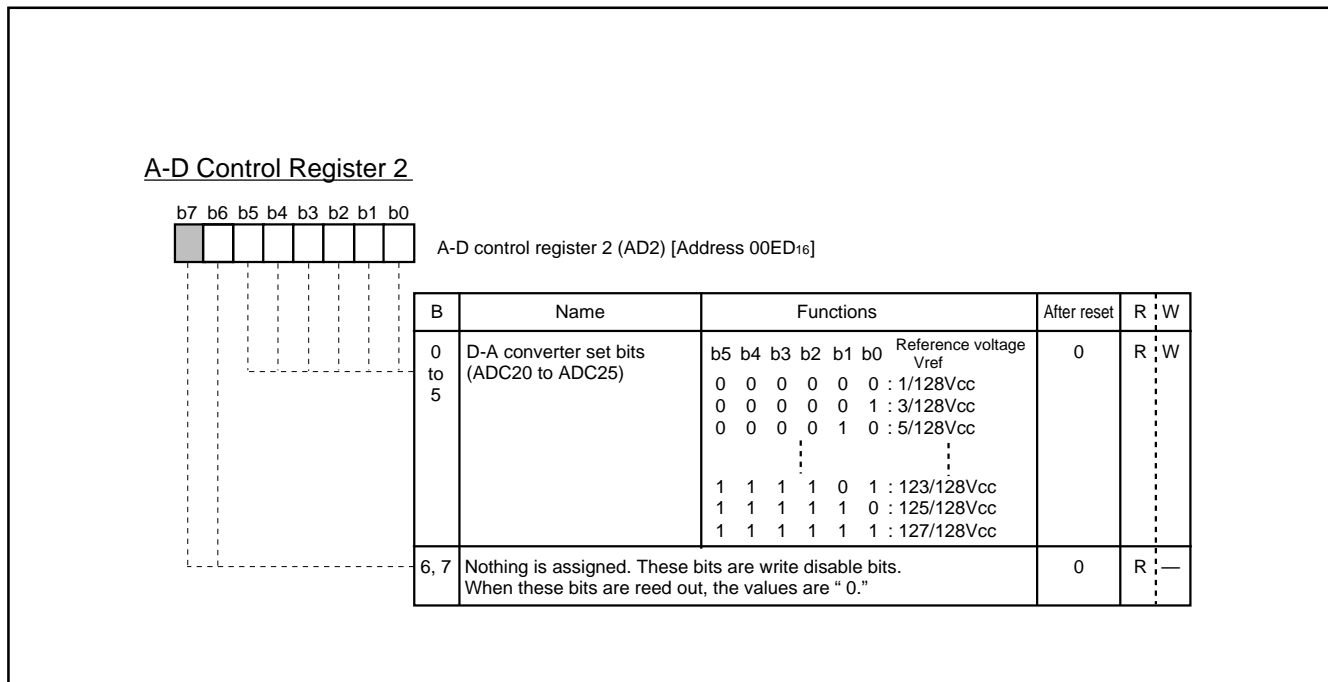


Fig. 27. A-D Control Register 2

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## DATA SLICER

The M37273MF-XXXSP includes the data slicer function for the closed caption decoder (referred to as the CCD). This function takes out the caption data superimposed in the vertical blanking interval of a composite video signal. A composite video signal which makes the sync chip's polarity negative is input to the CV<sub>IN</sub> pin.

When the data slicer function is not used, the data slicer circuit and the timing signal generating circuit can be cut off by setting bit 0 of the data slicer control register 1 (address 00E0<sub>16</sub>) to "0." These settings can realize the low-power dissipation.

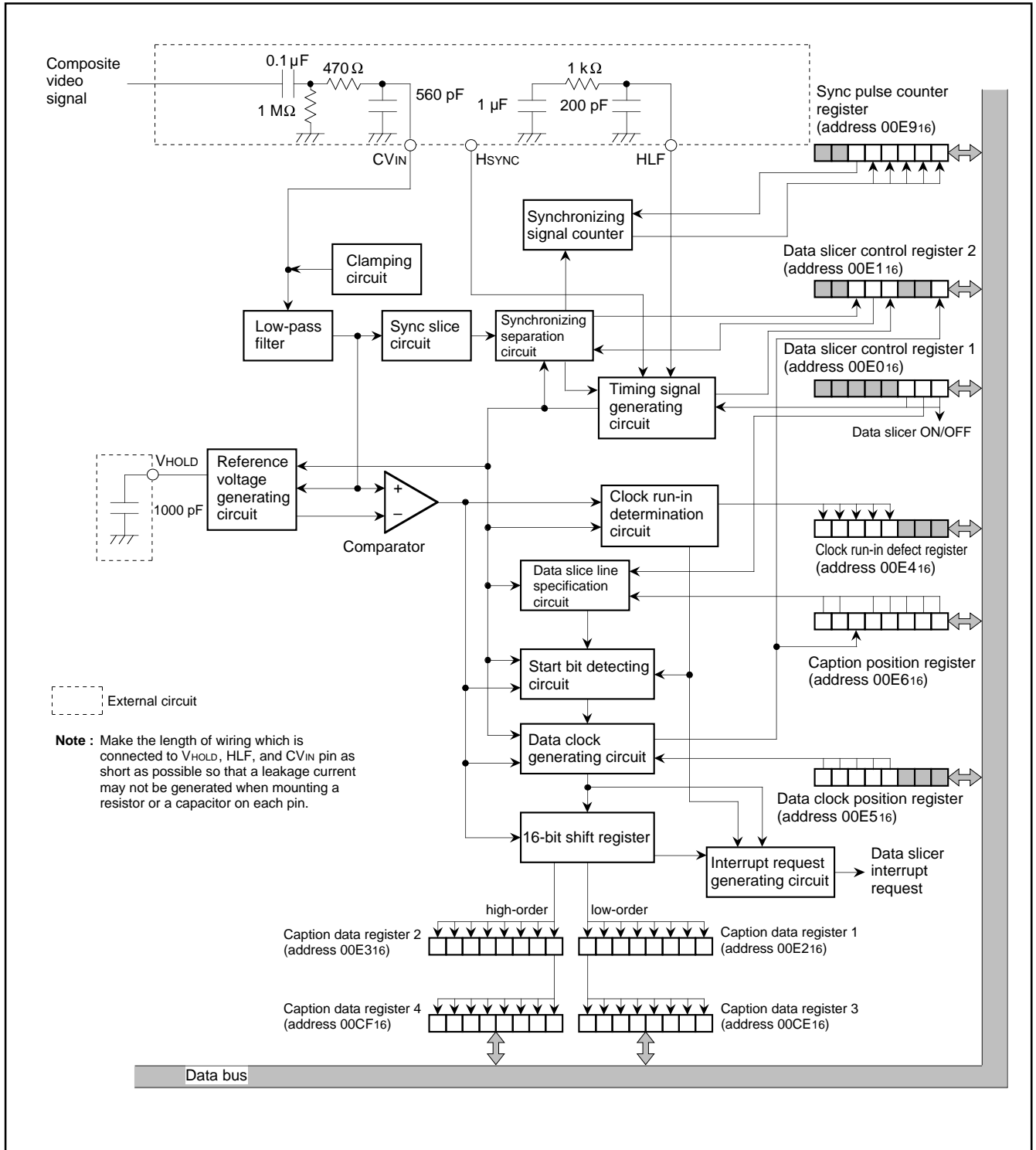


Fig. 28. Data Slicer Block Diagram

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**(1) Notes When not Using Data Slicer**

When bit 0 of data slicer control register 1 (address 00E016) is "0," terminate the pins as shown in Figure 29.

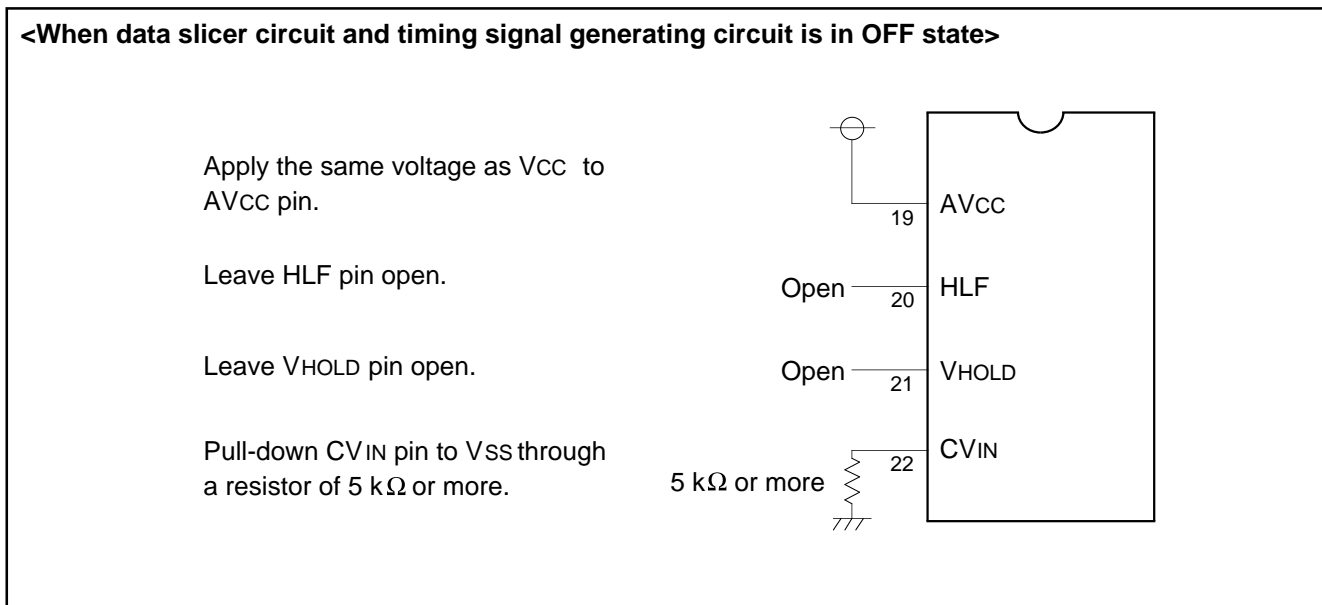


Fig. 29. Termination of Data Slicer Input/Output Pins when Data Slicer Circuit and Timing Generating Circuit Is in OFF State

When both bits 0 and 2 of data slicer control register 1 (address 00E016) are "1," terminate the pins as shown in Figure 30.

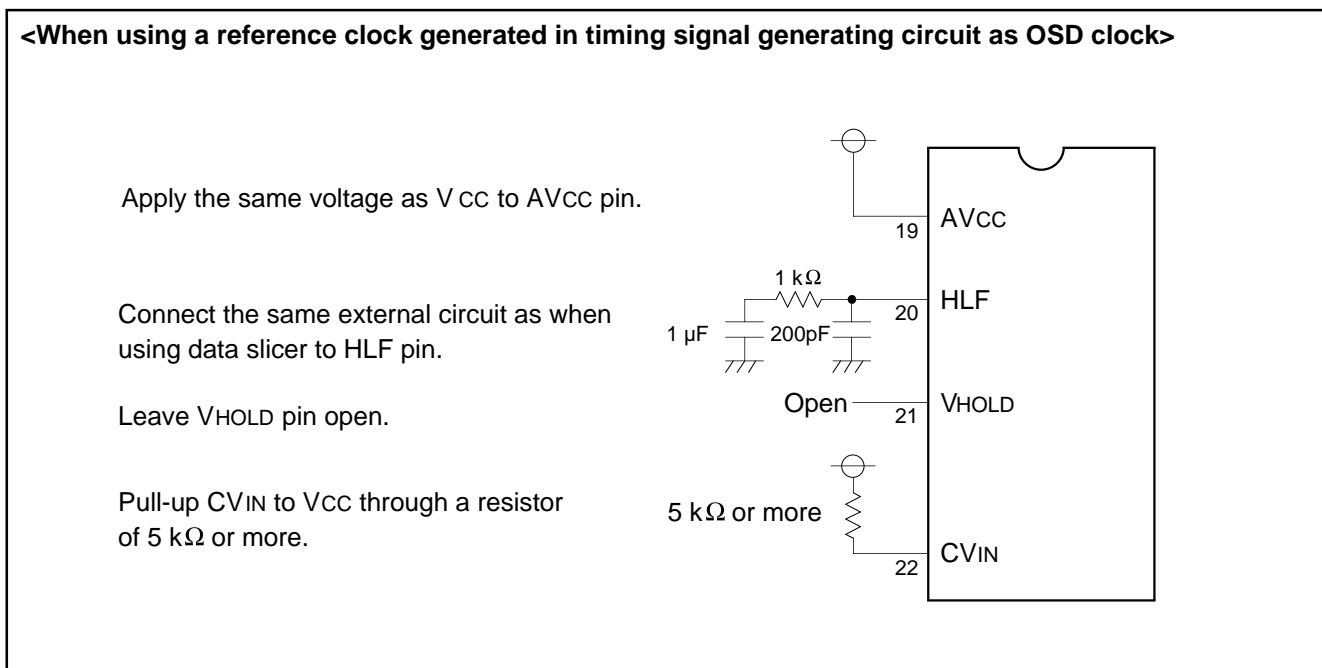


Fig. 30. Termination of Data Slicer Input/Output Pins when Timing Signal Generating Circuit Is in ON State



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Figure 31 shows the structure of the data slicer control registers.

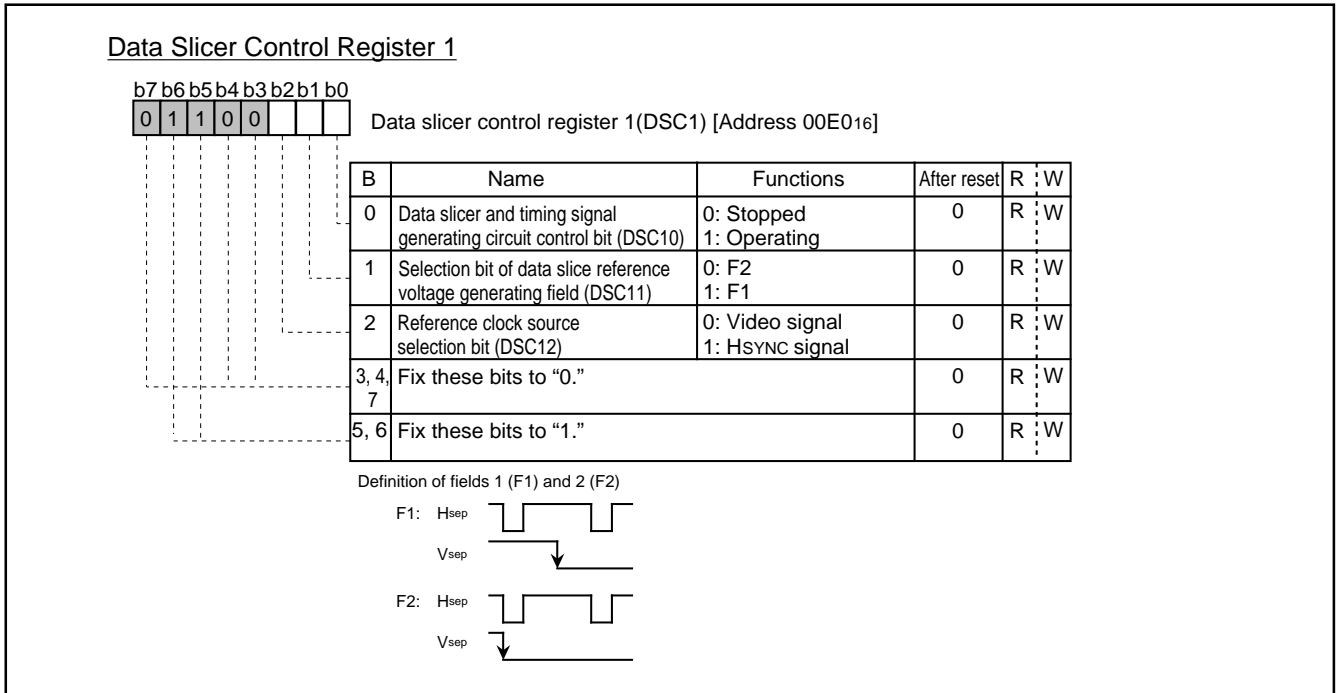


Fig. 31. Data Slicer Control Register 1

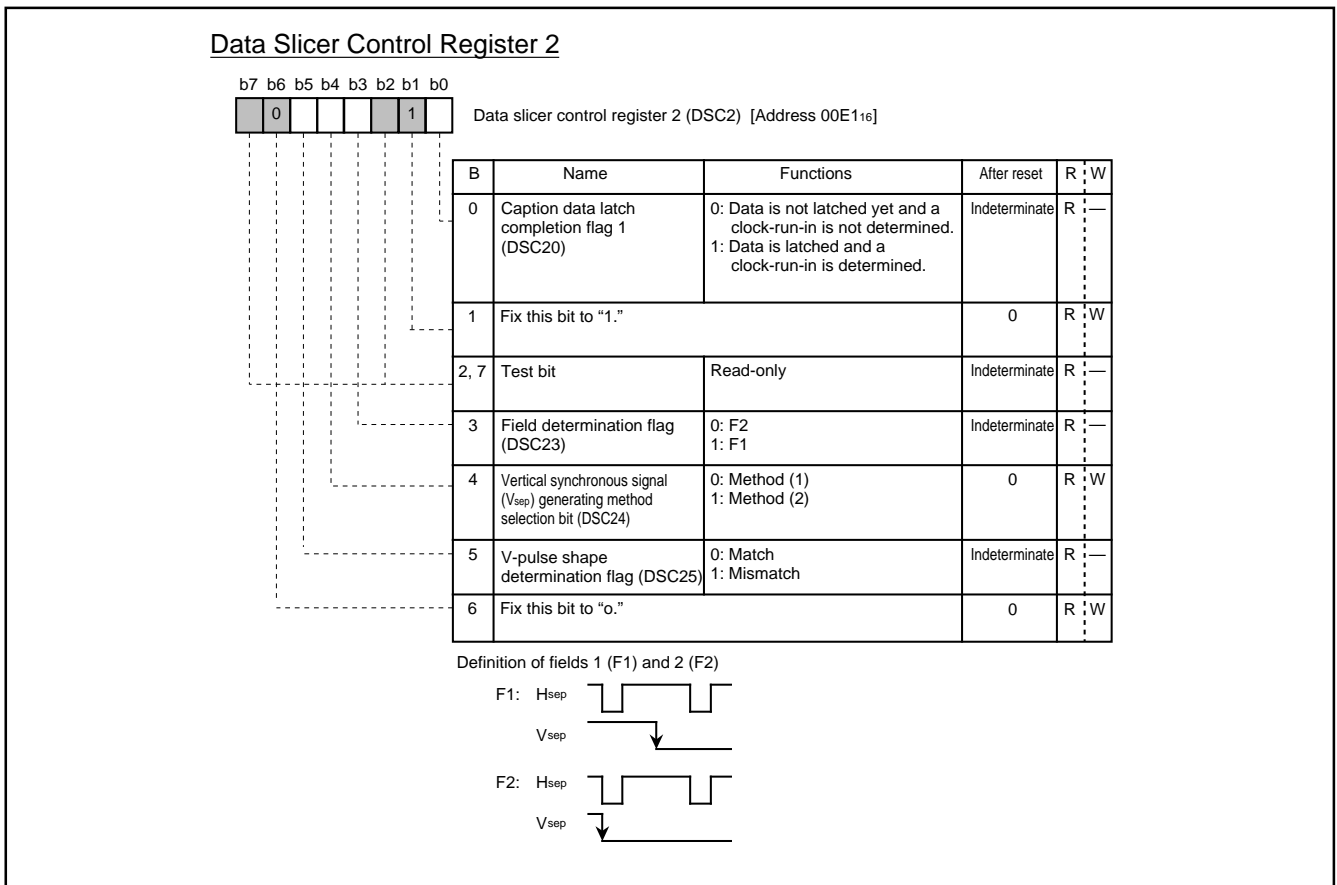


Fig. 32. Data Slicer Control Register 2

## (2) Clamping Circuit and Low-pass Filter

The clamp circuit clamps the sync chip part of the composite video signal input from the CV<sub>IN</sub> pin. The low-pass filter attenuates the noise of clamped composite video signal. The CV<sub>IN</sub> pin to which composite video signal is input requires a capacitor (0.1  $\mu$ F) coupling outside. Pull down the CV<sub>IN</sub> pin with a resistor of hundreds of kilohms to 1 M $\Omega$ . In addition, we recommend to install externally a simple low-pass filter using a resistor and a capacitor at the CV<sub>IN</sub> pin (refer to Figure 28).

## (3) Sync Slice Circuit

This circuit takes out a composite sync signal from the output signal of the low-pass filter.

## (4) Synchronous Signal Separation Circuit

This circuit separates a horizontal synchronous signal and a vertical synchronous signal from the composite sync signal taken out in the sync slice circuit.

### ① Horizontal Synchronous Signal (H<sub>sep</sub>)

A one-shot horizontal synchronizing signal H<sub>sep</sub> is generated at the falling edge of the composite sync signal.

### ② Vertical Synchronous Signal (V<sub>sep</sub>)

As a V<sub>sep</sub> signal generating method, it is possible to select one of the following 2 methods by using bit 4 of the data slicer control register 2 (address 00E1<sub>16</sub>).

- Method 1 The "L" level width of the composite sync signal is measured. If this width exceeds a certain time, a V<sub>sep</sub> signal is generated in synchronization with the rising of the timing signal immediately after this "L" level.
- Method 2 The "L" level width of the composite sync signal is measured. If this width exceeds a certain time, it is detected whether a falling of the composite sync signal exits or not in the "L" level period of the timing signal immediately after this "L" level. If a falling exists, a V<sub>sep</sub> signal is generated in synchronization with the rising of the timing signal (refer to Figure 33).

Figure 33 shows a V<sub>sep</sub> generating timing. The timing signal shown in the figure is generated from the reference clock which the timing generating circuit outputs.

Reading bit 5 of data slicer control register 2 permits determining the shape of the V-pulse portion of the composite sync signal. As shown in Figure 34, when the A level matches the B level, this bit is "0." In the case of a mismatch, the bit is "1."

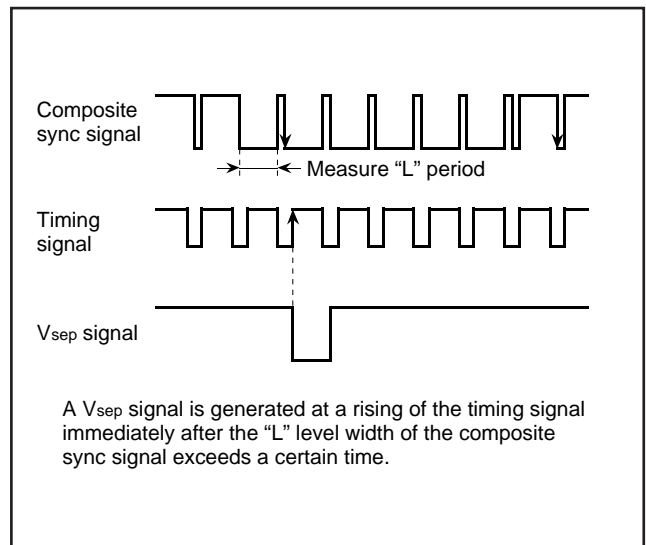


Fig. 33. Vsep Generating Timing (method 2)

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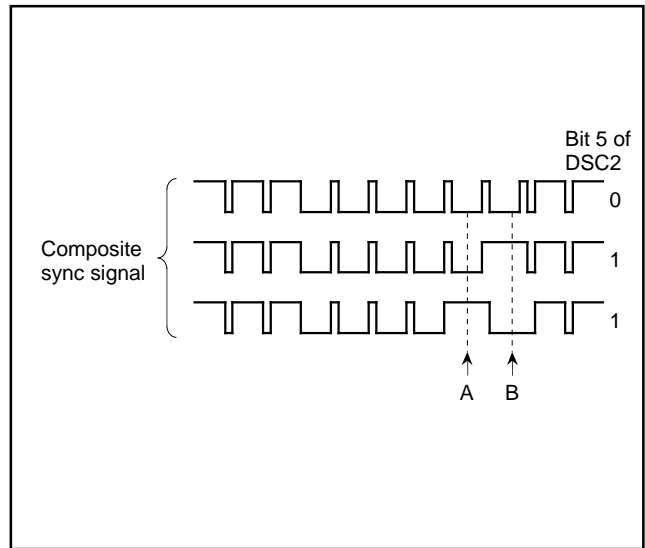
**(5) Timing Signal Generating Circuit**

This circuit generates a reference clock which is 832 times as large as the horizontal synchronous signal frequency. It also generates various timing signals on the basis of the reference clock, horizontal synchronous signal and vertical synchronizing signal. The circuit operates by setting bit 0 of data slicer control register 1 (address 00E0<sub>16</sub>) to "1."

The reference clock can be used as a display clock for OSD function in addition to the data slicer. The H<sub>SYNC</sub> signal can be used as a count source instead of the composite sync signal. However, when the H<sub>SYNC</sub> signal is selected, the data slicer cannot be used. A count source of the reference clock can be selected by bit 2 of data slicer control register 1 (address 00E0<sub>16</sub>).

For the pins HLF, connect a resistor and a capacitor as shown in Figure 28. Make the length of wiring which is connected to these pins as short as possible so that a leakage current may not be generated.

**Note:** It takes a few tens of milliseconds until the reference clock becomes stable after the data slicer and the timing signal generating circuit are started. In this period, various timing signals, H<sub>sep</sub> signals and V<sub>sep</sub> signals become unstable. For this reason, take stabilization time into consideration when programming.



**Fig. 34. Determination of V-pulse Waveform**

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**(6) Data Slice Line Specification Circuit**

① Specification of Data Slice Line

This circuit decides a line on which caption data is superimposed. The line 21 (fixed), 1 appropriate line for a period of 1 field (total 2 line for a period of 1 field), and both fields (F1 and F2) are sliced their data. The caption position register (address 00E616) is used for each setting (refer to Table 3).

The counter is reset at the falling edge of  $V_{sep}$  and is incremented by 1 every  $H_{sep}$  pulse. When the counter value matched the value specified by bits 4 to 0 of the caption position register, this  $H_{sep}$  is sliced.

The values of "0016" to "1F16" can be set in the caption position register (at setting only 1 appropriate line). Figure 35 shows the signals in the vertical blanking interval. Figure 36 shows the structure of the caption position register.

② Specification of Line to Set Slice Voltage

The reference voltage for slicing (slice voltage) is generated for the clock run-in pulse in the particular line (refer to Table 2). The field to generate slice voltage is specified by bit 1 of data slicer control register 1. The line to generate slice voltage 1 field is specified by bits 6, 7 of the caption position register (refer to Table 2).

③ Field Determination

The field determination flag can be read out by bit 3 of data slicer control register 2. This flag charge at the falling edge of  $V_{sep}$ .

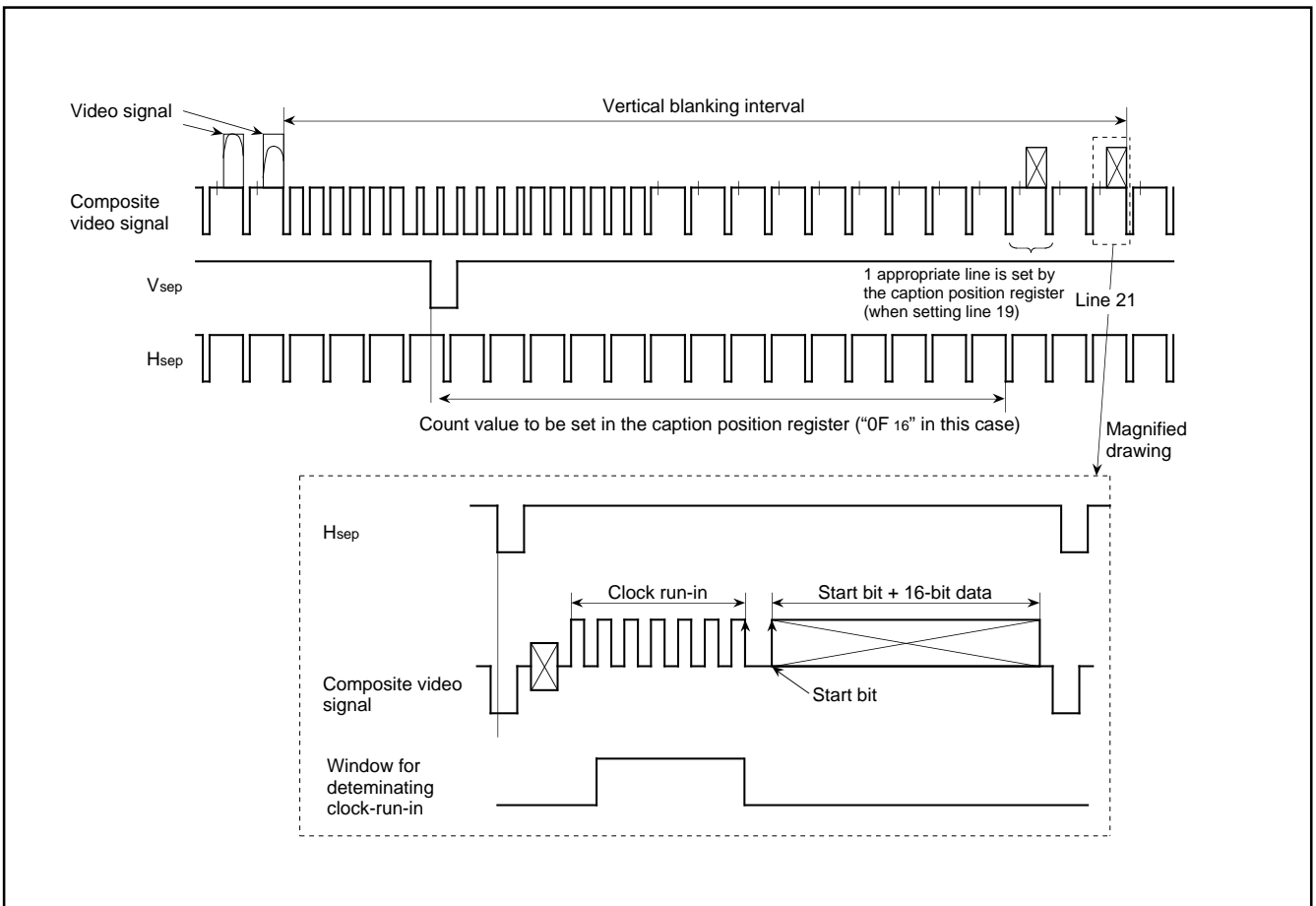


Fig. 35. Signals in Vertical Blanking Interval

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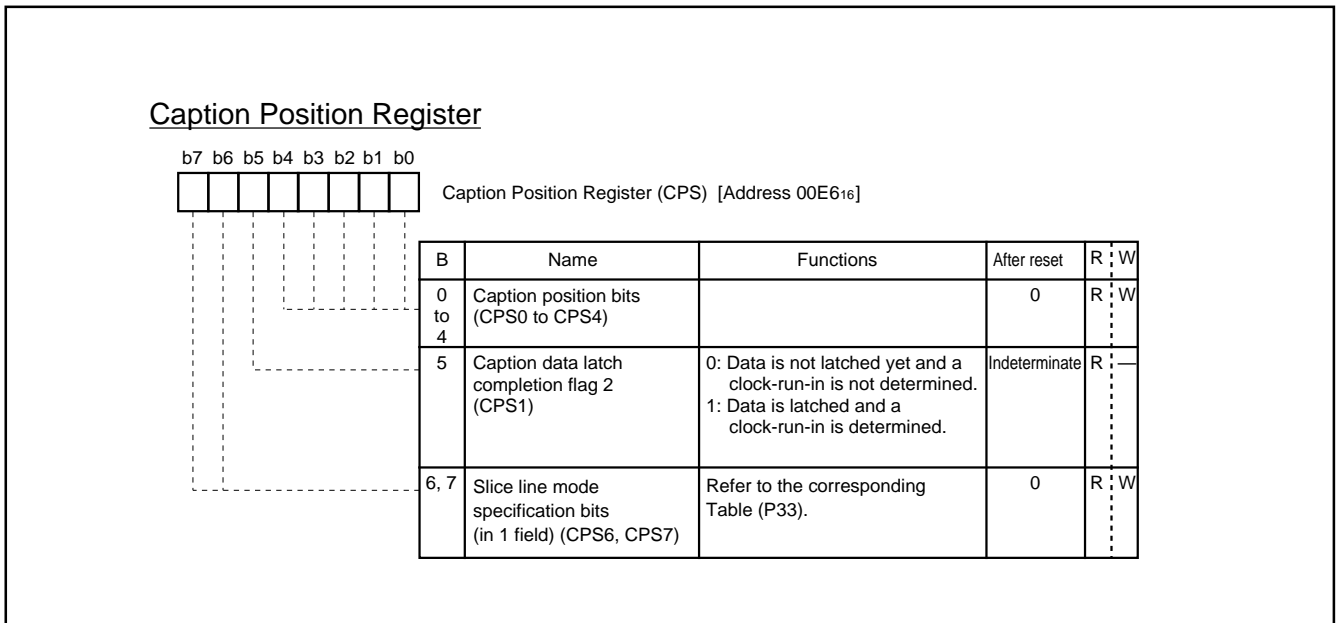


Fig. 36. Caption Position Register

Table 2. Specification of Data Slice Line

CPS		Field and Line to Be Sliced Data	Field and Line to Generate Slice Voltage
b7	b6		
0	0	<ul style="list-style-type: none"> <li>• Both fields of F1 and F2</li> <li>• Line 21 and a line specified by bits 4 to 0 of CPS (total 2 lines) (See note 2)</li> </ul>	<ul style="list-style-type: none"> <li>• Field specified by bit 1 of DSC1</li> <li>• Line 21 (total 1 line)</li> </ul>
0	1	<ul style="list-style-type: none"> <li>• Both fields of F1 and F2</li> <li>• A line specified by bits 4 to 0 of CPS (total 1 line) (See note 3)</li> </ul>	<ul style="list-style-type: none"> <li>• Field specified by bit 1 of DSC1</li> <li>• A line specified by bits 4 to 0 of CPS (total 1 line) (See note 3)</li> </ul>
1	0	<ul style="list-style-type: none"> <li>• Both fields of F1 and F2</li> <li>• Line 21 (total 1 line)</li> </ul>	<ul style="list-style-type: none"> <li>• Field specified by bit 1 of DSC1</li> <li>• Line 21 (total 1 line)</li> </ul>
1	1	<ul style="list-style-type: none"> <li>• Both fields of F1 and F2</li> <li>• Line 21 and a line specified by bits 4 to 0 of CPS (total 2 lines) (See note 2)</li> </ul>	<ul style="list-style-type: none"> <li>• Field specified by bit 1 of DSC1</li> <li>• Line 21 and a line specified by bits 4 to 0 of CPS (total 2 lines) (See note 2)</li> </ul>

Notes 1: DSC is data slicer control register 1.

CPS is caption position register.

2: Set "00<sub>16</sub>" to "1D<sub>16</sub>" to bits 4 to 0 of CPS.

3: Set "00<sub>16</sub>" to "1F<sub>16</sub>" to bits 4 to 0 of CPS.

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**(7) Reference Voltage Generating Circuit and Comparator**

The composite video signal clamped by the clamping circuit is input to the reference voltage generating circuit and the comparator.

① Reference Voltage Generating Circuit

This circuit generates a reference voltage (slice voltage) by using the amplitude of the clock run-in pulse in line specified by the data slice line specification circuit. Connect a capacitor between the V<sub>HOLD</sub> pin and the V<sub>SS</sub> pin, and make the length of wiring as short as possible so that a leakage current may not be generated.

② Comparator

The comparator compares the voltage of the composite video signal with the voltage (reference voltage) generated in the reference voltage generating circuit, and converts the composite video signal into a digital value.

**(8) Start Bit Detecting Circuit**

This circuit detects a start bit at line decided in the data slice line specification circuit.

The detection of a start bit is described below.

- ① A sampling clock is generated by dividing the reference clock output by the timing signal.
- ② A clock run-in pulse is detected by the sampling clock.
- ③ After detection of the pulse, a start bit pattern is detected from the comparator output.

**(9) Clock run-in Determination Circuit**

This circuit determinates clock run-in by counting the number of pulses in a window of the composite video signal.

The reference clock count value in one pulse cycle is stored in bits 3 to 7 of the clock run-in detect register (address 00E4<sub>16</sub>). Read out these bits after the occurrence of a data slicer interrupt (refer to (12) Interrupt Request Generating Circuit).

Figure 37 shows the structure of clock run-in detect register.

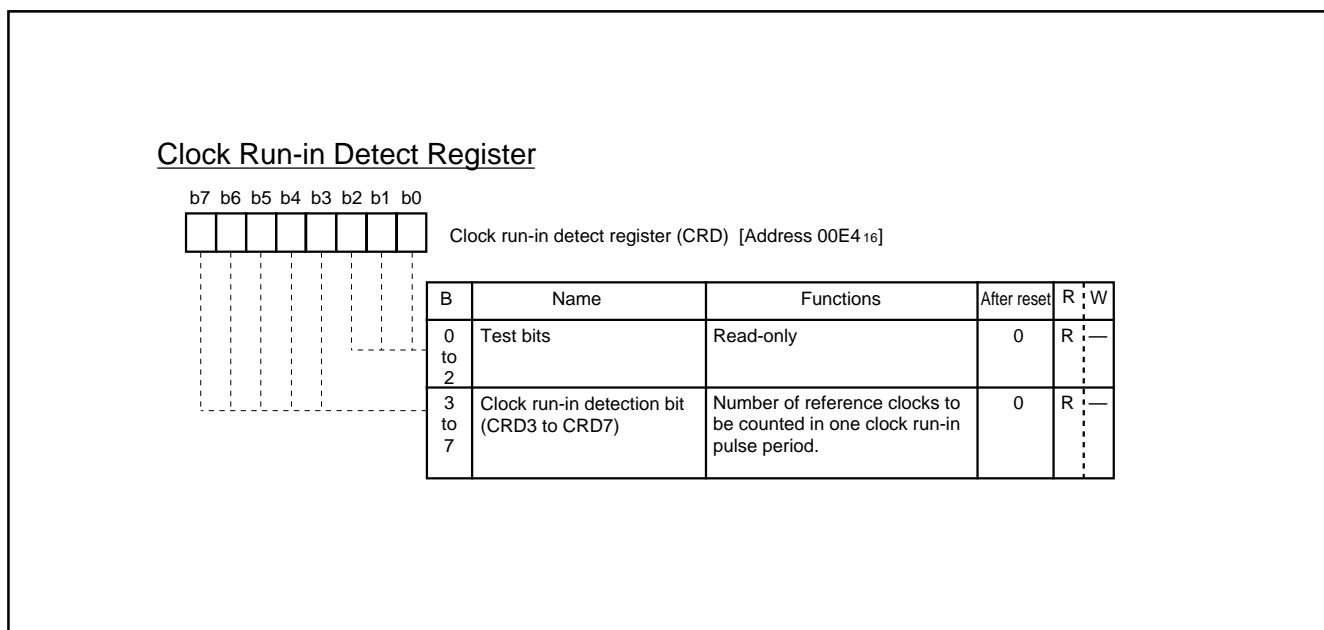


Fig. 37. Clock Run-in Detect Register

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**(10) Data clock generating circuit**

This circuit generates a data clock synchronized with the start bit detected in the start bit detecting circuit. The data clock stores caption data to the 16-bit shift register. When the 16-bit data has been stored and the clock run-in determination circuit determines clock run-in, the caption data latch completion flag is set. This flag is reset at a falling of the vertical synchronous signal (Vsep).

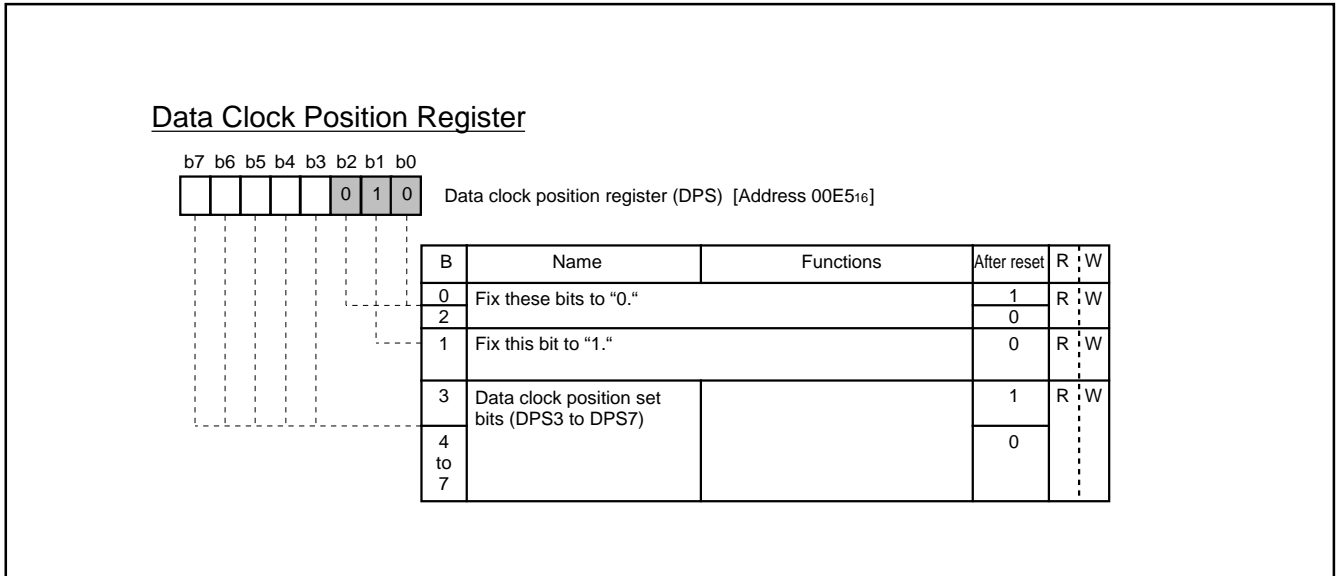


Fig. 38. Data Clock Position Register

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**(11) 16-bit Shift Register**

The caption data converted into a digital value by the comparator is stored into the 16-bit shift register in synchronization with the data clock. The contents of the high-order 8 bits of the stored caption data can be obtained by reading out data register 2 (address 00E3<sub>16</sub>) and data register 4 (address 00CF<sub>16</sub>). The contents of the low-order 8 bits can be obtained by reading out data register 1 (address 00E2<sub>16</sub>) and data register 3 (address 00CE<sub>16</sub>), respectively. These registers are reset to "0" at a falling of V<sub>sep</sub>. Read out data registers 1 and 2 after the occurrence of a data slicer interrupt (refer to (12) Interrupt Request Generating Circuit).

**(12) Interrupt Request Generating Circuit**

The interrupt requests as shown in Table 4 are generated by combination of the following bits; bits 6 and 7 of the caption position register (address 00E6<sub>16</sub>). Read out the contents of data registers 1 to 4 and the contents of bits 3 to 7 of the clock run-in detect register after the occurrence of a data slicer interrupt request.

**Table 3. Contents of Caption Data Latch Completion Flag and 16-bit Shift Register**

Slice Line Specification Mode		Contents of Caption Data Latch Completion Flag		Contents of 16-bit Shift Register	
CPS		Completion Flag 1 (bit 0 of DSC2)	Completion Flag 2 (bit 5 of CPS)	Caption Data Registers 1, 2	Caption Data Registers 3, 4
bit 7	bit 6				
0	0	Line 21	A line specified by bits 4 to 0 of CPS	16-bit data of line 21	16-bit data of a line specified by bits 4 to 0 of CPS
0	1	A line specified by bits 4 to 0 of CPS	Invalid	16-bit data of a line specified by bits 4 to 0 of CPS	Invalid
1	0	Line 21	Invalid	16-bit data of line 21	Invalid
1	1	Line 21	A line specified by bits 4 to 0 of CPS	16-bit data of line 21	16-bit data of a line specified by bits 4 to 0 of CPS

CPS: Caption position register  
DSC2: Data slicer control register 2

**Table 4. Occurrence Sources of Interrupt Request**

CPS		Occurrence Sources of Interrupt Request at End of Data Slice Line
b7	b6	
0	0	After slicing line 21
	1	After a line specified by bits 4 to 0 of CPS
1	0	After slicing line 21
	1	After slicing line 21

CPS: Caption position register



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**(13) Synchronous Signal Counter**

The synchronous signal counter counts the composite sync signal taken out from a video signal in the data slicer circuit or the vertical synchronous signal  $V_{sep}$  as a count source.

The count value in a certain time (T time) generated by  $f(X_{IN})/2^{13}$  or  $f(X_{IN})/2^{13}$  is stored into the 5-bit latch. Accordingly, the latch value changes in the cycle of T time. When the count value exceeds "1F<sub>16</sub>," "1F<sub>16</sub>" is stored into the latch.

The latch value can be obtained by reading out the sync pulse counter register (address 00E9<sub>16</sub>). A count source is selected by bit 5 of the sync pulse counter register.

The synchronous signal counter is used when bit 0 of PWM mode register 1 (address 0208<sub>16</sub>).

Figure 39 shows the structure of the sync pulse counter and Figure 40 shows the synchronous signal counter block diagram.

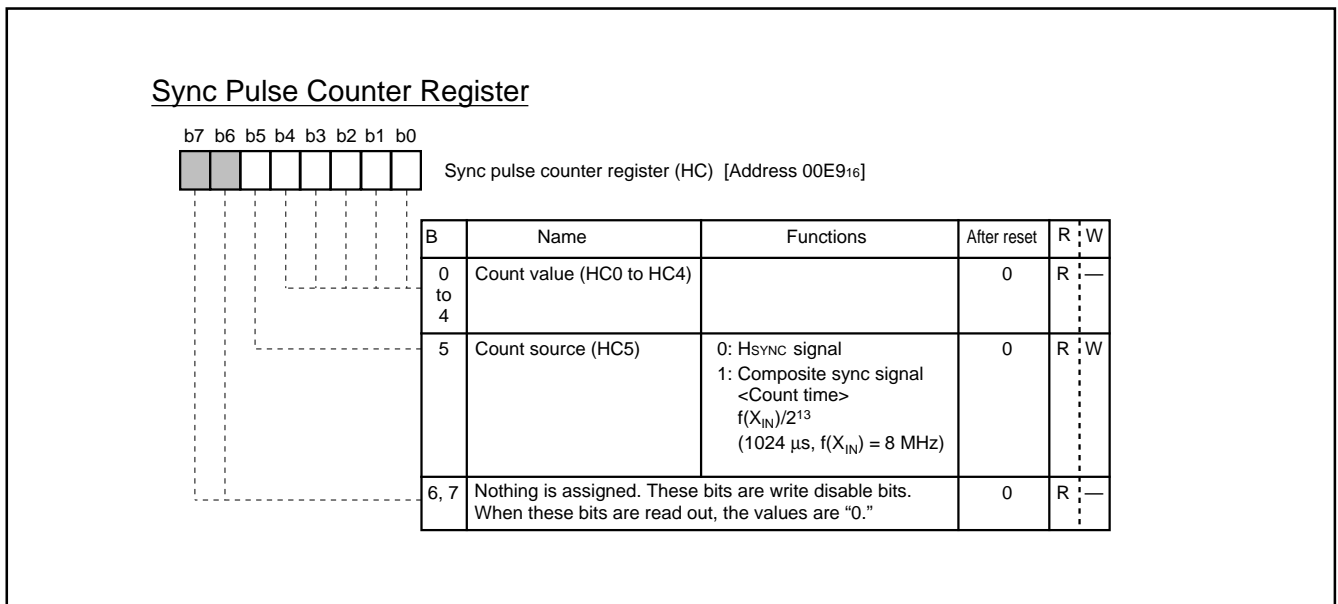


Fig. 39. Sync Pulse Counter Register

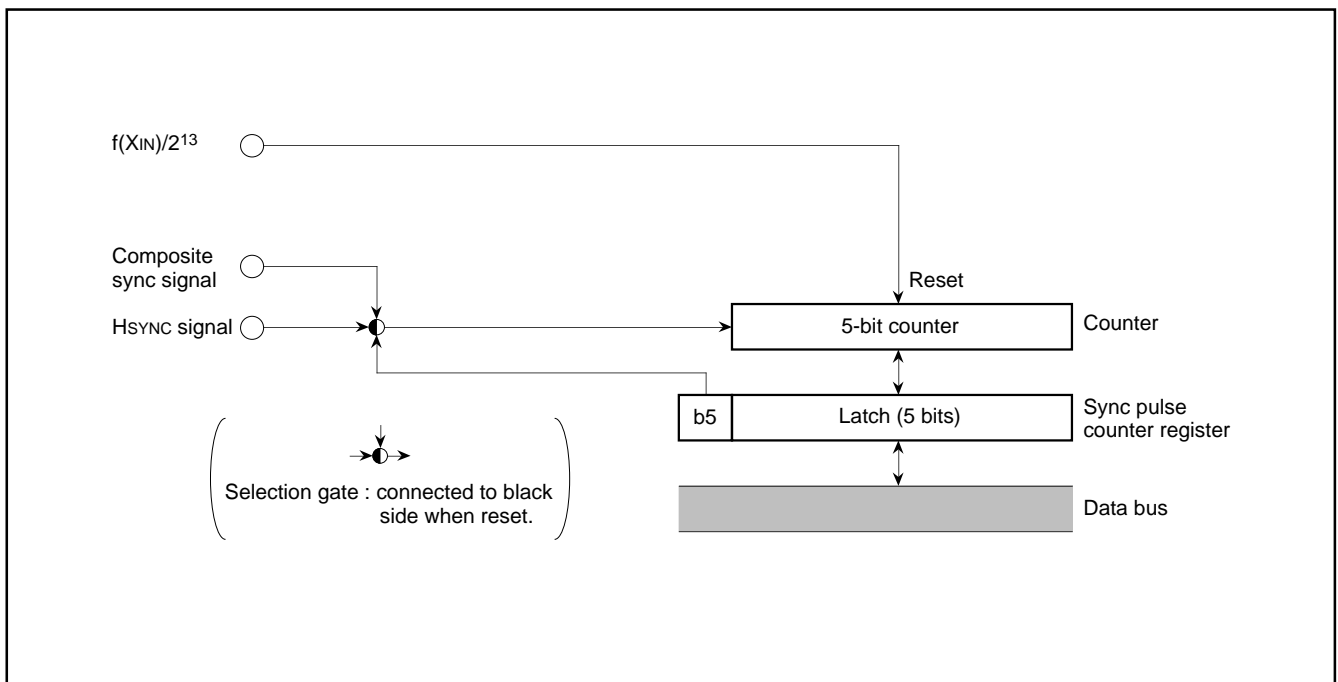


Fig. 40. Synchronous Signal Counter Block Diagram

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**MULTI-MASTER I<sup>2</sup>C-BUS INTERFACE**

The multi-master I<sup>2</sup>C-BUS interface is a serial communications circuit, conforming to the Philips I<sup>2</sup>C-BUS data transfer format. This interface, offering both arbitration lost detection and a synchronous functions, is useful for the multi-master serial communications.

Figure 41 shows a block diagram of the multi-master I<sup>2</sup>C-BUS interface and Table 5 shows multi-master I<sup>2</sup>C-BUS interface functions.

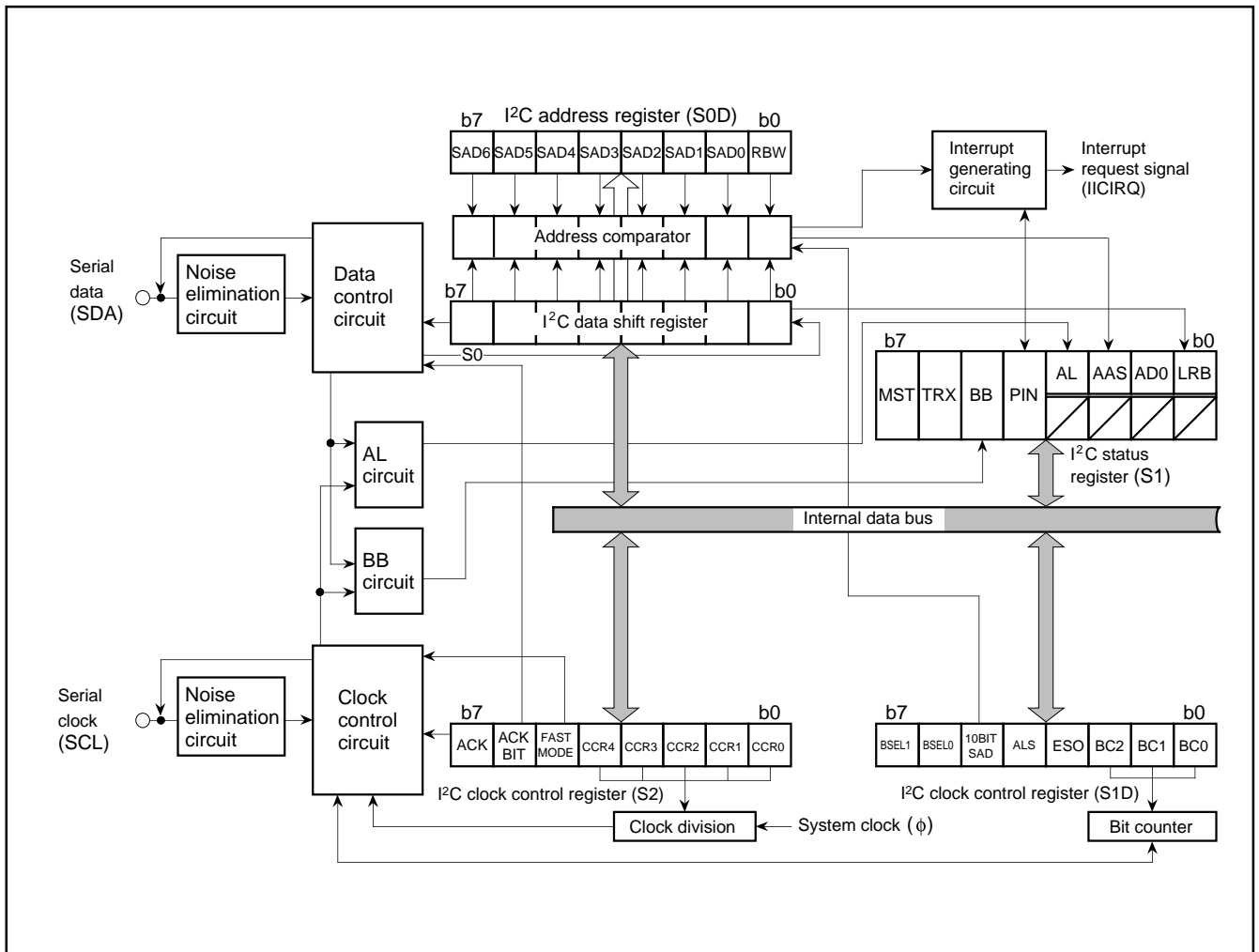
This multi-master I<sup>2</sup>C-BUS interface consists of the I<sup>2</sup>C address register, the I<sup>2</sup>C data shift register, the I<sup>2</sup>C clock control register, the I<sup>2</sup>C control register, the I<sup>2</sup>C status register and other control circuits.

**Table 5. Multi-master I<sup>2</sup>C-BUS Interface Functions**

Item	Function
Format	In conformity with Philips I <sup>2</sup> C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I <sup>2</sup> C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at $\phi = 4$ MHz)

$\phi$  : System clock =  $f(XIN)/2$

**Note:** We are not responsible for any third party's infringement of patent rights or other rights attributable to the use of the control function (bits 6 and 7 of the I<sup>2</sup>C control register at address 00F9<sub>16</sub>) for connections between the I<sup>2</sup>C-BUS interface and ports (SCL1, SCL2, SDA1, SDA2).



**Fig. 41. Block Diagram of Multi-master I<sup>2</sup>C-BUS Interface**

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**(1) I<sup>2</sup>C Data Shift Register**

The I<sup>2</sup>C data shift register (S0 : address 00F616) is an 8-bit shift register to store receive data and write transmit data.

When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL clock, and each time one-bit data is output, the data of this register are shifted one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL clock, and each time one-bit data is input, the data of this register are shifted one bit to the left.

The I<sup>2</sup>C data shift register is in a write enable status only when the ESO bit of the I<sup>2</sup>C control register (address 00F916) is "1." The bit counter is reset by a write instruction to the I<sup>2</sup>C data shift register. When both the ESO bit and the MST bit of the I<sup>2</sup>C status register (address 00F816) are "1," the SCL is output by a write instruction to the I<sup>2</sup>C data shift register. Reading data from the I<sup>2</sup>C data shift register is always enabled regardless of the ESO bit value.

**Note:** To write data into the I<sup>2</sup>C data shift register after setting the MST bit to "0" (slave mode), keep an interval of 8 machine cycles or more.

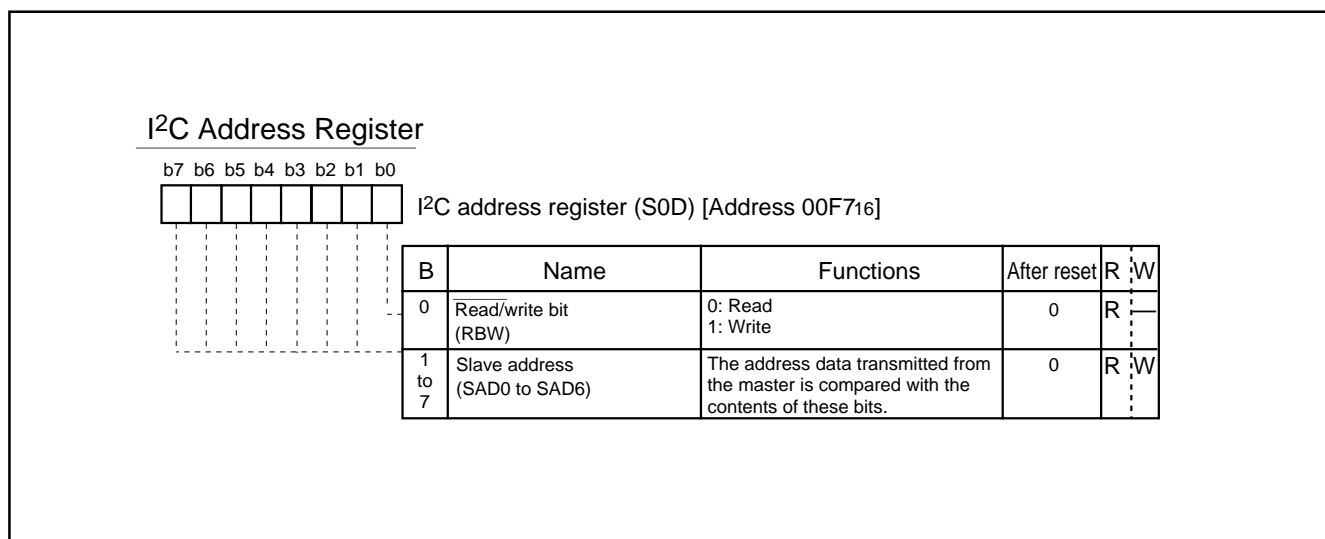


Fig. 42. I<sup>2</sup>C Data Shift Register

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**(2) I<sup>2</sup>C Address Register**

The I<sup>2</sup>C address register (address 00F7<sub>16</sub>) consists of a 7-bit slave address and a read/write bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition are detected.

■ Bit 0: Read/Write Bit (RBW)

Not used when comparing addresses, in the 7-bit addressing mode.

In the 10-bit addressing mode, the first address data to be received is compared with the contents (SAD<sub>6</sub> to SAD<sub>0</sub> + RBW) of the I<sup>2</sup>C address register.

The RBW bit is cleared to "0" automatically when the stop condition is detected.

■ Bits 1 to 7: Slave Address (SAD<sub>0</sub>–SAD<sub>6</sub>)

These bits store slave addresses. Regardless of the 7-bit addressing mode and the 10-bit addressing mode, the address data transmitted from the master is compared with the contents of these bits.

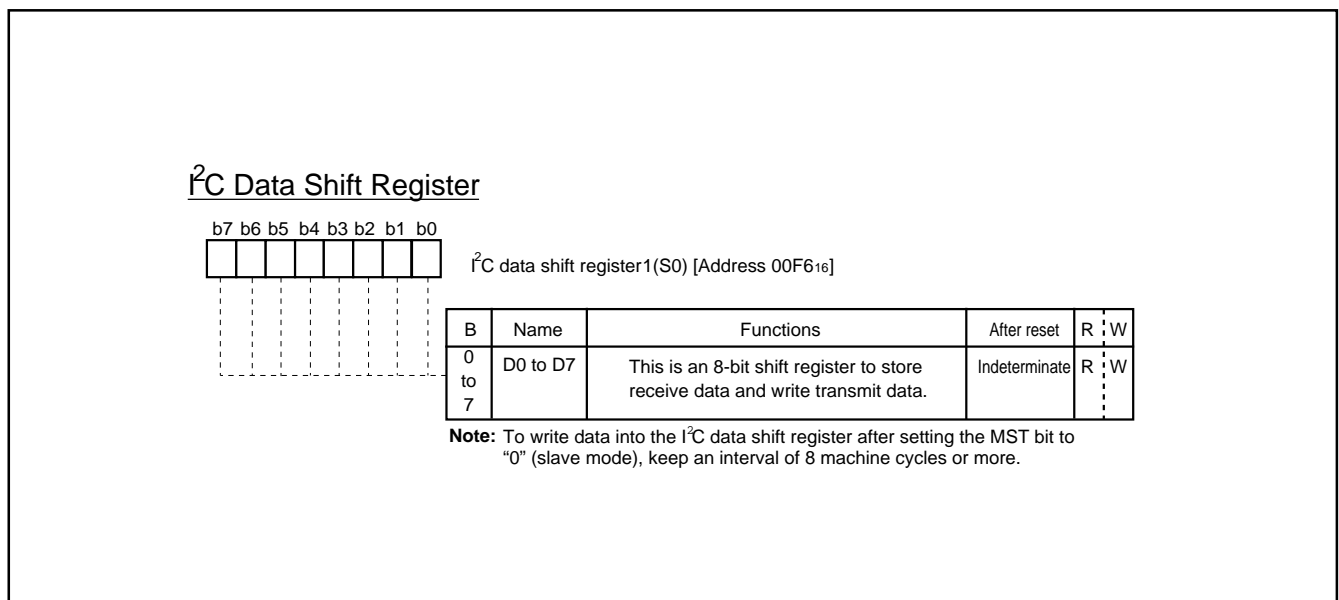


Fig. 43. I<sup>2</sup>C Address Register

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### (3) I<sup>2</sup>C Clock Control Register

The I<sup>2</sup>C clock control register (address 00FA16) is used to set ACK control, SCL mode and SCL frequency.

■ Bits 0 to 4: SCL Frequency Control Bits (CCR0–CCR4)

These bits control the SCL frequency. Refer to Table 7.

■ Bit 5: SCL Mode Specification Bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to “0,” the standard clock mode is set. When the bit is set to “1,” the high-speed clock mode is set.

■ Bit 6: ACK Bit (ACK BIT)

This bit sets the SDA status when an ACK clock\* is generated. When this bit is set to “0,” the ACK return mode is set and SDA goes to LOW at the occurrence of an ACK clock. When the bit is set to “1,” the ACK non-return mode is set. The SDA is held in the HIGH status at the occurrence of an ACK clock.

However, when the slave address matches the address data in the reception of address data at ACK BIT = “0,” the SDA is automatically made LOW (ACK is returned). If there is a mismatch between the slave address and the address data, the SDA is automatically made HIGH (ACK is not returned).

■ Bit 7: ACK Clock Bit (ACK)

This bit specifies a mode of acknowledgment which is an acknowledgment response of data transmission. When this bit is set to “0,” the no ACK clock mode is set. In this case, no ACK clock occurs after data transmission. When the bit is set to “1,” the ACK clock mode is set and the master generates an ACK clock upon completion of each 1-byte data transmission. The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (make SDA HIGH) and receives the ACK bit generated by the data receiving device.

**Note:** Do not write data into the I<sup>2</sup>C clock control register during transmission. If data is written during transmission, the I<sup>2</sup>C clock generator is reset, so that data cannot be transmitted normally.

\*ACK clock: Clock for acknowledgment

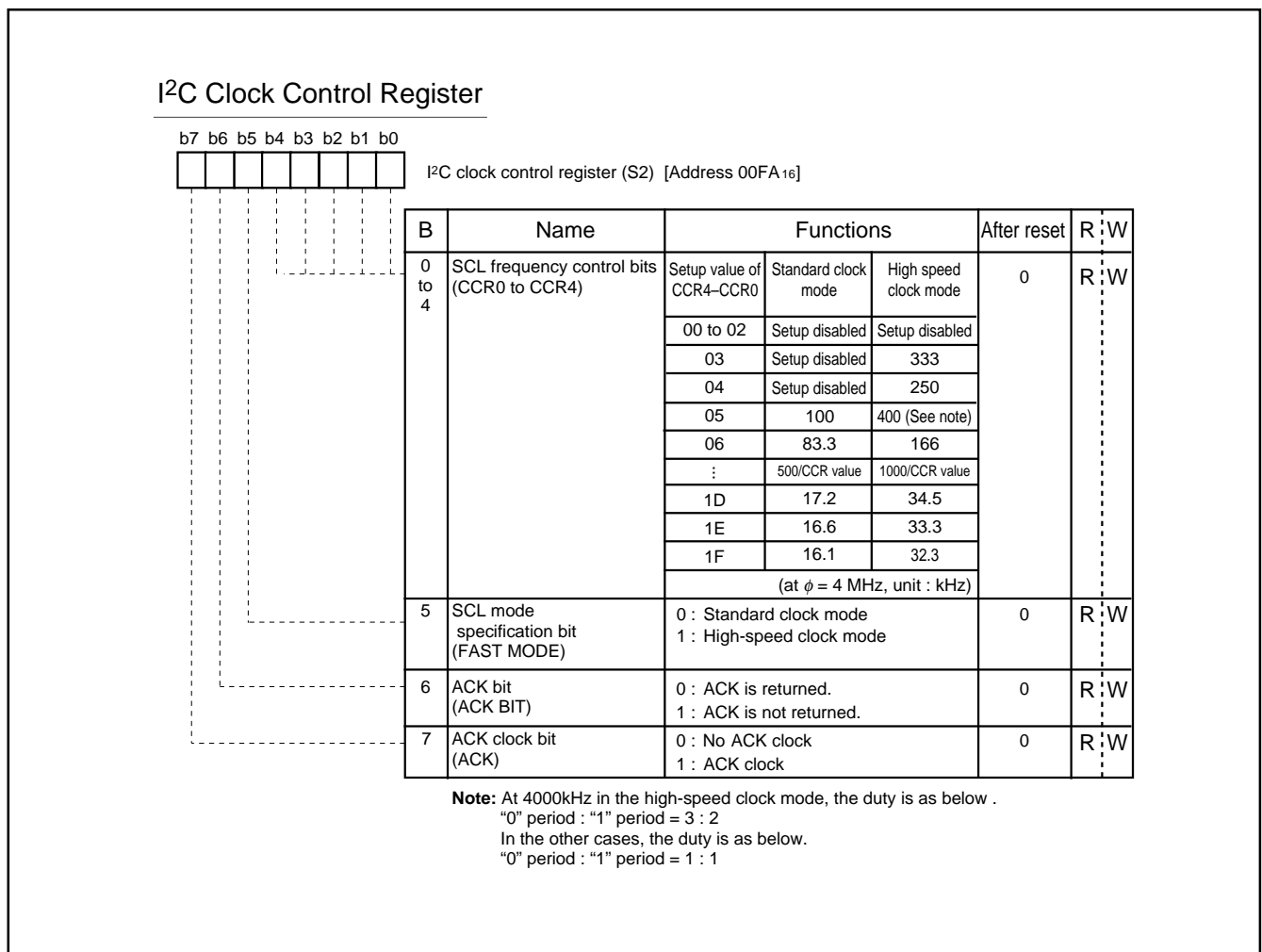


Fig. 44. I<sup>2</sup>C Clock Control Register

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**(4) I<sup>2</sup>C Control Register**

The I<sup>2</sup>C control register (address 00F916) controls the data communication format.

■ Bits 0 to 2: Bit Counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. An interrupt request signal occurs immediately after the number of bits specified with these bits are transmitted.

When a START condition is received, these bits become “0002” and the address data is always transmitted and received in 8 bits.

■ Bit 3: I<sup>2</sup>C Interface Use Enable Bit (ESO)

This bit enables usage of the multi-master I<sup>2</sup>C BUS interface. When this bit is set to “0,” the use disable status is provided, so the SDA and the SCL become high-impedance. When the bit is set to “1,” use of the interface is enabled.

When ESO = “0,” the following is performed.

- PIN = “1,” BB = “0” and AL = “0” are set (they are bits of the I<sup>2</sup>C status register at address 00F816).
- Writing data to the I<sup>2</sup>C data shift register (address 00F616) is disabled.

■ Bit 4: Data Format Selection Bit (ALS)

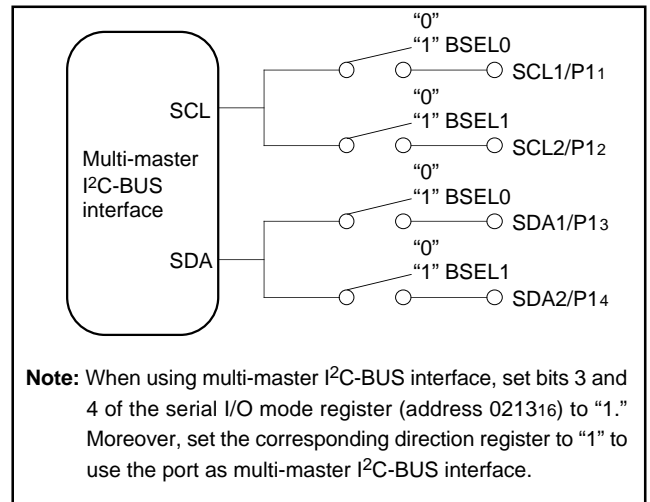
This bit decides whether or not to recognize slave addresses. When this bit is set to “0,” the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to “(5) I<sup>2</sup>C Status Register,” bit 1) is received, transmission processing can be performed. When this bit is set to “1,” the free data format is selected, so that slave addresses are not recognized.

■ Bit 5: Addressing Format Selection Bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to “0,” the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I<sup>2</sup>C address register (address 00F716) are compared with address data. When this bit is set to “1,” the 10-bit addressing format is selected, all the bits of the I<sup>2</sup>C address register are compared with address data.

■ Bits 6 and 7: Connection Control Bits between I<sup>2</sup>C-BUS Interface and Ports (BSEL0, BSEL1)

These bits controls the connection between SCL and ports or SDA and ports (refer to Figure 45).



**Note:** When using multi-master I<sup>2</sup>C-BUS interface, set bits 3 and 4 of the serial I/O mode register (address 021316) to “1.” Moreover, set the corresponding direction register to “1” to use the port as multi-master I<sup>2</sup>C-BUS interface.

**Fig. 45. Connection Port Control by BSEL0 and BSEL1**

**I<sup>2</sup>C Control Register**

b7	b6	b5	b4	b3	b2	b1	b0

I<sup>2</sup>C control register (S1D) [Address 00F916]

B	Name	Functions	After reset	R;W
0 to 2	Bit counter (Number of transmit/receive bits) (BC0 to BC2)	b2 b1 b0 0 0 0 : 8 0 0 1 : 7 0 1 0 : 6 0 1 1 : 5 1 0 0 : 4 1 0 1 : 3 1 1 0 : 2 1 1 1 : 1	0	R;W
3	I <sup>2</sup> C-BUS interface use enable bit (ESO)	0 : Disabled 1 : Enabled	0	R;W
4	Data format selection bit (ALS)	0 : Addressing mode 1 : Free data format	0	R;W
5	Addressing format selection bit (10BIT SAD)	0 : 7-bit addressing format 1 : 10-bit addressing format	0	R;W
6, 7	Connection control bits between I <sup>2</sup> C-BUS interface and ports	b7 b6 Connection port (See note) 0 0 : None 0 1 : SCL1, SDA1 1 0 : SCL2, SDA2 1 1 : SCL1, SDA1 SCL2, SDA2	0	R;W

**Note:** When using ports P11-P14 as I<sup>2</sup>C-BUS interface, the output structure changes automatically from CMOS output to N-channel open-drain output.

**Fig. 46. I<sup>2</sup>C Control Register**

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### (5) I<sup>2</sup>C Status Register

The I<sup>2</sup>C status register (address 00F816) controls the I<sup>2</sup>C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

#### ■ Bit 0: Last Receive Bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0." If ACK is not returned, this bit is set to "1." Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I<sup>2</sup>C data shift register (address 00F616).

#### ■ Bit 1: General Call Detecting Flag (AD0)

This bit is set to "1" when a general call\* whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition.

\*General call: The master transmits the general call address "0016" to all slaves.

#### ■ Bit 2: Slave Address Comparison Flag (AAS)

This flag indicates a comparison result of address data.

① In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions.

- The address data immediately after occurrence of a START condition matches the slave address stored in the high-order 7 bits of the I<sup>2</sup>C address register (address 00F716).
- A general call is received.

② In the slave reception mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition.

- When the address data is compared with the I<sup>2</sup>C address register (8 bits consists of slave address and RBW), the first bytes match.

③ The state of this bit is changed from "1" to "0" by executing a write instruction to the I<sup>2</sup>C data shift register (address 00F616).

#### ■ Bit 3: Arbitration Lost\* Detecting Flag (AL)

In the master transmission mode, when a device other than the microcomputer sets the SDA to "L," arbitration is judged to have been lost, so that this bit is set to "1." At the same time, the TRX bit is set to "0," so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0." When arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to receive and recognize its own slave address transmitted by another master device.

\*Arbitration lost: The status in which communication as a master is disabled.

#### ■ Bit 4: I<sup>2</sup>C-BUS Interface Interrupt Request Bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the state of the PIN bit changes from "1" to "0." At the same time, an interrupt request signal is sent to the CPU. The PIN bit is set to "0" in synchronization with a falling edge of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling edge of the PIN bit. When the PIN bit is "0," the SCL is kept in the "0" state and clock generation is disabled. Figure 48 shows an interrupt request signal generating timing chart.

The PIN bit is set to "1" in any one of the following conditions.

- Executing a write instruction to the I<sup>2</sup>C data shift register (address 00F616).
- When the ES0 bit is "0"
- At reset

The conditions in which the PIN bit is set to "0" are shown below:

- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

#### ■ Bit 5: Bus Busy Flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to "0," this bus system is not busy and a START condition can be generated. When this bit is set to "1," this bus system is busy and the occurrence of a START condition is disabled by the START condition duplication prevention function (Note).

This flag can be written by software only in the master transmission mode. In the other modes, this bit is set to "1" by detecting a START condition and set to "0" by detecting a STOP condition. When the ES0 bit of the I<sup>2</sup>C control register (address 00F916) is "0" and at reset, the BB flag is kept in the "0" state.

#### ■ Bit 6: Communication Mode Specification Bit (transfer direction specification bit: TRX)

This bit decides the direction of transfer for data communication. When this bit is "0," the reception mode is selected and the data of a transmitting device is received. When the bit is "1," the transmission mode is selected and address data and control data are output into the SDA in synchronization with the clock generated on the SCL.

When the ALS bit of the I<sup>2</sup>C control register (address 00F916) is "0" in the slave reception mode is selected, the TRX bit is set to "1" (transmit) if the least significant bit (R/W bit) of the address data transmitted by the master is "1." When the ALS bit is "0" and the R/W bit is "0," the TRX bit is cleared to "0" (receive).

The TRX bit is cleared to "0" in one of the following conditions.

- When arbitration lost is detected.
- When a STOP condition is detected.
- When occurrence of a START condition is disabled by the START condition duplication prevention function (Note).
- With MST = "0" and when a START condition is detected.
- With MST = "0" and when ACK non-return is detected.
- At reset

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■ Bit 7: Communication Mode Specification Bit (master/slave specification bit: MST)

This bit is used for master/slave specification for data communication. When this bit is "0," the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is "1," the master is specified and a START condition and a STOP condition are generated, and also the clocks required for data communication are generated on the SCL.

The MST bit is cleared to "0" in one of the following conditions.

- Immediately after completion of 1-byte data transmission when arbitration lost is detected
- When a STOP condition is detected.
- When occurrence of a START condition is disabled by the START condition duplication preventing function (Note).
- At reset

**Note:** The START condition duplication prevention function disables the START condition generation, reset of bit counter reset, and SCL output, when the following condition is satisfied:

- a START condition is set by another master device.

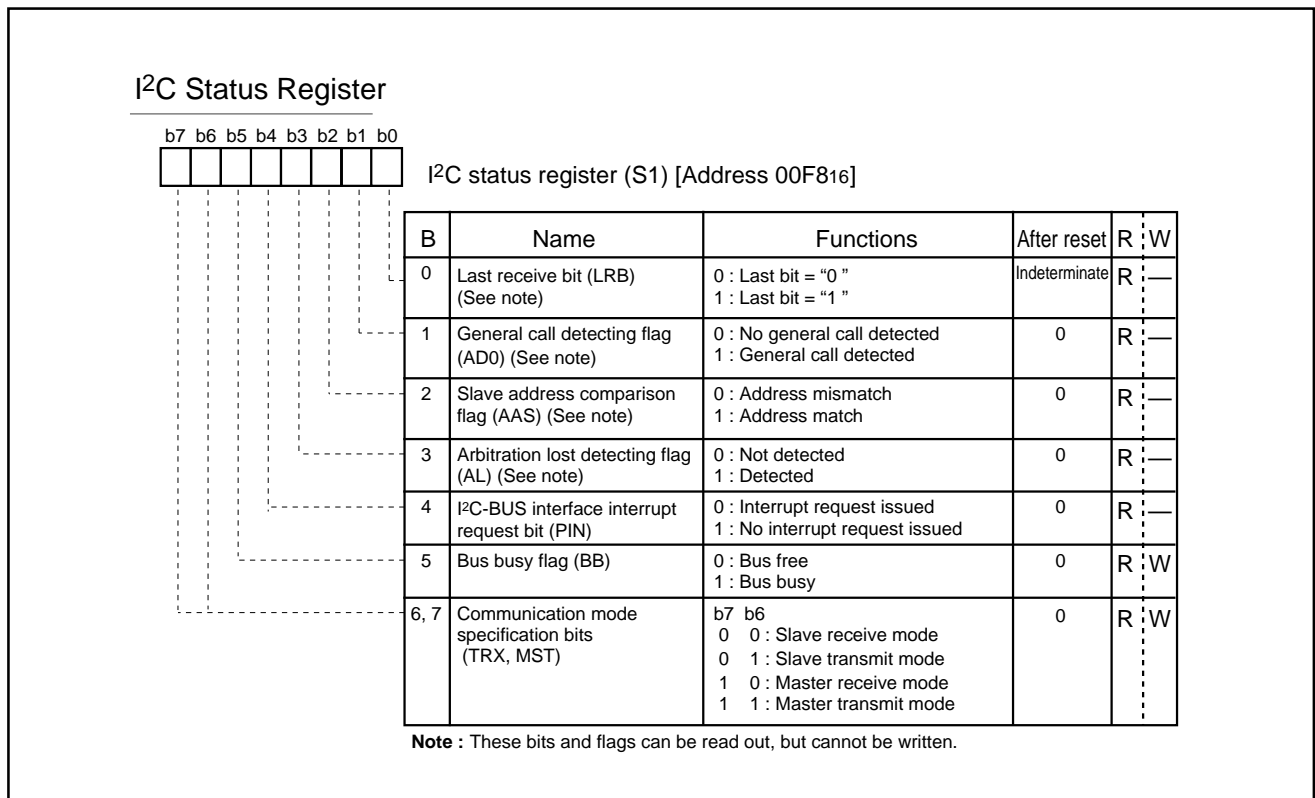


Fig. 47. I<sup>2</sup>C Status Register

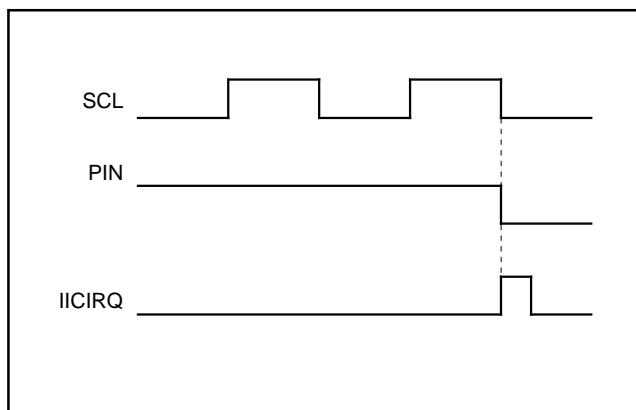


Fig. 48. Interrupt Request Signal Generation Timing



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**(6) START Condition Generation Method**

When the ESO bit of the I<sup>2</sup>C control register (address 00F9<sub>16</sub>) is "1," execute a write instruction to the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) to set the MST, TRX and BB bits to "1." A START condition will then be generated. After that, the bit counter becomes "0002" and an SCL for 1 byte is output. The START condition generation timing and BB bit set timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 49 for the START condition generation timing diagram, and Table 8 for the START condition/STOP condition generation timing table.

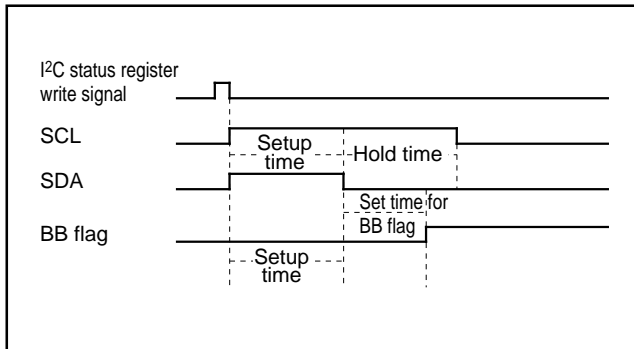


Fig. 49. START Condition Generation Timing Diagram

**(7) RESTART Condition Generation Method**

To generate the RESTART condition, take the following sequence:

- ① Set "20<sub>16</sub>" to the I<sup>2</sup>C status register (S1).
- ② Write a transmit data to the I<sup>2</sup>C data shift register.
- ③ Set "F0<sub>16</sub>" to the I<sup>2</sup>C status register (S1) again.

**<Example of Setting of RESTART Condition>**

I<sup>2</sup>C status register ; S1 = 20<sub>16</sub>  
I<sup>2</sup>C data shift register ; S0 = transmit data after restart  
I<sup>2</sup>C status register ; S1 = F0<sub>16</sub>

**(8) STOP Condition Generation Method**

When the ES0 bit of the I<sup>2</sup>C control register (address 00F9<sub>16</sub>) is "1," execute a write instruction to the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) for setting the MST bit and the TRX bit to "1" and the BB bit to "0." A STOP condition will then be generated. The STOP condition generation timing and the BB flag reset timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 50 for the STOP condition generation timing diagram, and Table 6 for the START condition/STOP condition generation timing table.

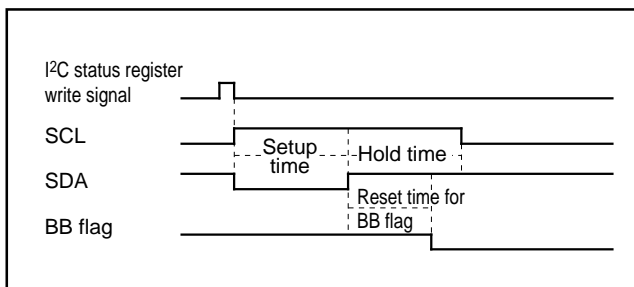


Fig. 50. STOP Condition Generation Timing Diagram

Table 6. START Condition/STOP Condition Generation Timing Table

Item	Standard Clock Mode	High-speed Clock Mode
Setup time	5.0 μs (20 cycles)	2.5 μs (10 cycles)
Hold time	5.0 μs (20 cycles)	2.5 μs (10 cycles)
Set/reset time for BB flag	3.0 μs (12 cycles)	1.5 μs (6 cycles)

**Note:** Absolute time at φ = 4 MHz. The value in parentheses denotes the number of φ cycles.

**(9) START/STOP Condition Detect Conditions**

The START/STOP condition detect conditions are shown in Figure 51 and Table 7. Only when the 3 conditions of Table 7 are satisfied, a START/STOP condition can be detected.

**Note:** When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal "IICIRQ" is generated to the CPU.

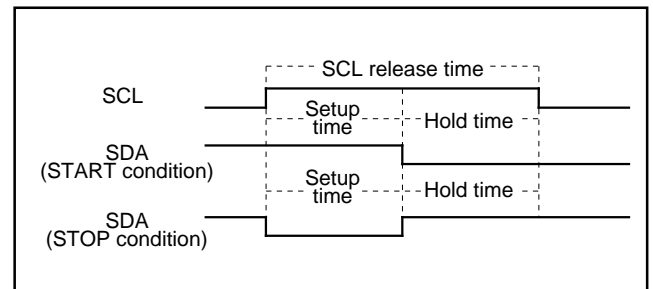


Fig. 51. START Condition/STOP Condition Detect Timing Diagram

Table 7. START Condition/STOP Condition Detect Conditions

Standard Clock Mode	High-speed Clock Mode
6.5 μs (26 cycles) < SCL release time	1.0 μs (4 cycles) < SCL release time
3.25 μs (13 cycles) < Setup time	0.5 μs (2 cycles) < Setup time
3.25 μs (13 cycles) < Hold time	0.5 μs (2 cycles) < Hold time

**Note:** Absolute time at φ = 4 MHz. The value in parentheses denotes the number of φ cycles.

## (10) Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats is described below.

### ① 7-bit addressing format

To meet the 7-bit addressing format, set the 10BIT SAD bit of the I<sup>2</sup>C control register (address 00F9<sub>16</sub>) to "0." The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I<sup>2</sup>C address register (address 00F7<sub>16</sub>). At the time of this comparison, address comparison of the RBW bit of the I<sup>2</sup>C address register (address 00F7<sub>16</sub>) is not made. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 52, (1) and (2).

### ② 10-bit addressing format

To meet the 10-bit addressing format, set the 10BIT SAD bit of the I<sup>2</sup>C control register (address 00F9<sub>16</sub>) to "1." An address comparison is made between the first-byte address data transmitted from the master and the 7-bit slave address stored in the I<sup>2</sup>C address register (address 00F7<sub>16</sub>). At the time of this comparison, an address comparison between the RBW bit of the I<sup>2</sup>C address register (address 00F7<sub>16</sub>) and the  $\overline{R/W}$  bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the  $\overline{R/W}$  bit which is the last bit of the address data not only specifies the direction of communication for control data but also is processed as an address data bit.

When the first-byte address data matches the slave address, the AAS bit of the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) is set to "1." After the second-byte address data is stored into the I<sup>2</sup>C data shift register (address 00F6<sub>16</sub>), make an address comparison between the second-byte data and the slave address by software. When the address data of the 2nd bytes matches the slave address, set the RBW bit of the I<sup>2</sup>C address register (address 00F7<sub>16</sub>) to "1" by software. This processing can match the 7-bit slave address and  $\overline{R/W}$  data, which are received after a RESTART condition is detected, with the value of the I<sup>2</sup>C address register (address 00F7<sub>16</sub>). For the data transmission format when the 10-bit addressing format is selected, refer to Figure 52, (3) and (4).

## (11) Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

- ① Set a slave address in the high-order 7 bits of the I<sup>2</sup>C address register (address 00F7<sub>16</sub>) and "0" in the RBW bit.
- ② Set the ACK return mode and SCL = 100 kHz by setting "85<sub>16</sub>" in the I<sup>2</sup>C clock control register (address 00FA<sub>16</sub>).
- ③ Set "10<sub>16</sub>" in the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) and hold the SCL at the HIGH.
- ④ Set a communication enable status by setting "48<sub>16</sub>" in the I<sup>2</sup>C control register (address 00F9<sub>16</sub>).
- ⑤ Set the address data of the destination of transmission in the high-order 7 bits of the I<sup>2</sup>C data shift register (address 00F6<sub>16</sub>) and set "0" in the least significant bit.
- ⑥ Set "F0<sub>16</sub>" in the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occurs.

- ⑦ Set transmit data in the I<sup>2</sup>C data shift register (address 00F6<sub>16</sub>). At this time, an SCL and an ACK clock automatically occurs.
- ⑧ When transmitting control data of more than 1 byte, repeat step ⑦.
- ⑨ Set "D0<sub>16</sub>" in the I<sup>2</sup>C status register (address 00F8<sub>16</sub>). After this, if ACK is not returned or transmission ends, a STOP condition will be generated.

## (12) Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode, using the addressing format, is shown below.

- ① Set a slave address in the high-order 7 bits of the I<sup>2</sup>C address register (address 00F7<sub>16</sub>) and "0" in the RBW bit.
- ② Set the no ACK clock mode and SCL = 400 kHz by setting "25<sub>16</sub>" in the I<sup>2</sup>C clock control register (address 00FA<sub>16</sub>).
- ③ Set "10<sub>16</sub>" in the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) and hold the SCL at the HIGH.
- ④ Set a communication enable status by setting "48<sub>16</sub>" in the I<sup>2</sup>C control register (address 00F9<sub>16</sub>).
- ⑤ When a START condition is received, an address comparison is made.
- ⑥ •When all transmitted addresses are "0" (general call) :  
AD0 of the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) is set to "1" and an interrupt request signal occurs.  
•When the transmitted addresses match the address set in ① :  
AAS of the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) is set to "1" and an interrupt request signal occurs.  
•In the cases other than the above :  
AD0 and AAS of the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) are set to "0" and no interrupt request signal occurs.
- ⑦ Set dummy data in the I<sup>2</sup>C data shift register (address 00F6<sub>16</sub>).
- ⑧ When receiving control data of more than 1 byte, repeat step ⑦.
- ⑨ When a STOP condition is detected, the communication ends.

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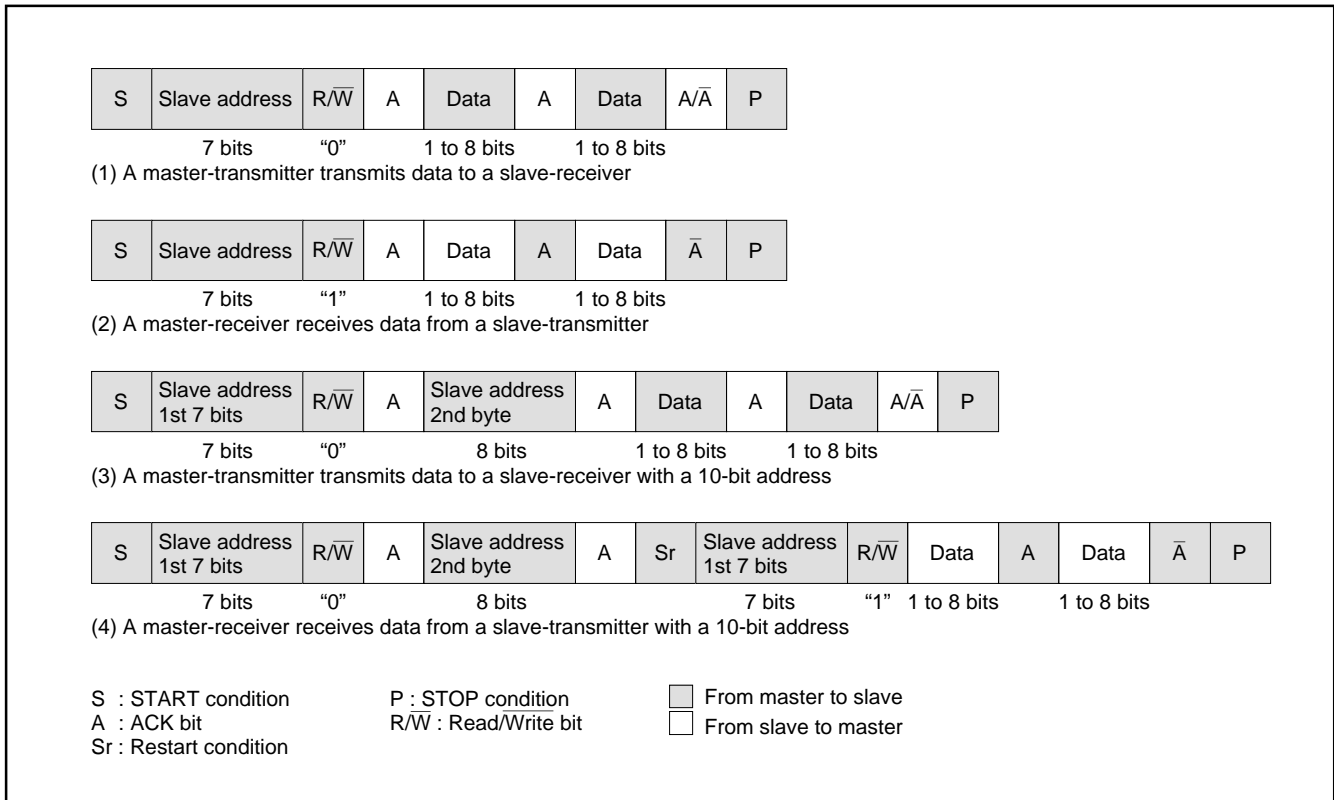


Fig. 52. Address Data Communication Format

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**OSD FUNCTIONS**

Table 8 outlines the OSD functions of the M37273MF-XXXSP.  
The M37273MF-XXXSP incorporates an OSD circuit of 32 characters X 2 lines. There are 2 display modes and they are selected by a block unit. The display modes are selected by bits 0 and 1 of block control register i (i = 1 and 2).  
The features of each mode are described below.

**Table 8. Features of Each Display Mode**

Parameter	Display Mode	
	CC Mode (Closed caption mode)	OSD Mode (Border OFF) (On-screen display mode)
Number of display characters	32 characters X 2 lines	
Character display area	16 X 26 dots	16 X 20 dots
Kinds of characters	254 kinds	
Kinds of character sizes	1 kind	8 kinds
	Pre-divide ratio (Note)	X 2, X 3
	Dot size	1Tc X 1/2H
Attribute	Smooth italic, under line, flash	Border (black)
Character font coloring	1 screen : 7 kinds, Max. 7 kinds (a character unit)	
Raster coloring	Possible (a screen unit, max. 7 kinds)	
Character background coloring	_____	Possible (a character unit, 1 screen : 7 kinds, max. 7 kinds)
OSD output	R, G, B, OUT1, OUT2	
Function	Auto solid space function Window function	_____
Display expansion (multiline display)	Possible	

**Notes 1:** The divide ratio of the frequency divider (the pre-divide circuit) is referred as "pre-divide ratio" hereafter.  
**2:** The character size is specified with dot size and pre-divide ratio (refer to (2) Dote size).

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The OSD circuit has an extended display mode. This mode allows multiple lines (3 lines or more) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 53 shows the configuration of OSD character. Figure 54 shows the block diagram of the OSD circuit. Figure 55 shows the OSD control register. Figure 56 shows the block control register.

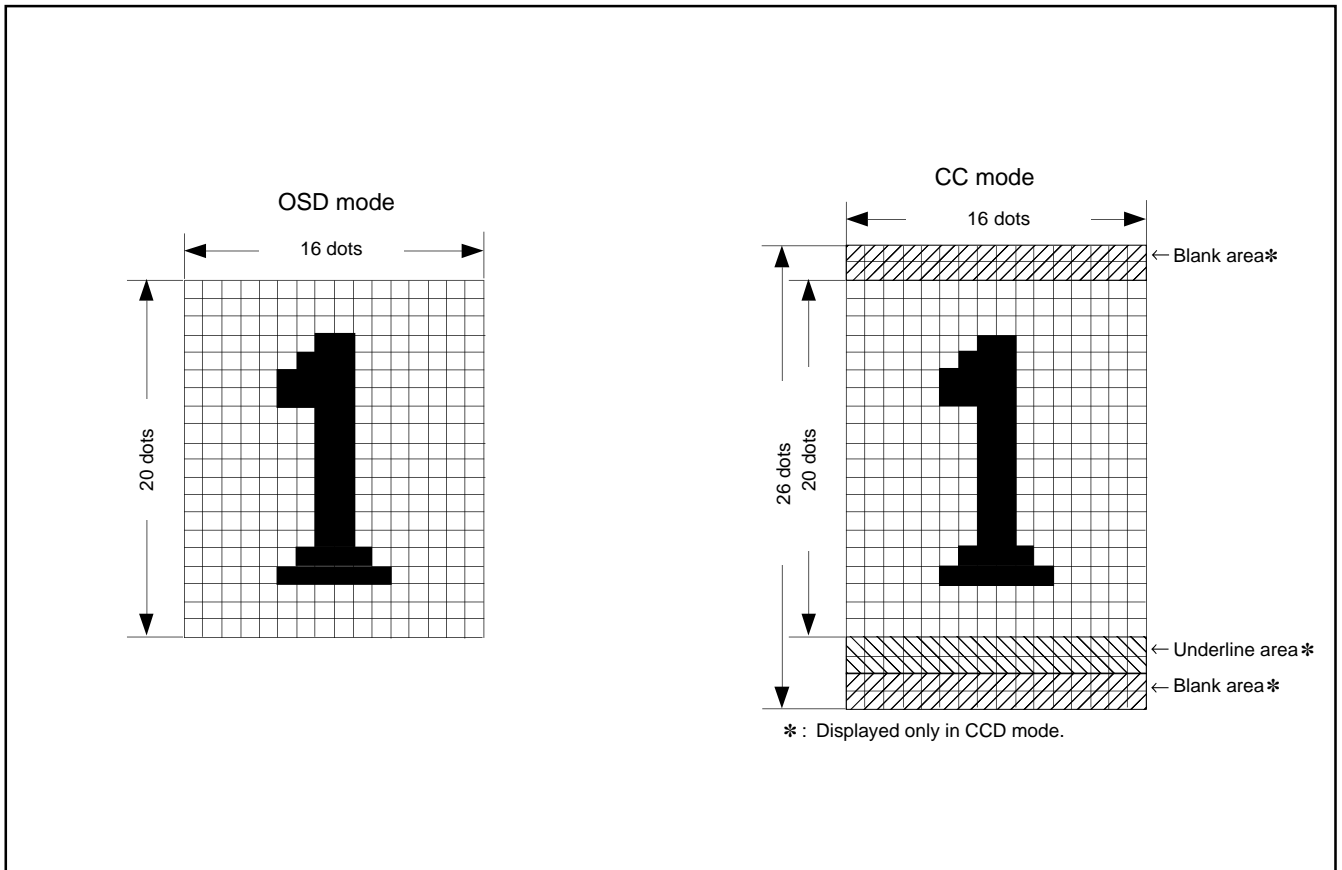


Fig. 53. Configuration of OSD Character Display Area

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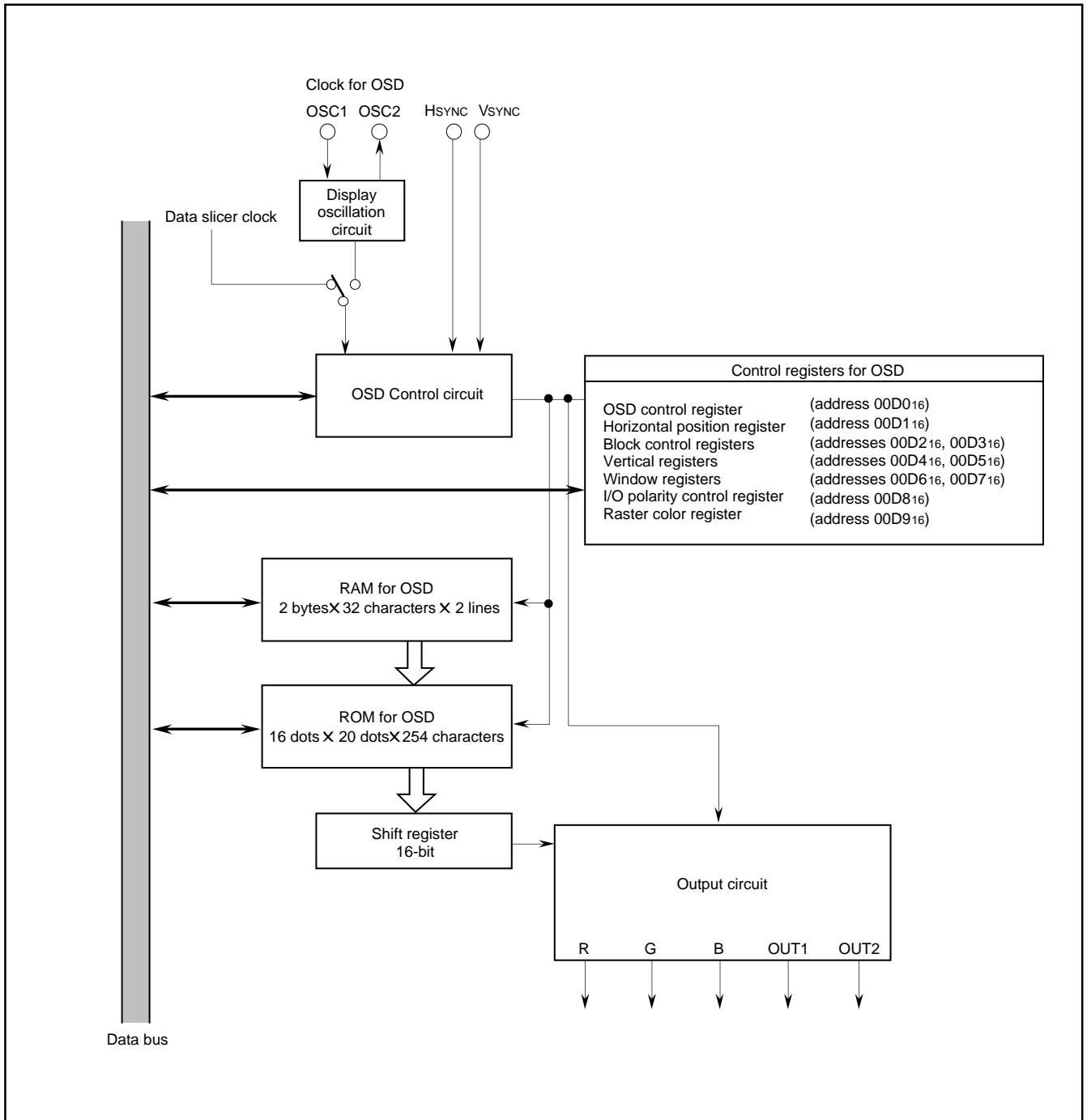


Fig. 54. Block Diagram of OSD Circuit

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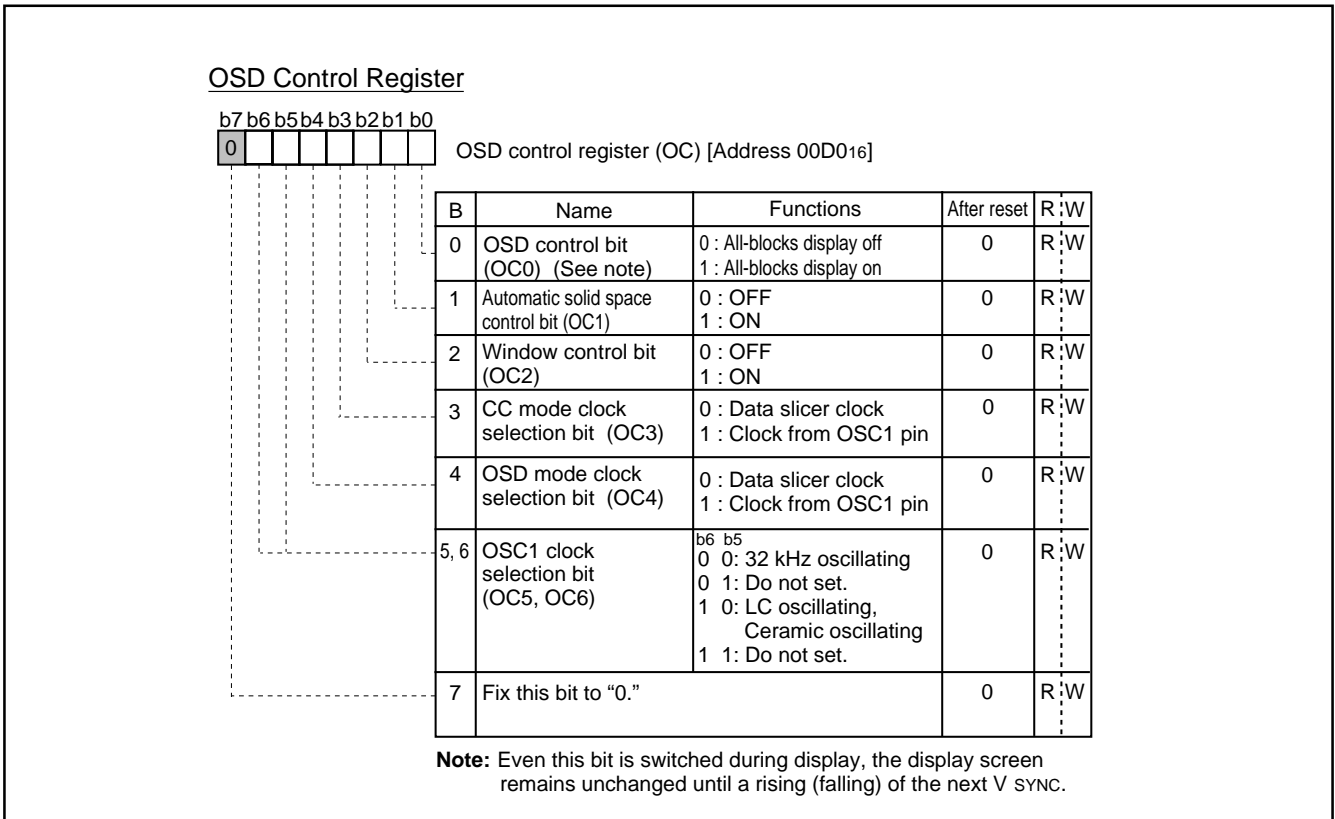


Fig. 55. OSD Control Register

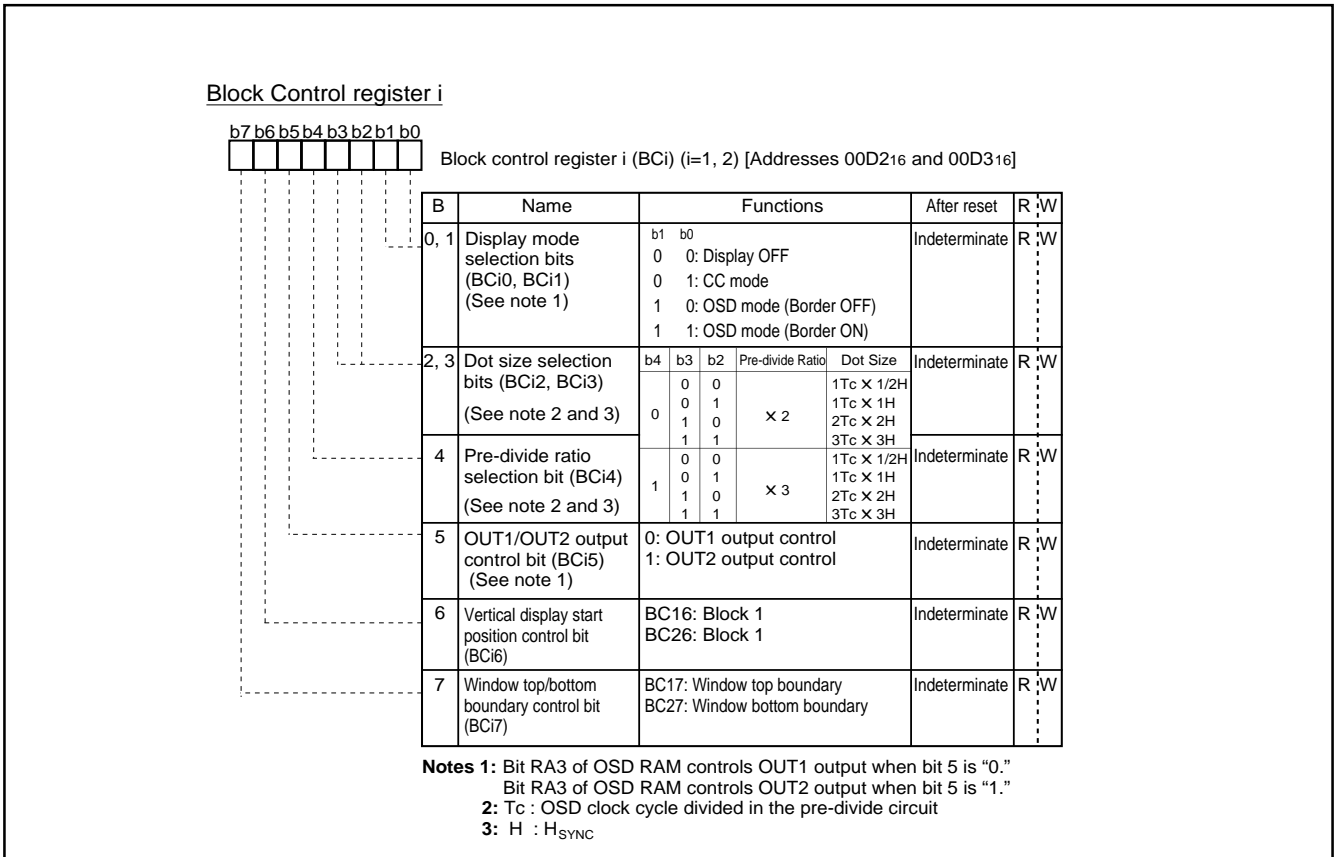


Fig. 56. Block Control Registers

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**(1) Display Position**

The display positions of characters are specified in units called a "block." There are 2 blocks, blocks 1 and 2. Up to 32 characters can be displayed in each block (refer to (5) Memory for OSD).

The display position of each block can be set in both horizontal and vertical directions by software.

The display position in the horizontal direction can be selected for all blocks in common from 128-step display positions in units of 4 T<sub>osc</sub> (T<sub>osc</sub> = OSD oscillation cycle).

The display position in the vertical direction for each block can be selected from 512-step display positions in units of 1 T<sub>H</sub> (T<sub>H</sub> = H<sub>sync</sub> cycle).

Blocks are displayed in conformance with the following rules:

- ① When the display position of block 1 is overlapped with that of block 2 (Figure 57, (b)), the block 1 is displayed on the front.
- ② When another block display position appears while one block is displayed (Figure 57, (c)), the block with a larger set value as the vertical display start position is displayed.

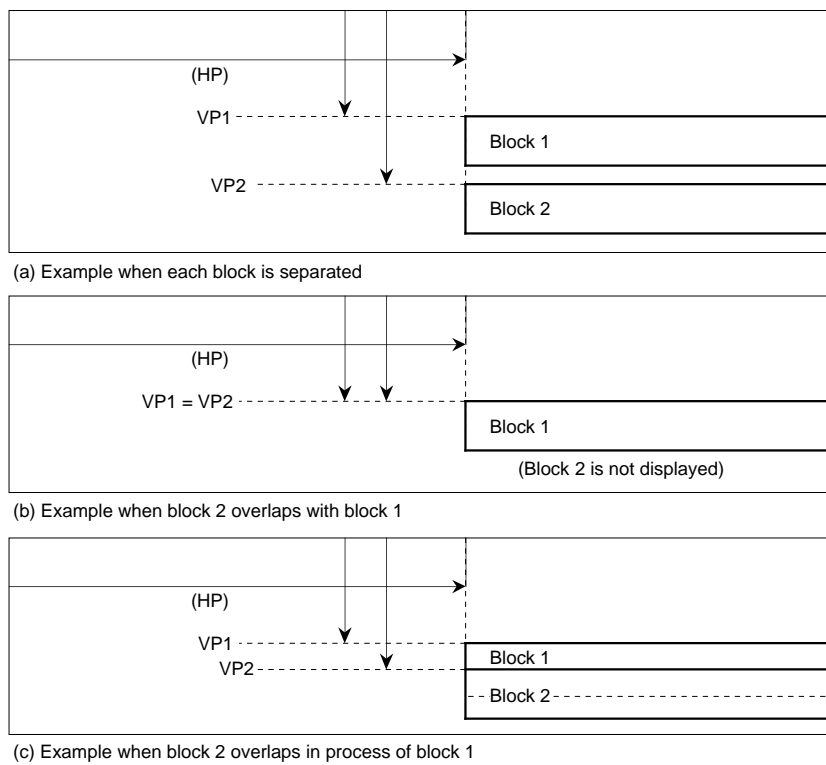


Fig. 57. Display Position



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The display position in the vertical direction is determined by counting the horizontal sync signal (HSYNC). At this time, when VSYNC and HSYNC are positive polarity (negative polarity), it starts to count the rising edge (falling edge) of HSYNC signal from after fixed cycle of rising edge (falling edge) of VSYNC signal. So interval from rising edge (falling edge) of VSYNC signal to rising edge (falling edge) of HSYNC signal needs enough time (2 machine cycles or more) for avoiding jitter. The polarity of HSYNC and VSYNC signals can select with the I/O polarity control register (address 00D816).

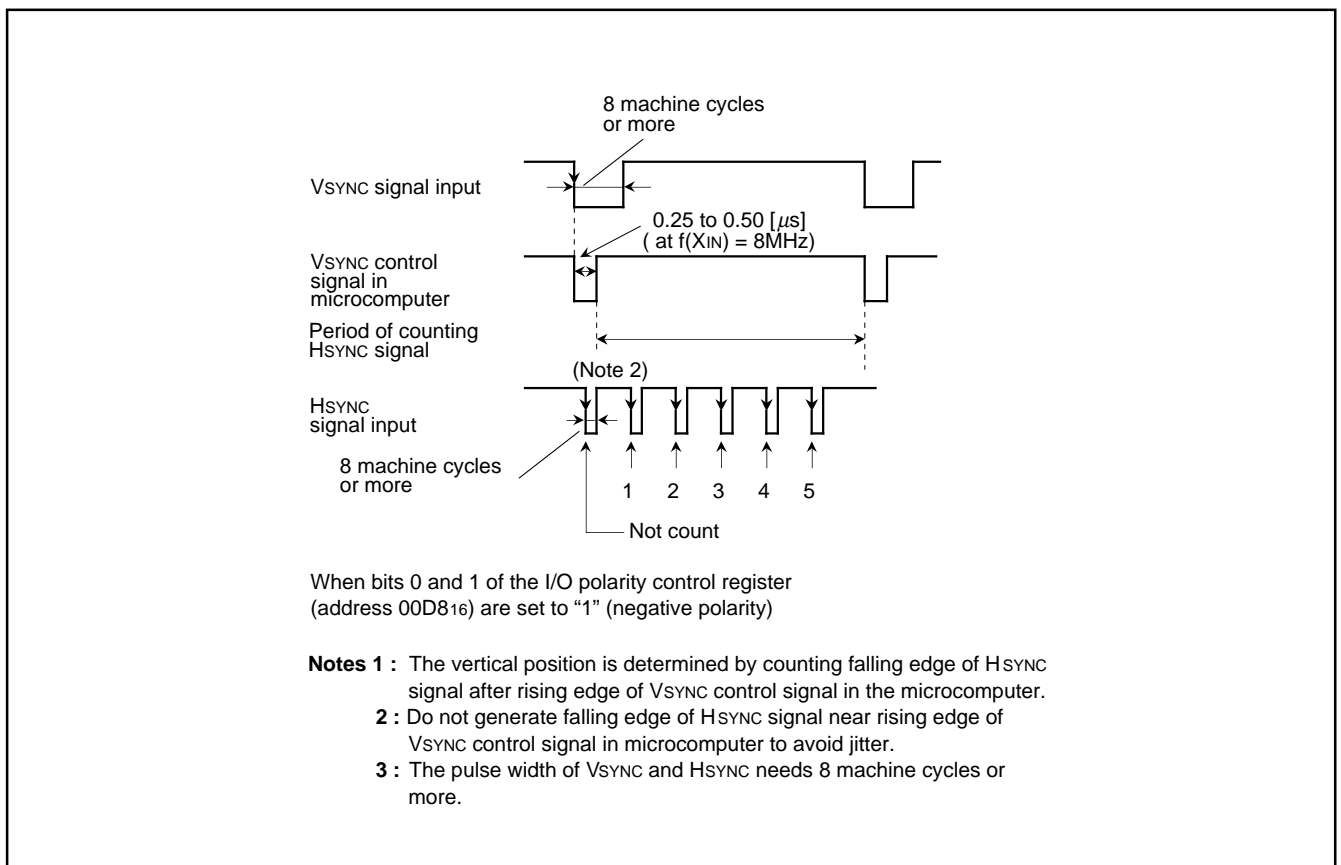


Fig. 58. Supplement Explanation for Display Position

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The vertical position for each block can be set in 512 steps (where each step is 1<sub>TH</sub> (TH: HSYNC cycle)) as values "0016" to "FF16" in vertical position register i (i = 1 and 2) (addresses 00D416 and 00D516) and values "0" or "1" in bit 6 of block control register i (i = 1 and 2) (addresses 00D216 and 00D316). The structure of the vertical position registers is shown in Figure 59.

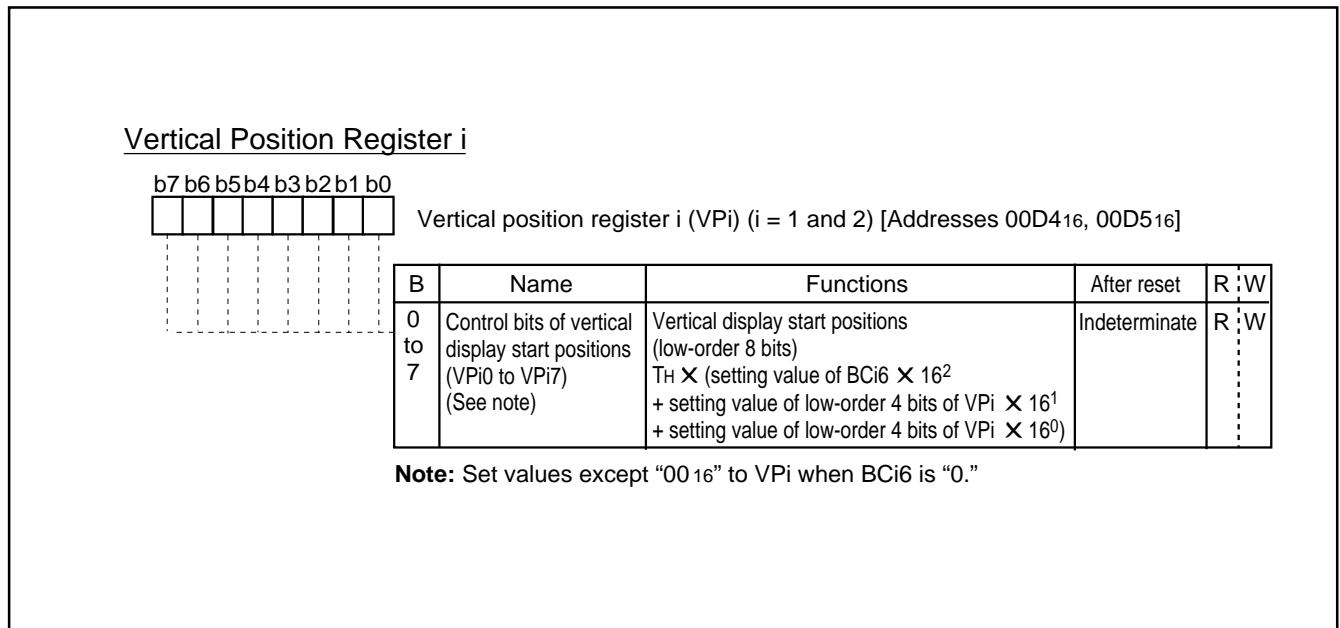


Fig. 59. Vertical Position Registers

The horizontal position is common to all blocks, and can be set in 128 steps (where 1 step is 4TOSC, TOSC being the oscillating cycle for display) as values "0016" to "FF16" in bits 0 to 6 of the horizontal position register (address 00D116). The structure of the horizontal position register is shown in Figure 60.

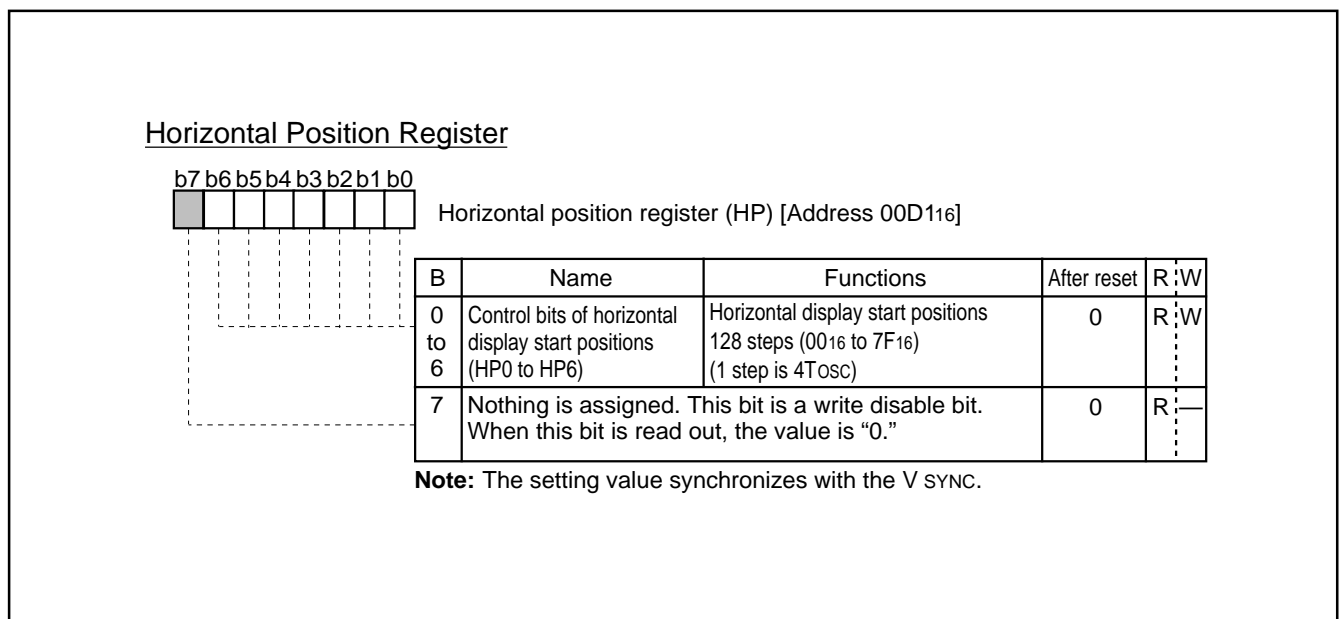


Fig. 60. Horizontal Position Register

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- Notes 1 :**  $1T_c$  ( $T_c$  : OSD clock cycle divided by prescaler) gap occurs between the horizontal display start position set by the horizontal position register and the most left dot of the 1st block. Accordingly, when 2 blocks have different pre-divide ratios, their horizontal display start position will not match.
- 2 :** The horizontal start position is based on the OSD clock source cycle selected for each block. Accordingly, when 2 blocks have different OSD clock source cycles, their horizontal display start position will not match.

- 3 :** When setting "0016" to the horizontal position register, it needs approximately  $62T_{osc}$  ( $= T_{def}$ ) interval from a rising edge (when negative polarity is selected) of HSYNC signal to the horizontal display start position.

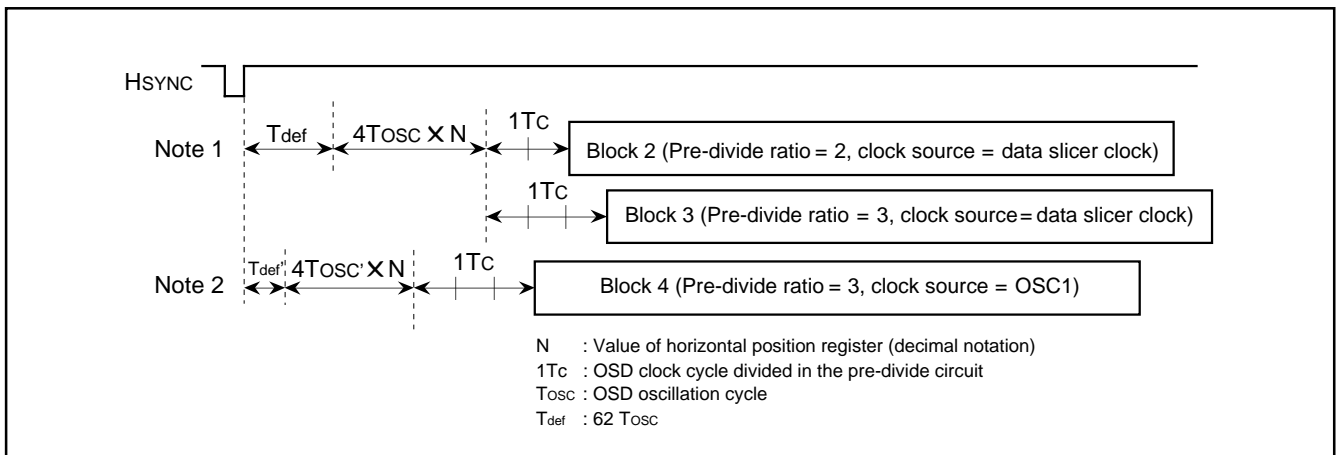


Fig. 61. Notes on Horizontal Display Start Position

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**(2) Dot Size**

The dot size can be selected by a block unit. The dot size in vertical direction is determined by dividing HSYNC in the vertical dot size control circuit. The dot size in horizontal is determined by dividing the following clock in the horizontal dot size control circuit : the clock gained by dividing the OSD clock source (data slicer clock, OSC1) in the pre-divide circuit. The clock cycle divided in the pre-divide circuit is defined as 1Tc.

The dot size of each block is specified by bits 2 to 4 of the block control register i.

Refer to Figure 56 (the structure of the block control register i).

The block diagram of dot size control circuit is shown in Figure 62.

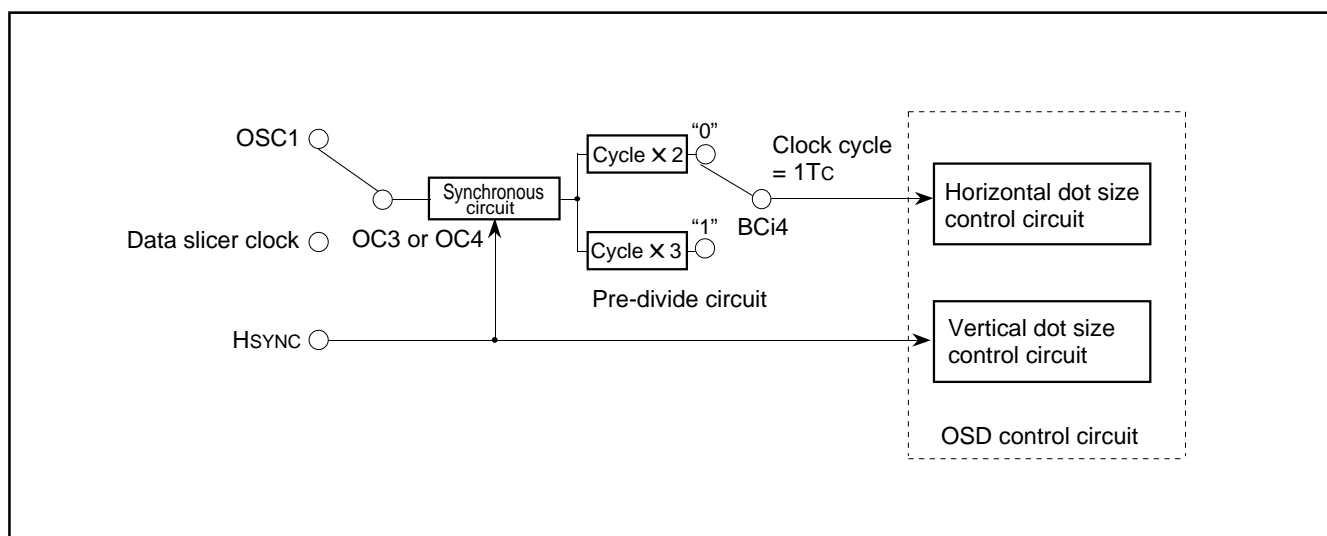


Fig. 62. Block Diagram of Dot Size Control Circuit

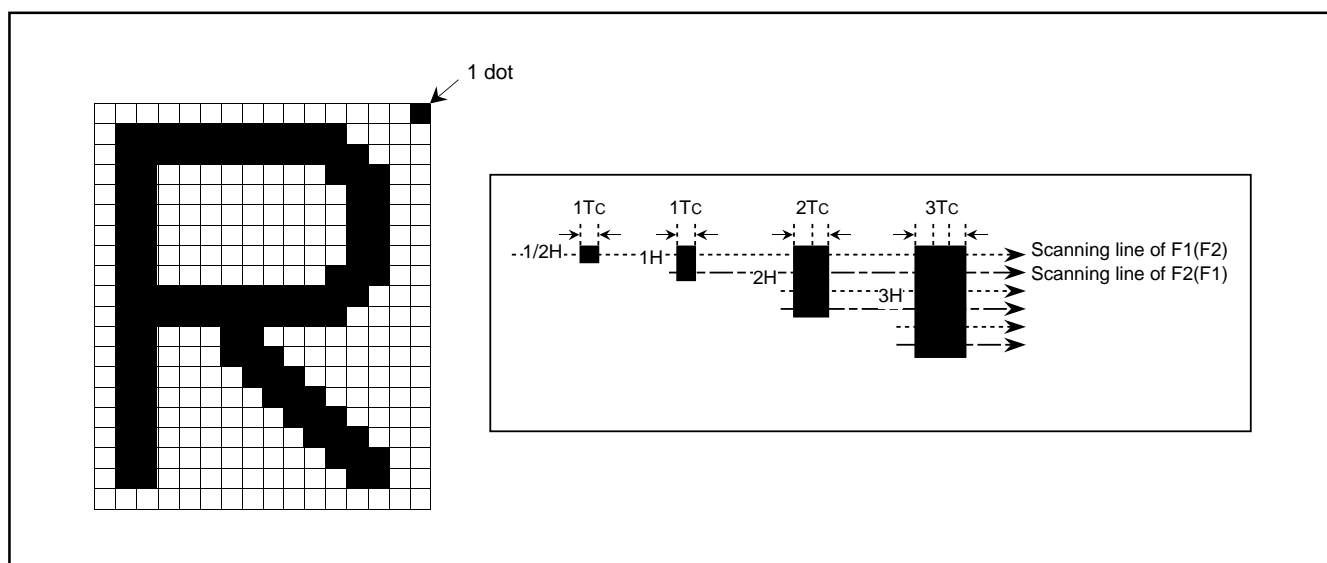


Fig. 63. Definition of Dot Sizes

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**(3) Clock for OSD**

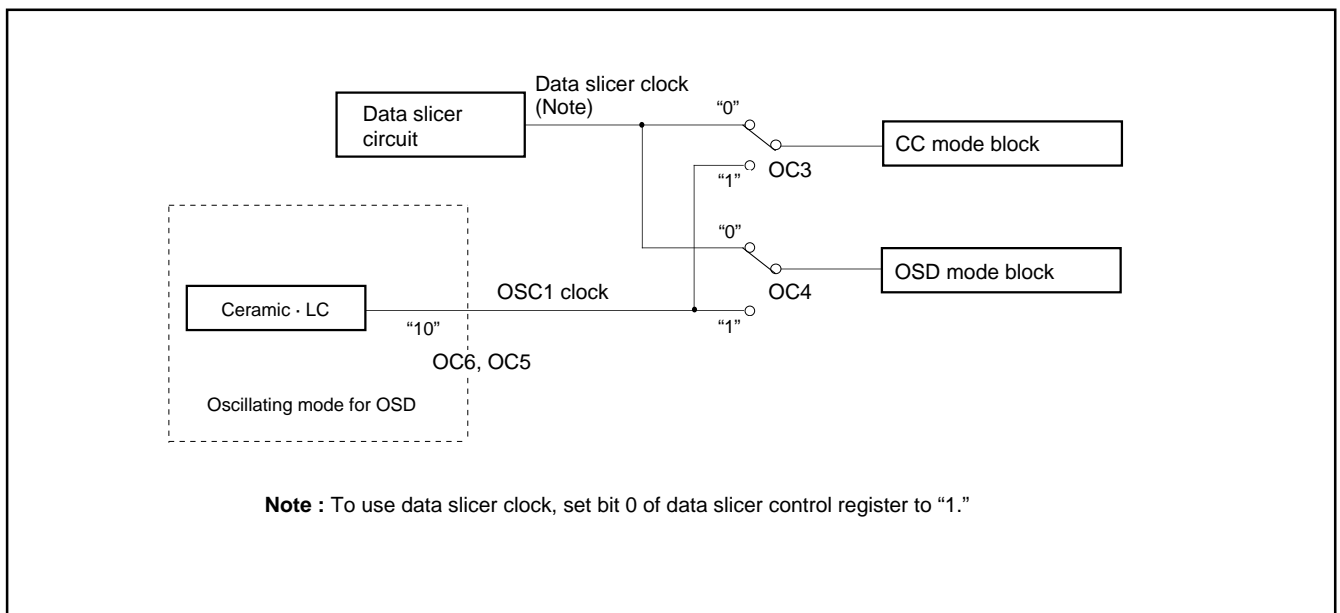
As a clock for display to be used for OSD, it is possible to select one of the following 3 types.

- Data slicer clock output from the data slicer (approximately 26 MHz)
- OSC1 clock supplied from the pins OSC1 and OSC2
- Clock from the ceramic resonator or the LC oscillator from the pins OSC1 and OSC2

This OSD clock for each block can be selected by the following bits : bit 7 of the raster color register (address 00D916), bits 3 to 6 of the clock source control register (addresses 00D016). A variety of character sizes can be obtained by combining dot sizes with OSD clocks. When not using the pins OSC1 and OSC2 for the OSD clock I/O pins, the pins can be used as sub-clock I/O pins or port P2.

**Table 9. Setting for P26/OSC1/XCIN, P27/OSC2/XCOUT**

Register	Function	OSD clock I/O Pin	Sub-clock I/O Pin	I/O Port
b7 of raster color register		0	0	1
OSD control register	b6	1	0	1
	b5	0	0	0



**Fig. 64. Block Diagram of OSD Selection Circuit**

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**(4) Field Determination Display**

To display the block with vertical dot size of 1/2H, whether an even field or an odd field is determined through differences in a synchronizing signal waveform of interlacing system. The dot line 0 or 1 (refer to Figure 66) corresponding to the field is displayed alternately. In the following, the field determination standard for the case where both the horizontal sync signal and the vertical sync signal are negative-polarity inputs will be explained. A field determination is determined by detecting the time from a falling edge of the horizontal sync signal until a falling edge of the VSYNC control signal (refer to Figure 58) in the microcomputer and then comparing this time with the time of the previous field. When the time is longer than the comparing time, it is regarded as even field. When the time is shorter, it is regarded as odd field

The contents of this field can be read out by the field determination flag (bit 6 of the I/O polarity control register at address 00D816). A dot line is specified by bit 5 of the I/O polarity control register (refer to Figure 66).

However, the field determination flag read out from the CPU is fixed to "0" at even field or "1" at odd field, regardless of bit 5.

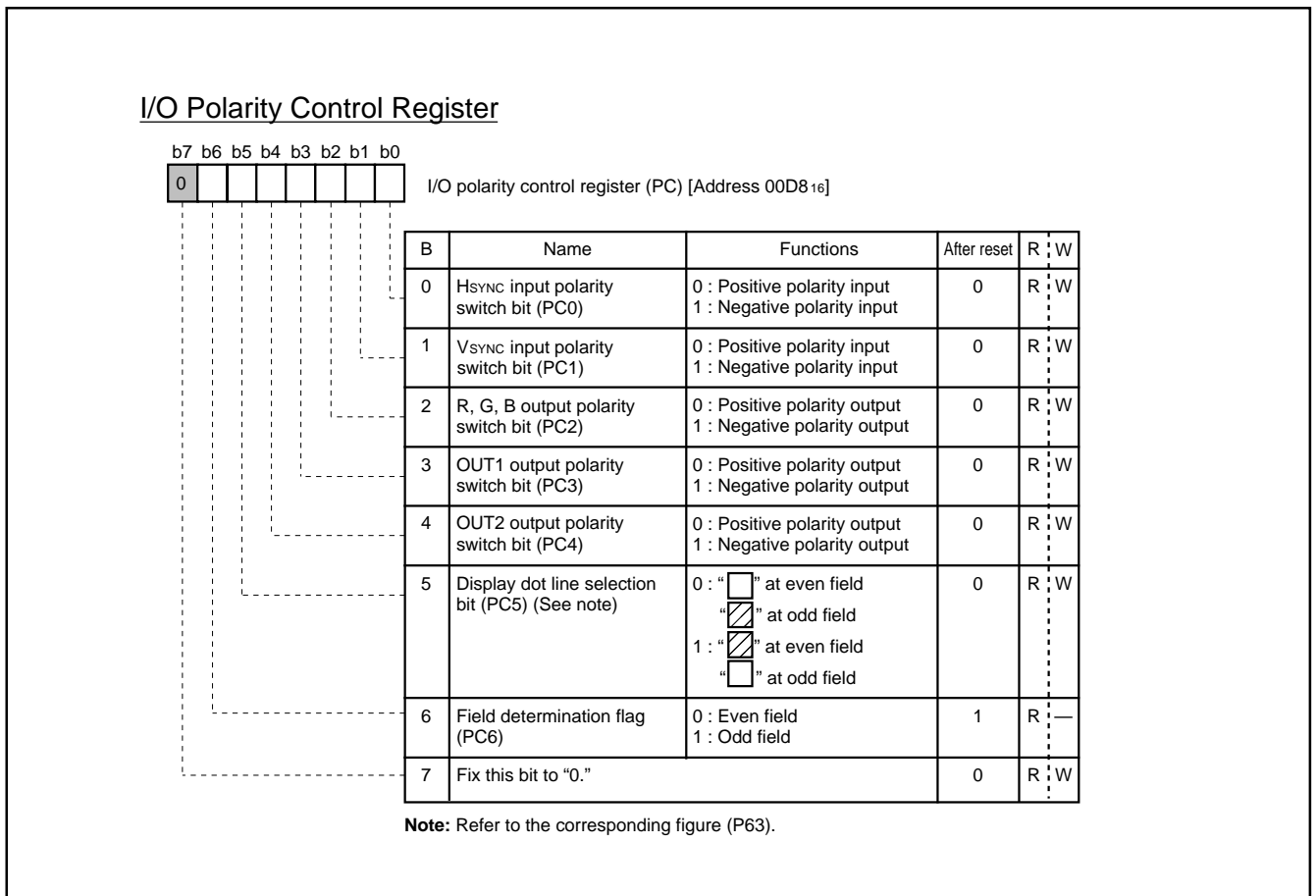


Fig. 65. I/O Polarity Control Register

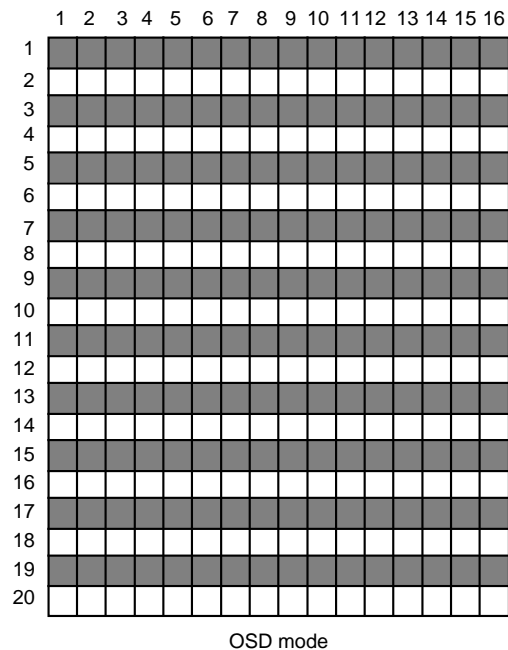
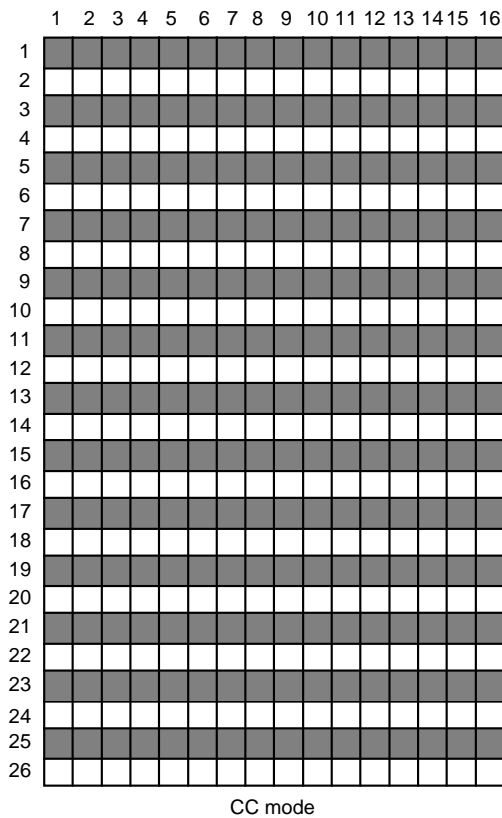
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Both Hsync signal and Vsync signal are negative-polarity input

Hsync		Field	Field determination flag(Note)	Display dot line selection bit	Display dot line
Vsync and Vsync control signal in microcomputer		Odd	/	/	/
Upper : Vsync signal		Even	0 (T2 > T1)	0	Dot line 1 <input type="checkbox"/>
				1	Dot line 0 <input checked="" type="checkbox"/>
Lower : Vsync control signal in microcomputer		Odd	1 (T3 < T2)	0	Dot line 0 <input checked="" type="checkbox"/>
				1	Dot line 1 <input type="checkbox"/>

When using the field determination flag, be sure to set bit 0 of the PWM mode register 1 (address 020816) to "0."



When the display dot line selection bit is "0," the "□" font is displayed at even field, the "■" font is displayed at odd field. Bit 6 of the I/O polarity control register can be read as the field determination flag : "1" is read at odd field, "0" is read at even field.

OSD ROM font configuration diagram

**Note :** The field determination flag changes at a rising edge of the V sync control signal (negative-polarity input) in the microcomputer.

Fig. 66. Relation between Field Determination Flag and Display Font

**(5) Memory for OSD**

There are 2 types of memory for OSD : ROM for OSD (addresses 11400<sub>16</sub> to 13BFF<sub>16</sub>) used to store character dot data (masked) and RAM for OSD (addresses 0800<sub>16</sub> to 087F<sub>16</sub>) used to specify the characters and colors to be displayed. The following describes each type of memory.

① **ROM for OSD (addresses 11400<sub>16</sub> to 13BFF<sub>16</sub>)**

The ROM for OSD contains dot pattern data for characters to be displayed. To actually display the character code stored in this ROM, it is necessary to specify them by writing the character code inherent to each character (code determined based on the addresses in the ROM for OSD) into the RAM for OSD.

Data of the character font is specified shown in Figure 67.

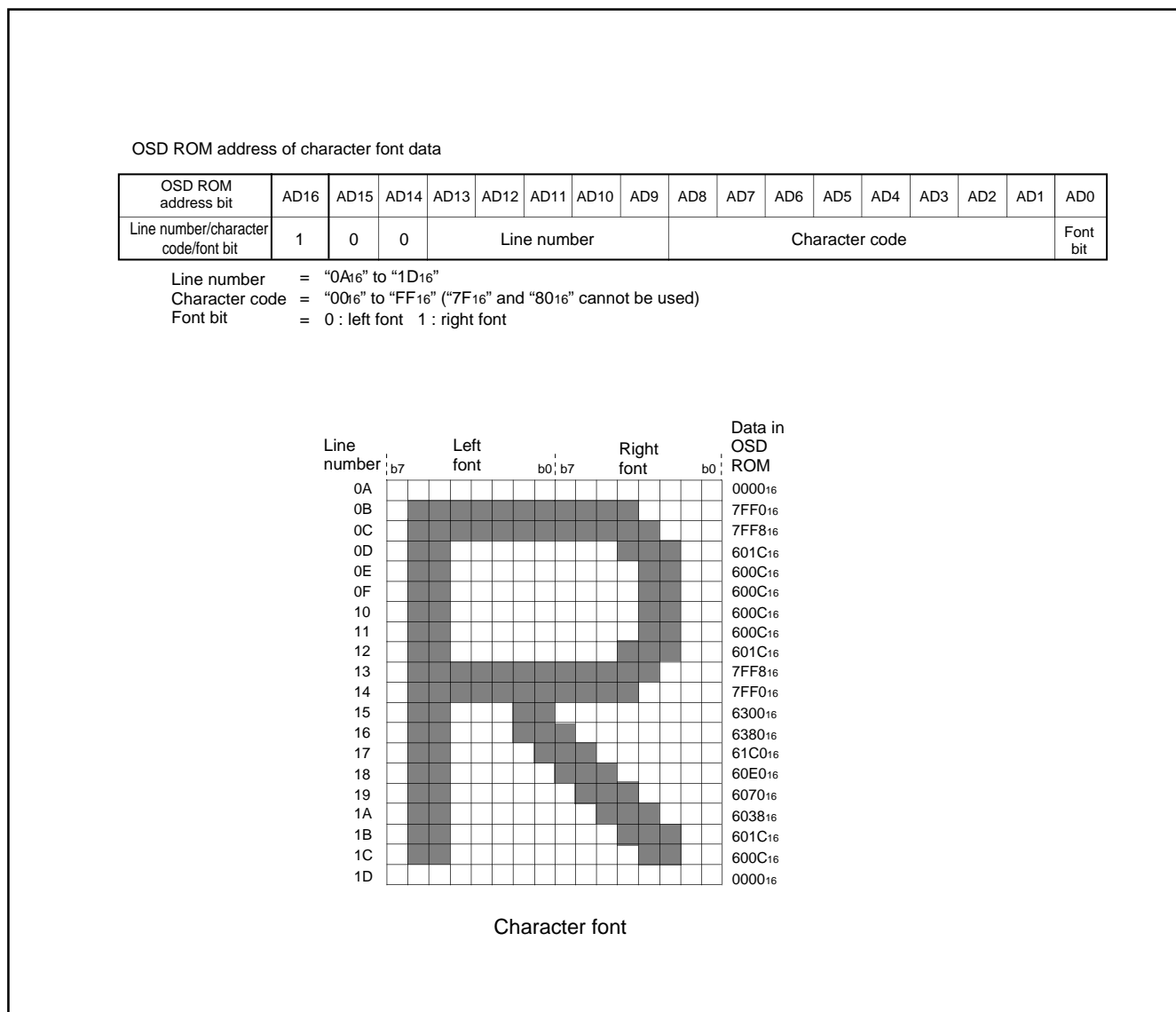


Fig. 67. OSD Character Data Storing Form



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**Notes 1 :** The 80-byte addresses corresponding to the character code "7F<sub>16</sub>" and "80<sub>16</sub>" in OSD ROM are the test data storing area. Set "FF<sub>16</sub>" to the area. (We stores the test data to this area and the different data from "FF<sub>16</sub>" is stored for the actual products.)

The test data storing area :  
addresses 11000<sub>16</sub> + (4 + 2n) X 100<sub>16</sub> + FE<sub>16</sub> to  
11000<sub>16</sub> + (5 + 2n) X 100<sub>16</sub> + 01<sub>16</sub>  
(n = 0 to 19)

addresses 114FE<sub>16</sub> to 11501<sub>16</sub>  
 addresses 116FE<sub>16</sub> to 11701<sub>16</sub>  
 ⋮  
 addresses 138FE<sub>16</sub> to 13901<sub>16</sub>  
 addresses 13AFE<sub>16</sub> to 13B01<sub>16</sub>

**2 :** The character code "09<sub>16</sub>" is used for "transparent space" when displaying Closed Caption. Therefore, set "00<sub>16</sub>" to the 40-byte addresses corresponding to the character code "09<sub>16</sub>."

The transparent space font data storing area :  
addresses 11000<sub>16</sub> + (4 + 2n) X 100<sub>16</sub> + 12<sub>16</sub> to  
11000<sub>16</sub> + (4 + 2n) X 100<sub>16</sub> + 13<sub>16</sub>  
(n = 0 to 19)

addresses 11412<sub>16</sub> and 11413<sub>16</sub>  
 addresses 11612<sub>16</sub> and 11613<sub>16</sub>  
 ⋮  
 addresses 13812<sub>16</sub> and 13813<sub>16</sub>  
 addresses 13A12<sub>16</sub> and 13A13<sub>16</sub>

② **RAM for OSD (addresses 0800<sub>16</sub> to 087F<sub>16</sub>)**

The RAM for OSD is allocated at addresses 0800<sub>16</sub> to 087F<sub>16</sub>, and is divided into a display character code specification part, color code 1 specification part, and color code 2 specification part for each block.

Table 13 shows the contents of the RAM for OSD.

For example, to display 1 character position (the left edge) in block 1, write the character code in address 0800<sub>16</sub>, write the color code 1 at 0820<sub>16</sub>.

The structure of the RAM for OSD is shown in Figure 68.

**Table 10. Contents of OSD RAM**

Block	Display Position (from left)	Character Code Specification	Color Code Specification
Block 1	1st character	0800 <sub>16</sub>	0820 <sub>16</sub>
	2nd character	0801 <sub>16</sub>	0821 <sub>16</sub>
	3rd character	0802 <sub>16</sub>	0822 <sub>16</sub>
	⋮	⋮	⋮
	30th character	081D <sub>16</sub>	083D <sub>16</sub>
	31st character	081E <sub>16</sub>	083E <sub>16</sub>
Block 2	32nd character	081F <sub>16</sub>	083F <sub>16</sub>
	1st character	0840 <sub>16</sub>	0860 <sub>16</sub>
	2nd character	0841 <sub>16</sub>	0861 <sub>16</sub>
	3rd character	0842 <sub>16</sub>	0862 <sub>16</sub>
	⋮	⋮	⋮
	30th character	085D <sub>16</sub>	087D <sub>16</sub>
Block 2	31st character	085E <sub>16</sub>	087E <sub>16</sub>
	32nd character	085F <sub>16</sub>	087F <sub>16</sub>

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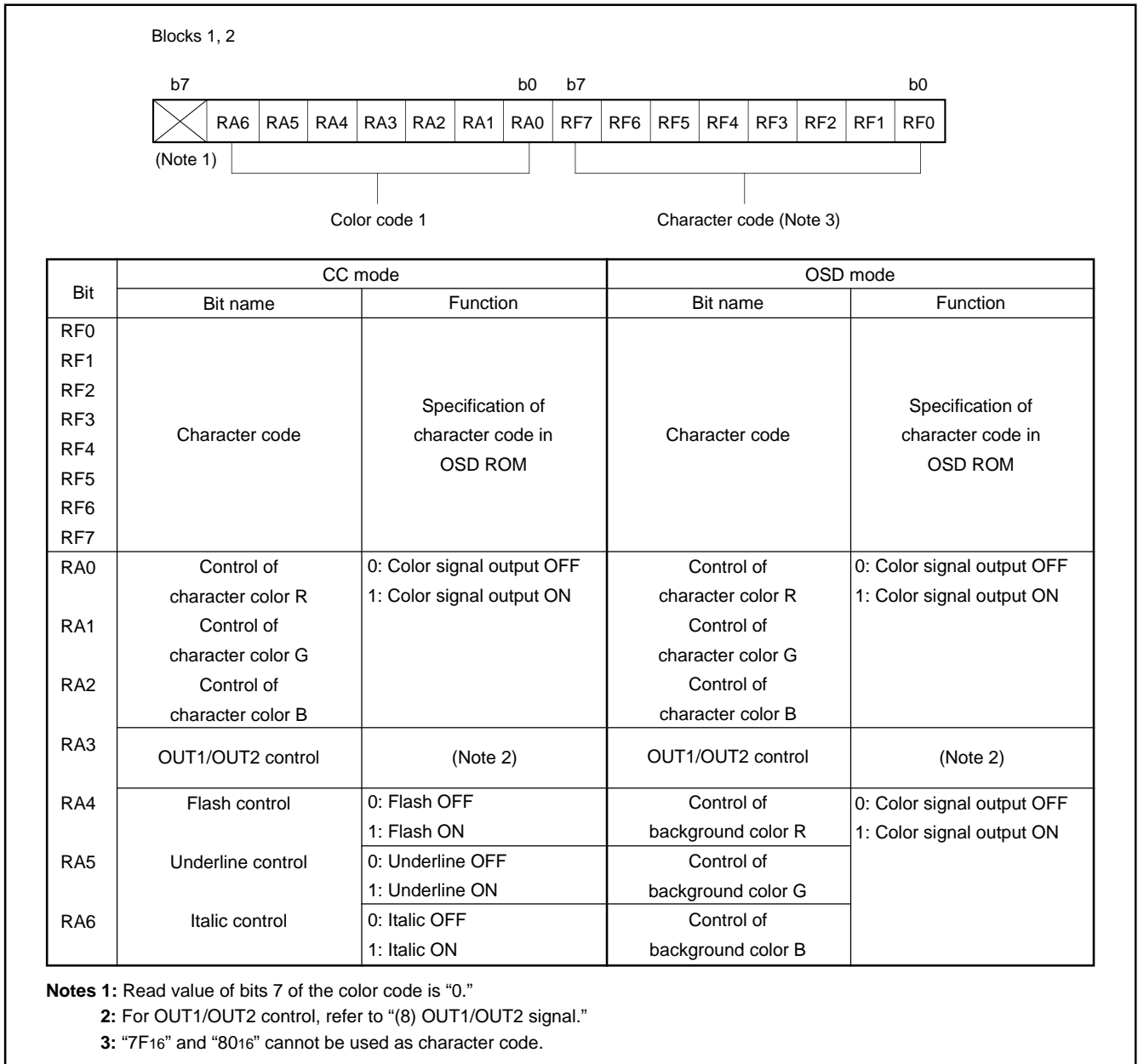


Fig. 68. OSD RAM

**(6) Character color**

The color for each character is displayed by the color code. The kinds and specification method of character color are different depending on each mode.

- CC mode ) .....7 kinds
- OSD mode ) Specified by bits 0 (R), 1 (G), and 2 (B) of the color code

**(7) Character background color**

The character background color can be displayed in the character display area only in the OSD mode. The character background color for each character is specified by the color code. The kinds and specification method of character background color are different depending on each mode.

- OSD mode ..... 7 kinds
- Specified by bits 4 (R), 5 (G), and 6 (B) of the color code

**Note :** The character background color is displayed in the following part :  
 (character display area)–(character font)–(border).  
 Accordingly, the character background color does not mix with these color signal.

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**(8) OUT1, OUT2 signals**

The OUT1, OUT2 signals are used to control the luminance of the video signal. The output waveform of the OUT1, OUT2 signals is controlled by display mode, bit 3 (RA3) of color code (refer to Figure 65), bit 5 of the block control register i (refer to Figure 54). The set-

ting values for controlling OUT1, OUT2 and the corresponding output waveform is shown in Figure 69.

**Note :** When OUT2 signal is output, set bit 7 of OSD port control register to "1."

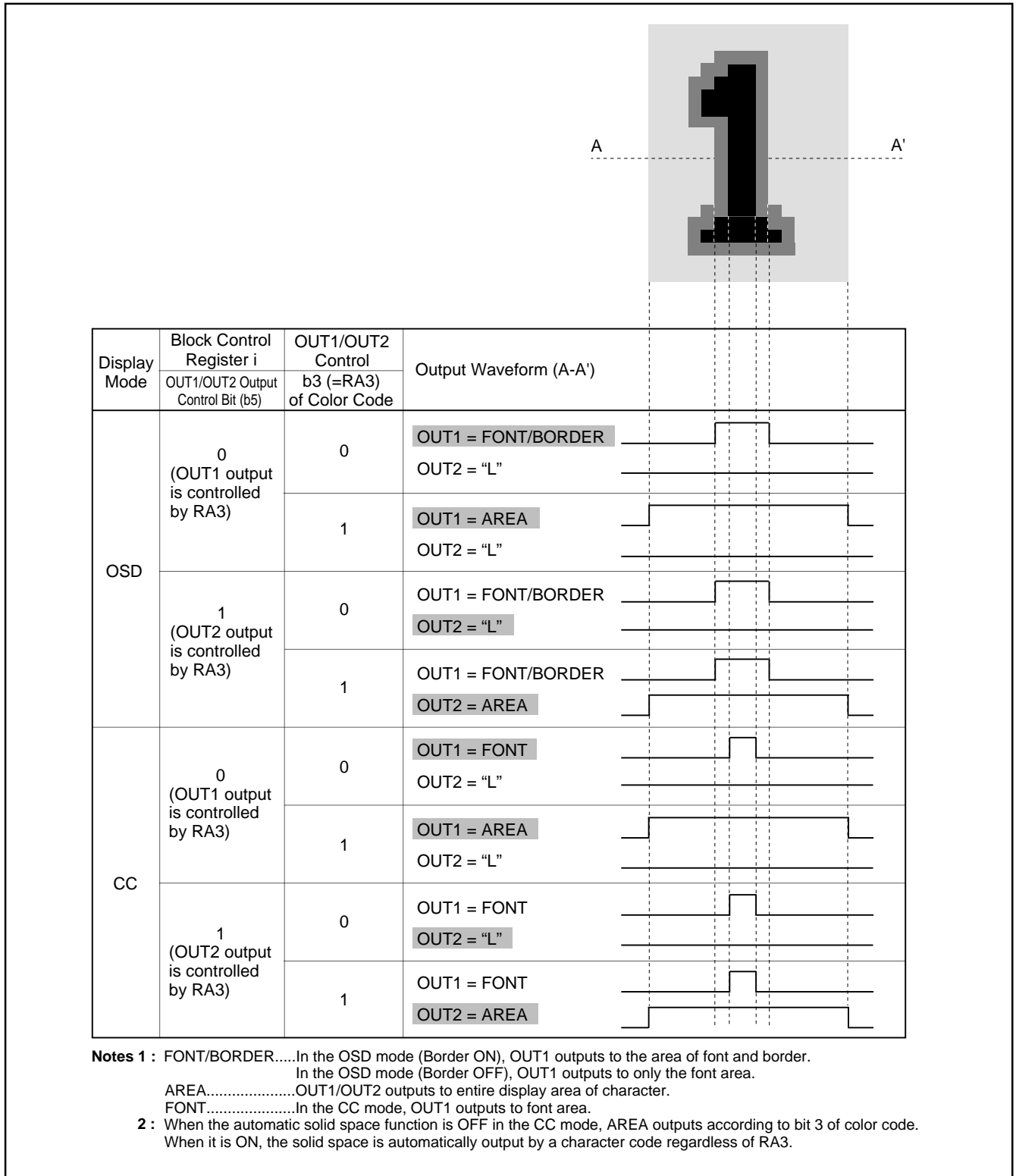


Fig. 69. Setting Value for Controlling OUT1, OUT2 and Corresponding Output Waveform

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**(9) Attribute**

The attributes (border, flash, underline, italic) are controlled to the character font. The attributes for each character are specified by the color code (refer to Figure 68). The attributes to be controlled are different depending on each mode.

CC mode ..... Flash, underline, italic  
OSD mode ..... Border

① **Under line**

The underline is output at the 23th and 24th dots in vertical direction only in the CC mode. The underline is controlled by bit 5 of the color code. The color of underline is the same color as that of the character font.

② **Flash**

The parts of the character font, the underline, and the character background are flashed only in the CC mode. The color signals (R, G, B, OUT1) of the character font and the underline are controlled by bit 5 of the color code. The character font part (solid box) is not flashed. The flash cycle bases on the VSYNC count.

- VSYNC cycle X 48 = 800 ms (at display ON)
- VSYNC cycle X 16 = 267 ms (at display OFF)

③ **Italic**

The italic is made by slanting the font stored in OSD ROM to the right only in the CC mode. The italic is controlled by bit 6 of the color code.

The display example of the italic and underline is shown in Figure 70. In this case, "R" is displayed.

**Notes 1:** When setting both the italic and the flash, the italic character flashes.

**2:** The adjacent character (one side or both side) to an italic character is displayed in italic even when the character is not specified to display in italic (refer to Figure 71).

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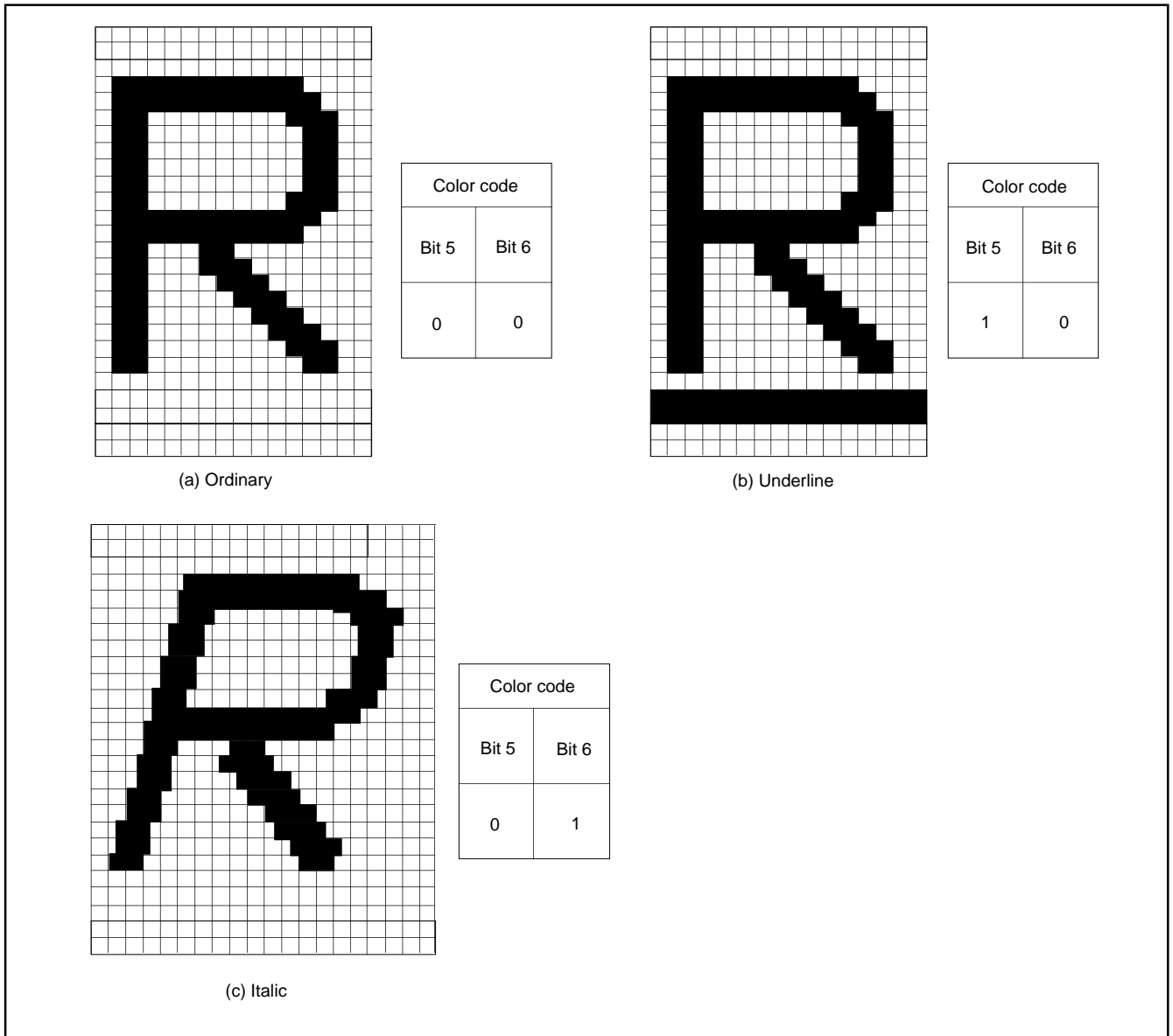


Fig. 70. Example of Attribute Display (in CC Mode)

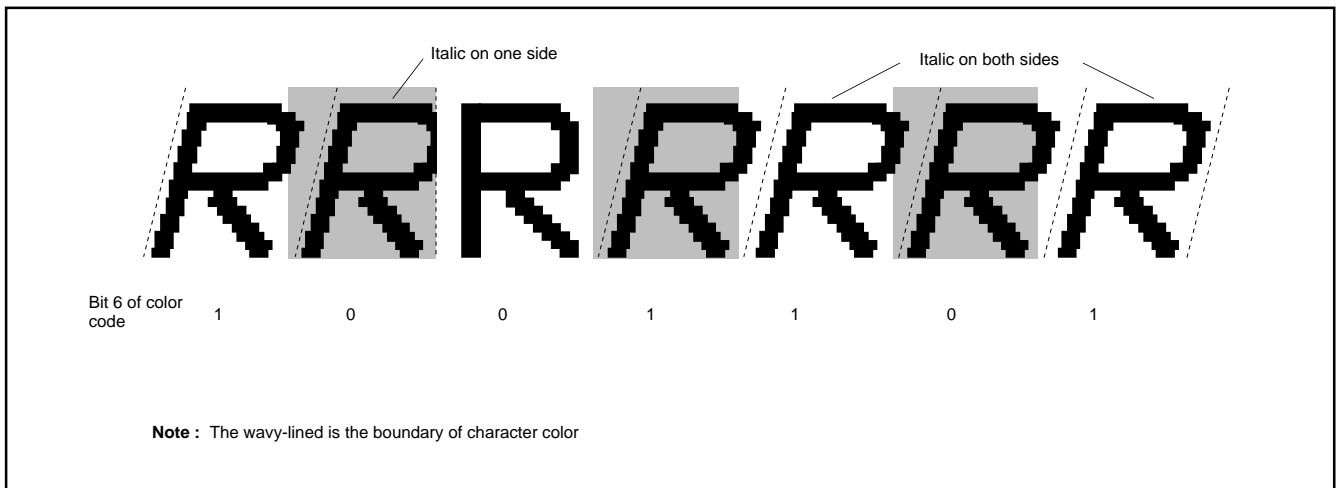


Fig. 71. Example of Italic Display

④ **Border**

The border is output around of character font (all bordered) in the OSD mode. The border ON/OFF is controlled by bit 0 and 1 of the block control register i (refer to Figure 56).

The OUT1 signal is used for border output.

The horizontal size (x) of border is 1Tc (OSD clock cycle divided in the pre-divide circuit) regardless of the character font dot size. The vertical size (y) different depending on the screen scan mode and the vertical dot size of character font.

**Notes 1** : The border dot area is the shaded area as shown in Figure 72.

**2** : When the border dot overlaps on the next character font, the character font has priority (refer to Figure 74 A).  
When the border dot overlaps on the next character background, the border has priority (refer to Figure 74 B).

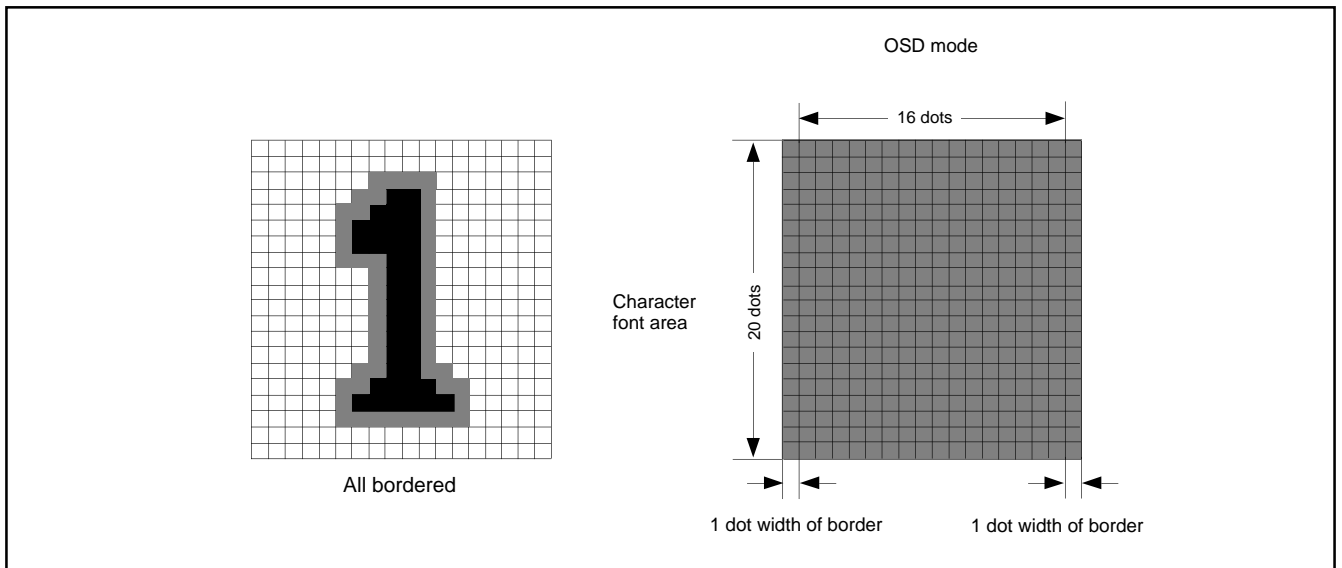


Fig. 72. Example of Border Display

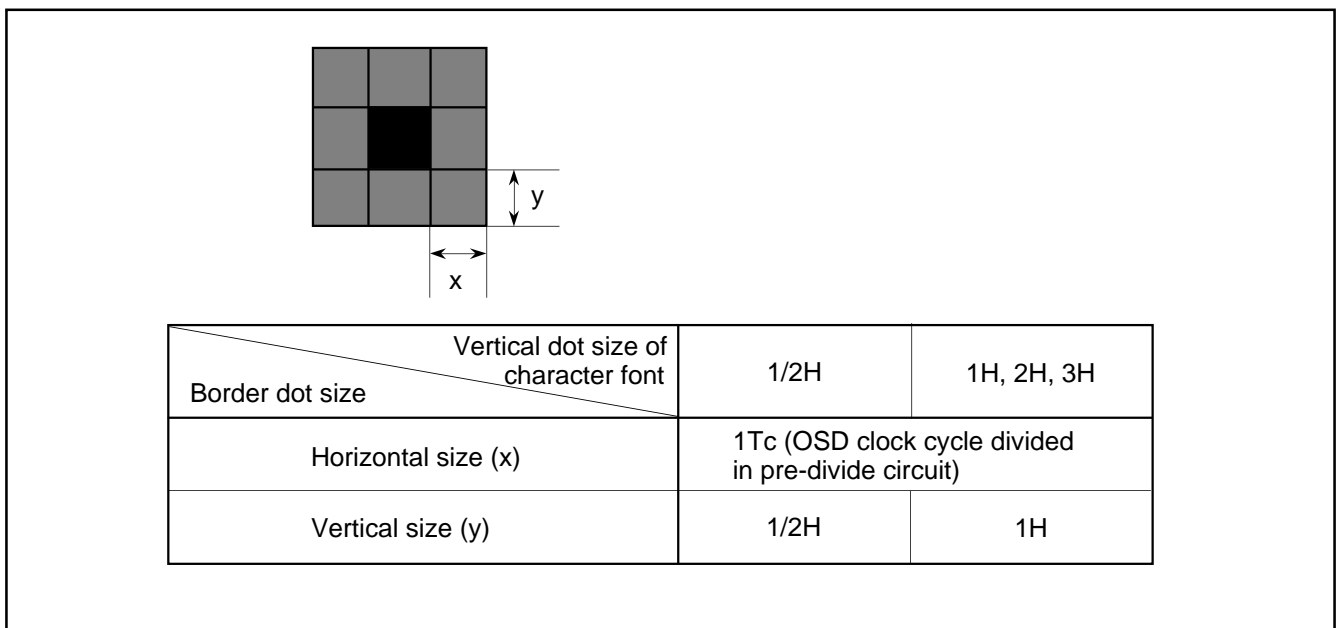


Fig. 73. Horizontal and Vertical Size of Border

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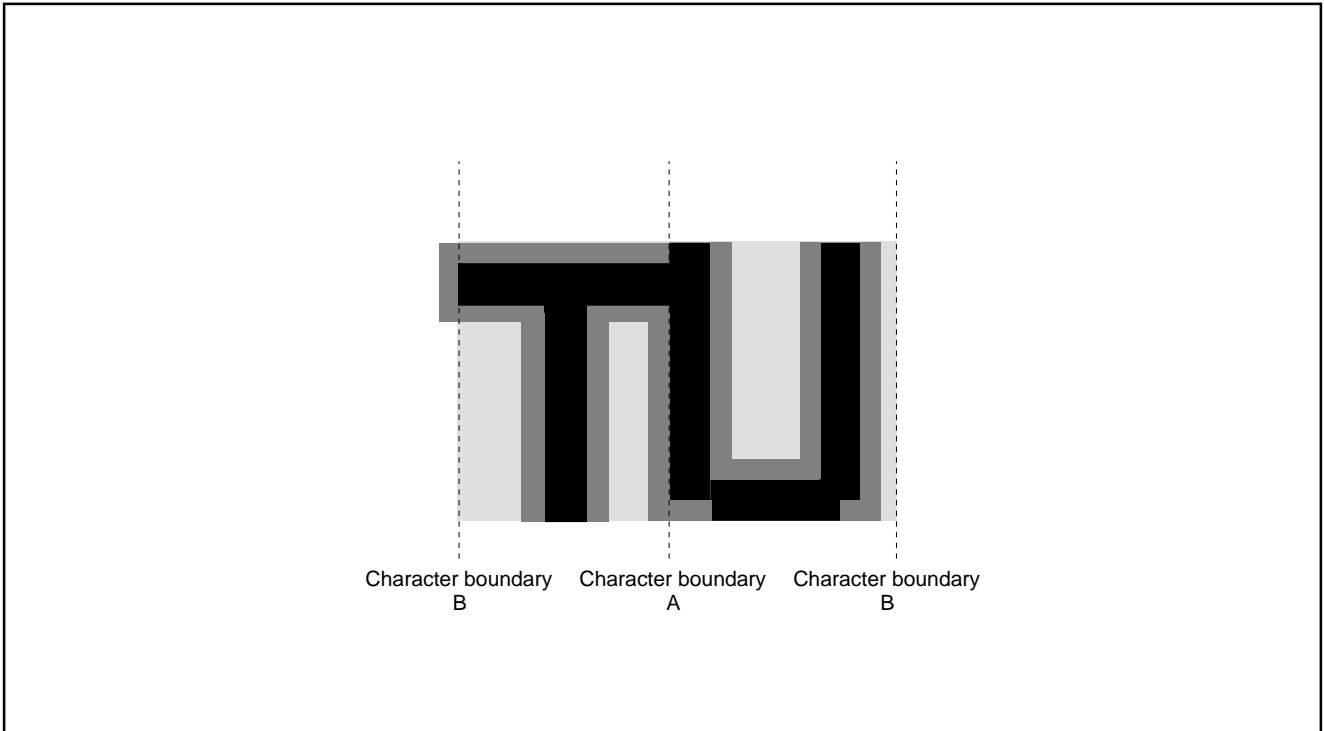


Fig. 74. Border Priority

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**(10) Multiline Display**

The M37273MF-XXXSP can ordinarily display 2 lines on the CRT screen by displaying 2 blocks at different vertical positions. In addition, it can display up to 16 lines by using OSD interrupts.

An OSD interrupt request occurs at the point at which display of each block has been completed. In other words, when a scanning line reaches the point of the display position (specified by the vertical position registers) of a certain block, the character display of that block starts, and an interrupt occurs at the point at which the scanning line exceeds the block.

- Notes 1:** An OSD interrupt does not occur at the end of display when the block is not displayed. In other words, if a block is set to off display by the display control bit of the block control register (addresses 00D216, 00D316), an OSD interrupt request does not occur (refer to Figure 75 (A)).
- 2:** When another block display appears while one block is displayed, an OSD interrupt request occurs only once at the end of the another block display (refer to Figure 75 (B)).
- 3:** On the screen setting window, an OSD interrupt occurs even at the end of the CC mode block (off display) out of window (refer to Figure 75 (C)).

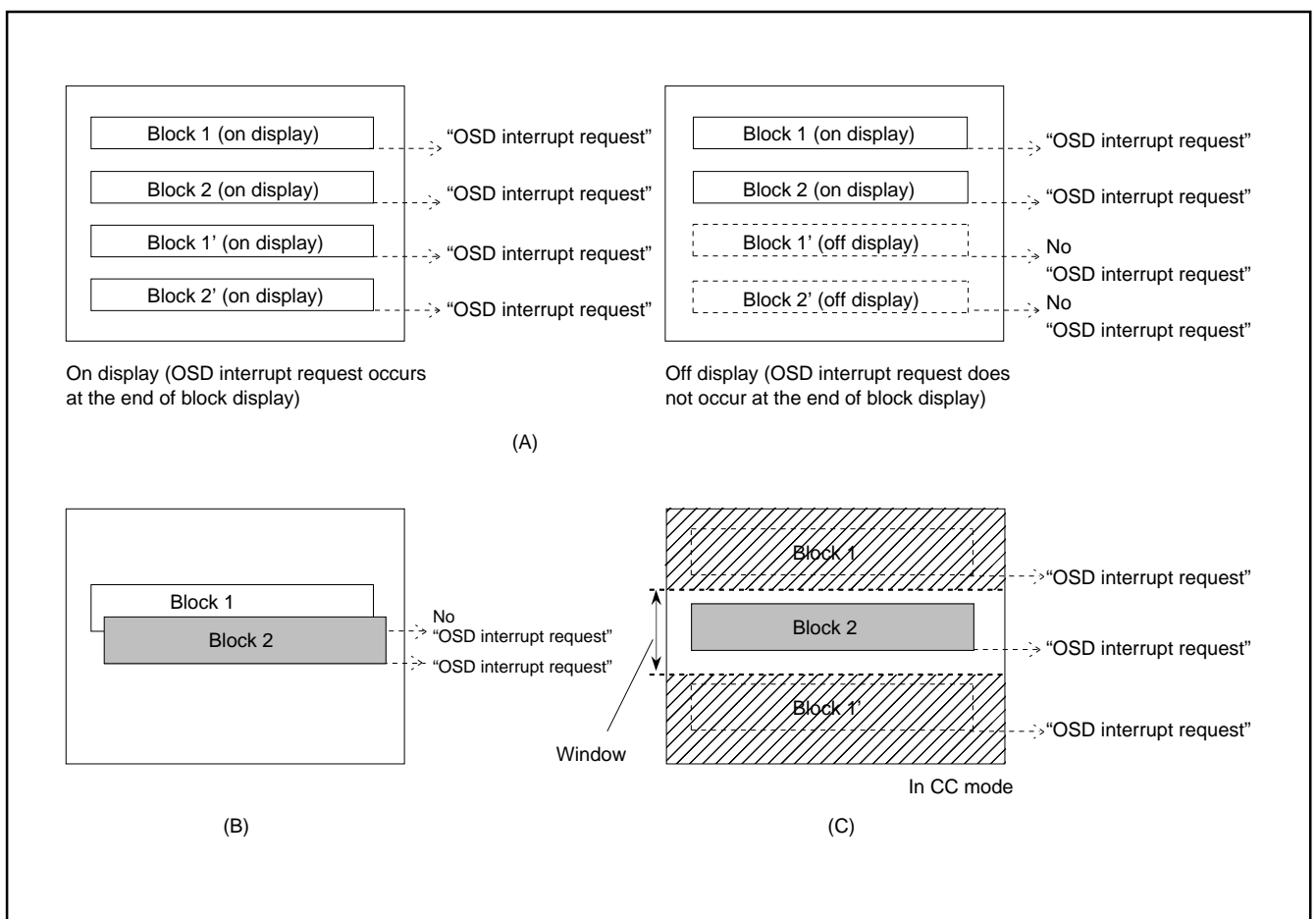


Fig. 75. Note on Occurrence of OSD Interrupt



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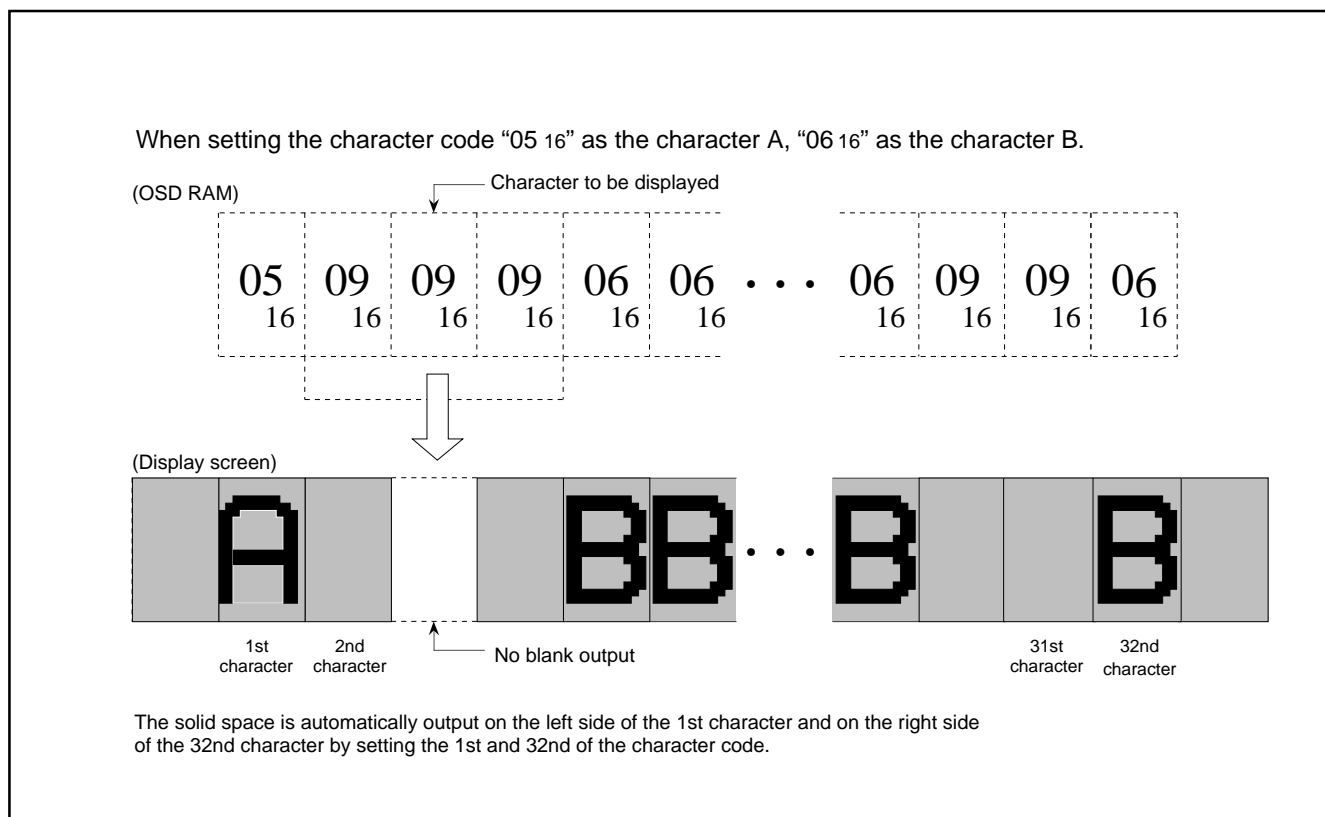
**(11) Automatic Solid Space Function**

This function generates automatically the solid space (OUT1 or OUT2 blank output) of the character area in the CC mode.

The solid space is output in the following area :

- the character area except character code "09<sub>16</sub>"
- the character area on the left and right sides of character code "09<sub>16</sub>"

This function is turned on and off by bit 1 of the OSD control register (refer to Figure 55).



**Fig. 76. Display Screen Example of Automatic Solid Space**

**Note :** The character code "09<sub>16</sub>" is used for "transparent space" when displaying Closed Caption.

Therefore, set "00<sub>16</sub>" to the 40-byte addresses corresponding to the character code "09<sub>16</sub>."

The transparent space font data storing area :

addresses 11000<sub>16</sub> + (4 + 2n) X 100<sub>16</sub> + 12<sub>16</sub> to  
11000<sub>16</sub> + (4 + 2n) X 100<sub>16</sub> + 13<sub>16</sub>

(n = 0 to 19)

[ addresses 11412<sub>16</sub> and 11413<sub>16</sub>  
addresses 11612<sub>16</sub> and 11613<sub>16</sub>  
⋮  
addresses 13812<sub>16</sub> and 13813<sub>16</sub>  
addresses 13A12<sub>16</sub> and 13A13<sub>16</sub> ]

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**(12) Window Function**

This function sets the top and bottom boundary of display limit on a screen. The window function is valid only in the CC mode. The top boundary is set by the window registers 1 and bit 7 of block control register 1. The bottom boundary is set by window registers 1 and bit 7 of block control register 2. This function is turned on and off by bit 2 of the OSD control register (refer to Figure 55).

The structure of window registers 1 and 2 is shown in Figure 78 and 79.

- Notes 1:** Do not set values except "0016" to the window register 1 when bit 7 of block control register 1 is "0."  
**2:** Set the register value fit for the following condition :  
 (Value of top boundary of window) < (Value of bottom boundary of window)

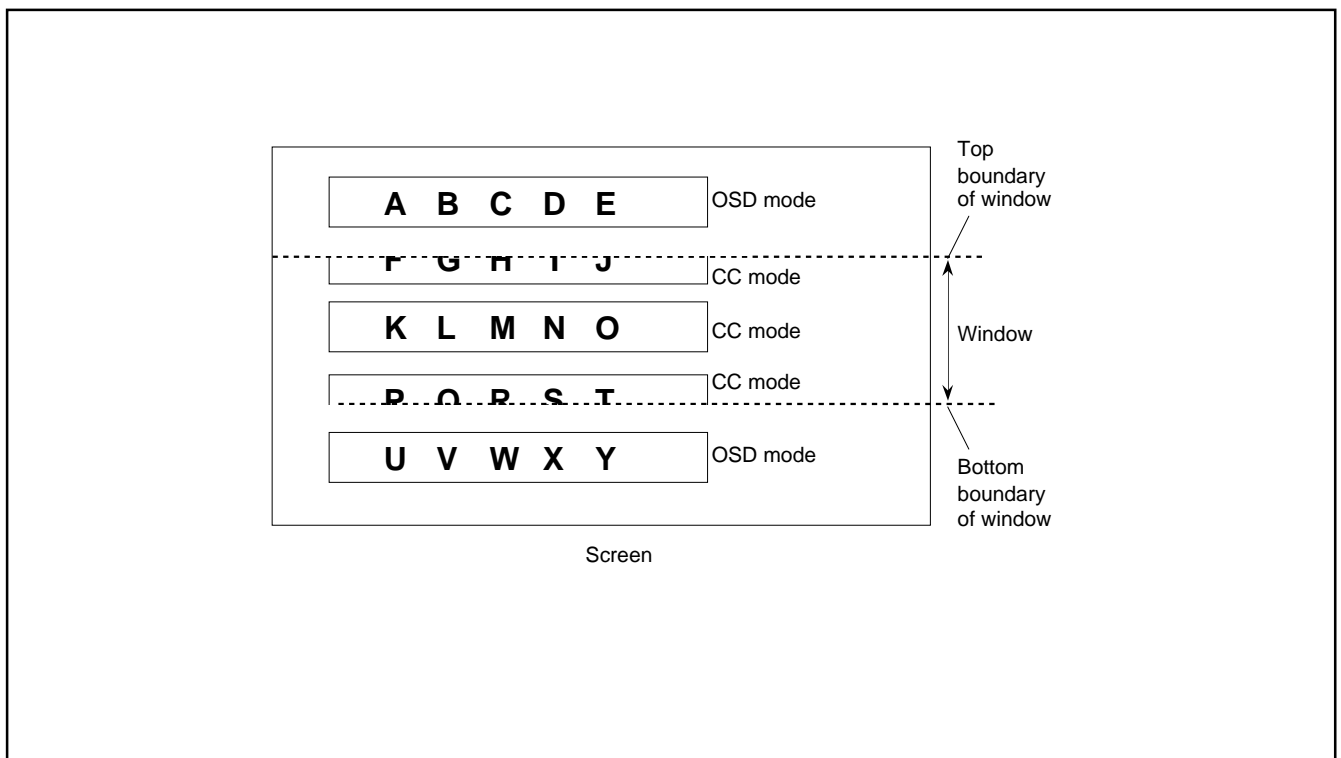


Fig. 77. Example of Window Function

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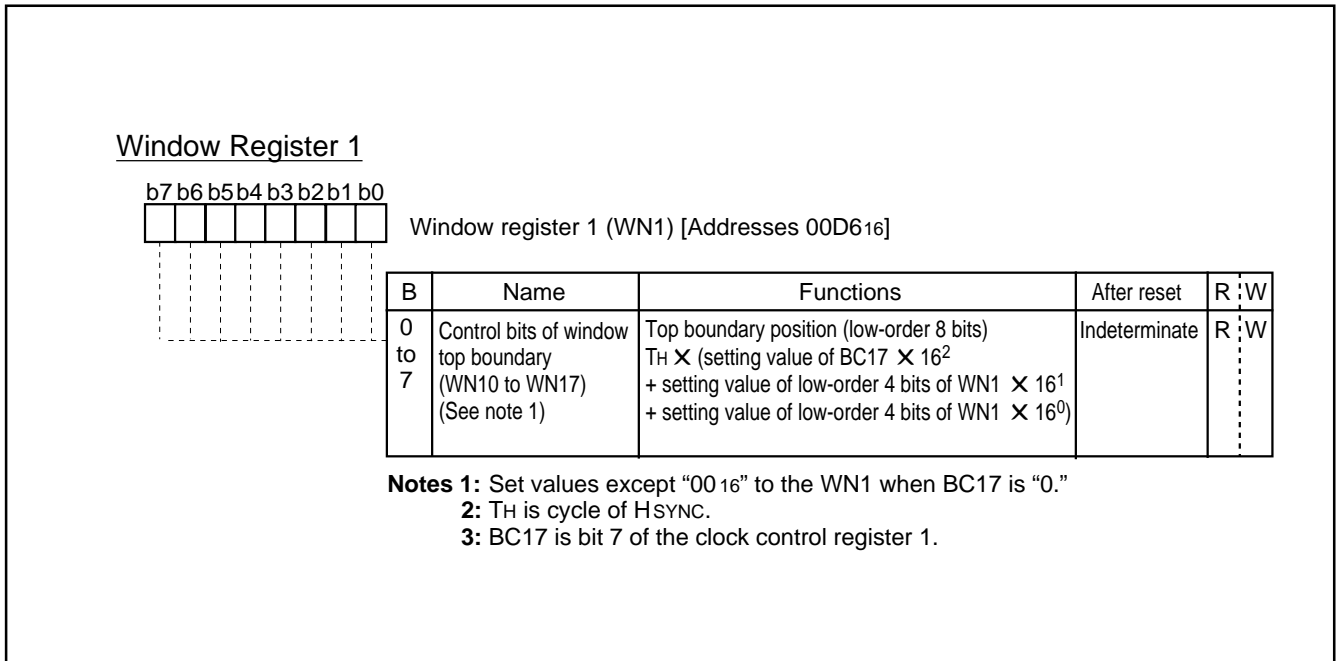


Fig. 78. Window Register 1

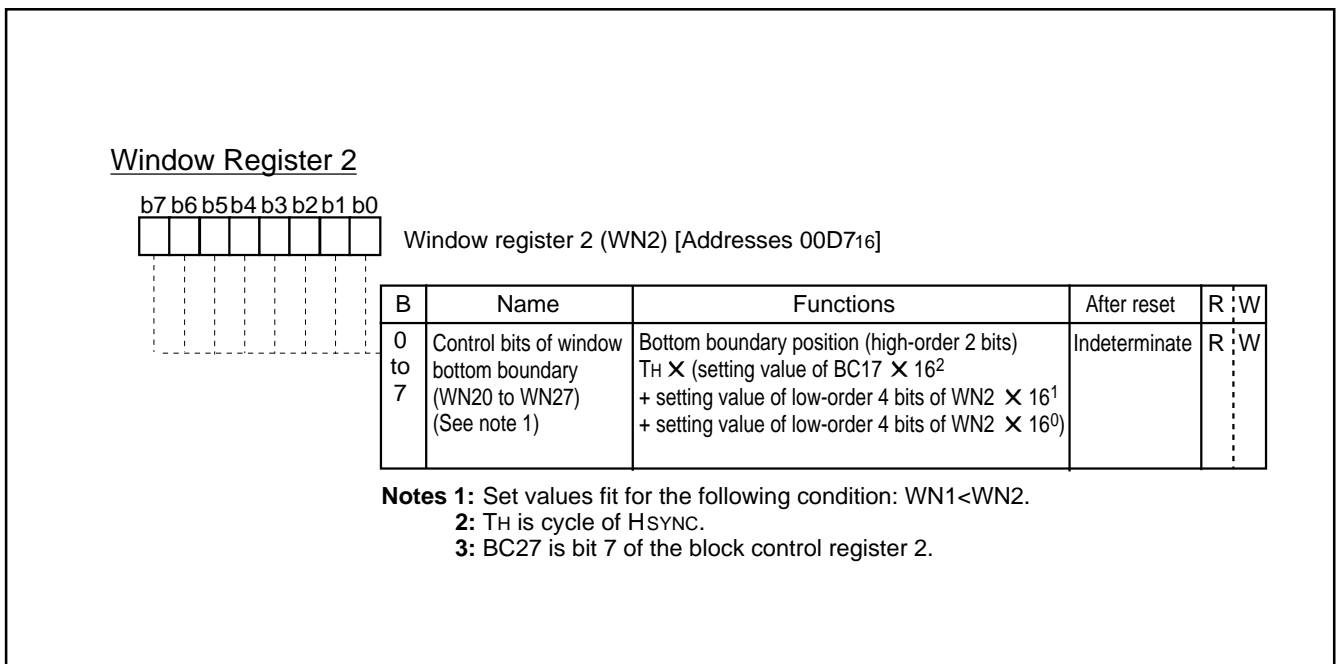


Fig. 79. Window Register 2

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**(13) OSD Output Pin Control**

The OSD output pins R, G, B, OUT1, and OUT2 can also function as ports P52, P53, P54, P55, and P10. When using OUT2 pin, set bit 0 of the port P1 direction register (address 00C316) to "1" (output mode). After that, switch between the OSD output function and the port function by the OSD port control register.

The input polarity of the HSYNC, VSYNC and output polarity of signals R, G, B, OUT1 and OUT2 can be specified with the I/O polarity control register (address 00D8) . Set a bit to "0" to specify positive polarity; set it to "1" to specify negative polarity (refer to Figure 65).

The structure of the OSD port control register is shown in Figure 80.

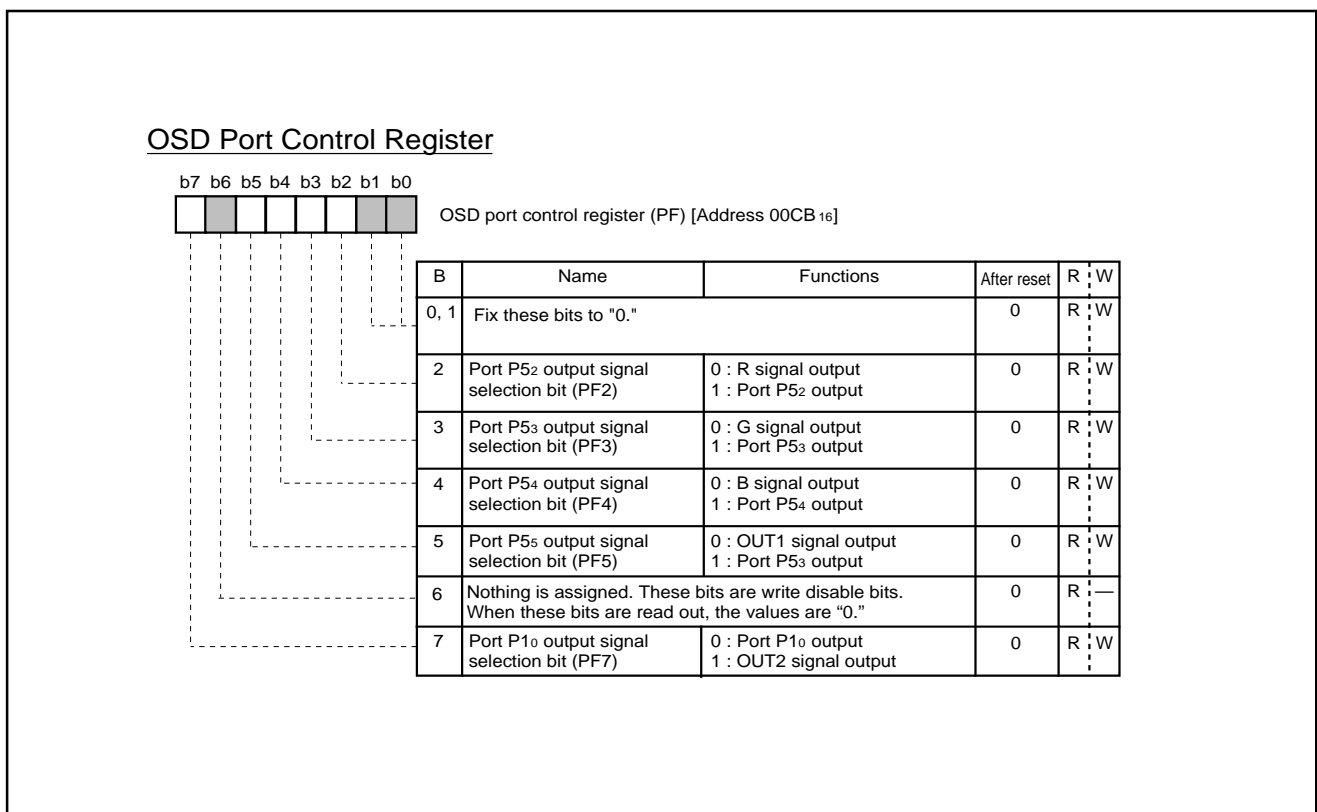


Fig. 80. OSD Port Control Register

**(14) Raster Coloring Function**

An entire screen (raster) can be colored by setting the bits 4 to 0 of the raster color register. Since each of the R, G, B, OUT1, and OUT2 pins can be switched to raster coloring output, 7 raster colors can be obtained.

If the OUT1 pin has been set to raster coloring output, a raster coloring signal is always output during 1 horizontal scanning period. This setting is necessary for erasing a background TV image.

If the R, G, and B pins have been set to output, a raster coloring signal is output in the part except a no-raster colored character (in Figure 81, a character "1") and the character background output during 1 horizontal scanning period. This ensures that character color/character background color is not mixed with the raster color.

The structure of the raster color register is shown in Figure 82, the example of raster coloring is shown in Figure 81.

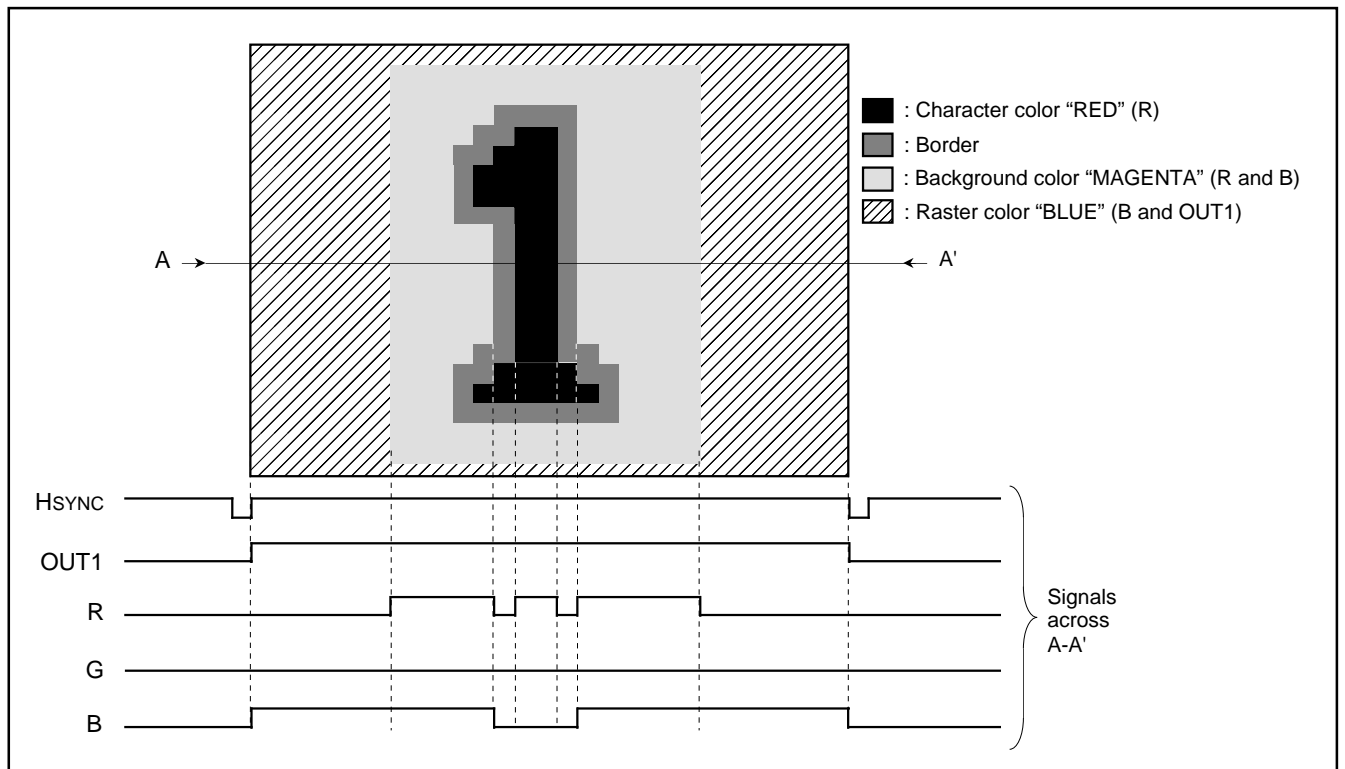
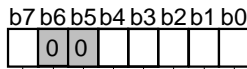


Fig. 81. Example of Raster Coloring

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Raster Color Register



Raster color register (RC) [Address 00D916]

B	Name	Functions	After reset	R;W
0	Raster color R control bit (RC0)	0 : No output 1 : Output	0	R;W
1	Raster color G control bit (RC1)	0 : No output 1 : Output	0	R;W
2	Raster color B control bit (RC2)	0 : No output 1 : Output	0	R;W
3	Raster color OUT1 control bit (RC3)	0 : No output 1 : Output	0	R;W
4	Raster color OUT2 control bit (RC4)	0 : No output 1 : Output	0	R;W
5, 6	Fix these bits to "0."		0	R;W
7	Port function selection bit (RC7)	0 : OSC1/XCIN, OSC2/XCOUT 1 : P26, P27	0	R;W

**Note:** Either OSD clock source or 32 kHz oscillating clock is selected by bits 5 and 6 of the OSD control register.

Fig. 82. Raster Color Register

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**ROM CORRECTION FUNCTION**

This can correct program data in ROM. Up to 2 addresses (2 blocks) can be corrected, a program for correction is stored in the ROM correction memory in RAM. The ROM memory for correction is 32 bytes X 2 blocks.

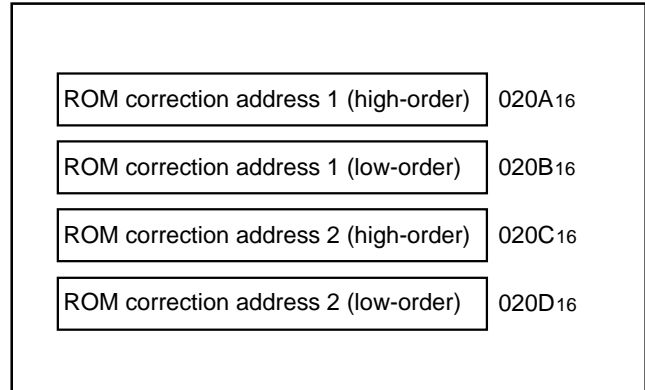
Block 1 : addresses 0300<sub>16</sub> to 031F<sub>16</sub>

Block 2 : addresses 0320<sub>16</sub> to 033F<sub>16</sub>

Set an address of the ROM data to be corrected into the ROM correction address register. When the value of the counter matches the ROM data address in the ROM correction address, the main program branches to the correction program stored in the ROM memory for correction. To return from the correction program to the main program, the op code and operand of the JMP instruction (total of 3 bytes) are necessary at the end of the correction program. When the blocks 1 and 2 are used in series, the above instruction is not needed at the end of the block 1.

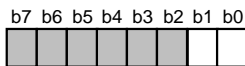
The ROM correction function is controlled by the ROM correction enable register.

- Notes 1** : Specify the first address (op code address) of each instruction as the ROM correction address.
- 2** : Use the JMP instruction (total of 3 bytes) to return from the main program to the correction program.
- 3** : Do not set the same ROM correction address to blocks 1 and 2.



**Fig. 83. ROM Correction Address Registers**

ROM Correction Enable Register



ROM correction enable register (RCR) [Address 020E<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Block 1 enable bit (RC0)	0: Disabled 1: Enabled	0	R	W
1	Block 2 enable bit (RC1)	0: Disabled 1: Enabled	0	R	W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

**Fig. 84. ROM Correction Enable Register**

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**RESET CIRCUIT**

When the oscillation of a quartz-crystal oscillator or a ceramic resonator is stable and the power source voltage is  $5\text{ V} \pm 10\%$ , hold the RESET pin at LOW for  $2\ \mu\text{s}$  or more, then return it to HIGH. Then, as shown in Figure 86, reset is released and the program starts from the address formed by using the content of address  $\text{FFFF}_{16}$  as the high-order address and the content of the address  $\text{FFFE}_{16}$  as the low-order address. The internal state of microcomputer at reset are shown in Figures 5 to 8.

An example of the reset circuit is shown in Figure 85.

The reset input voltage must be kept 0.9 V or less until the power source voltage surpasses 4.5 V.

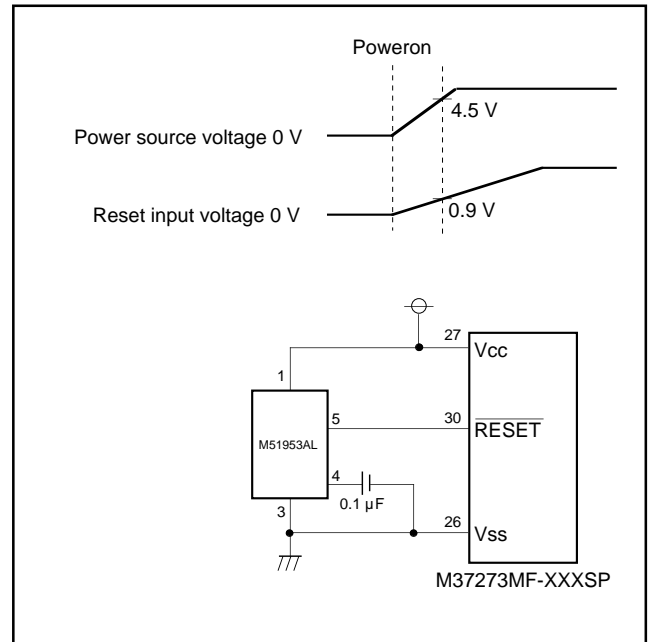


Fig. 85. Example of Reset Circuit

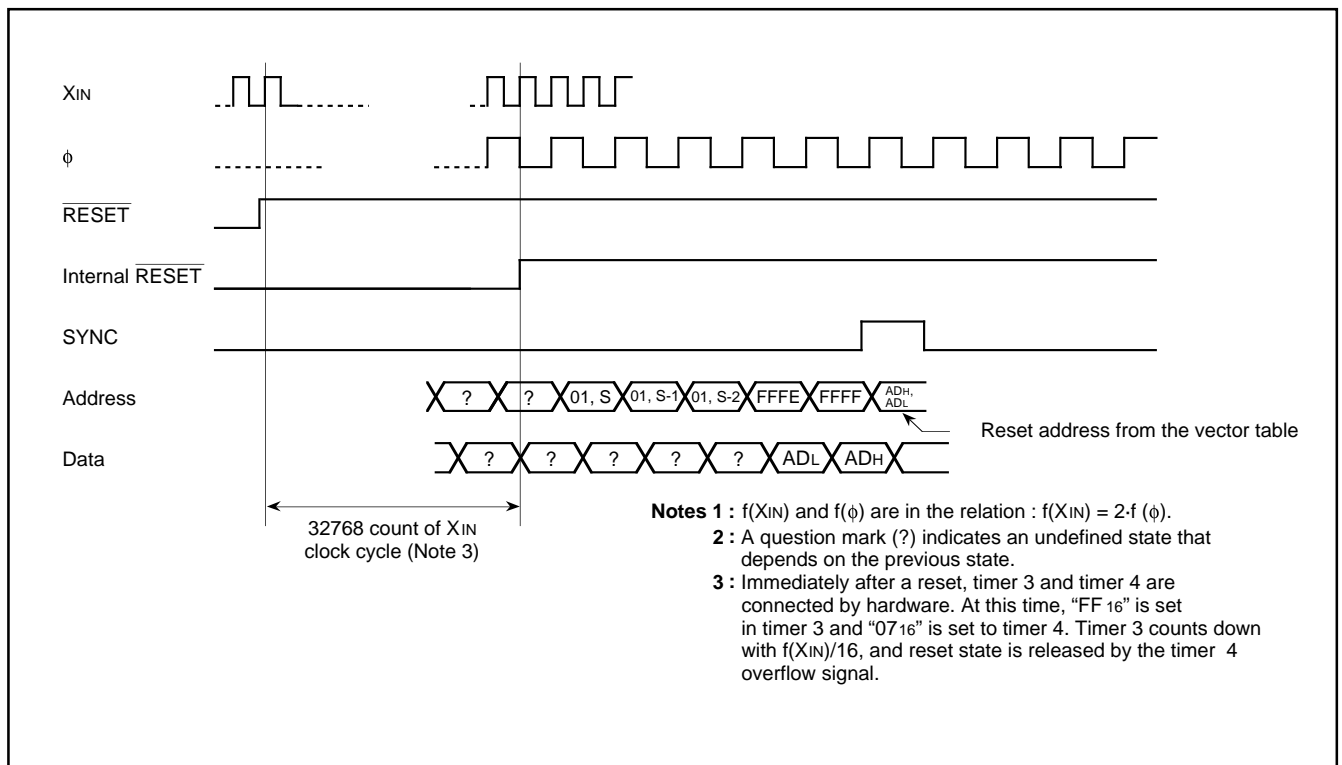


Fig. 86. Reset Sequence



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## CLOCK GENERATING CIRCUIT

The M37273MF-XXXSP has 2 built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOU). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feedback resistor exists on-chip. However, an external feedback resistor is needed between XCIN and XCOU. When using XCIN-XCOU as sub-clock, clear bits 5 and 6 of the OSD control register to "0." To supply a clock signal externally, input it to the XIN (XCIN) pin and make the XOUT (XCOU) pin open. When not using XCIN clock, connect the XCIN to VSS and make the XCOU pin open.

After reset has completed, the internal clock  $\phi$  is half the frequency of XIN. Immediately after poweron, both the XIN and XCIN clock start oscillating. To set the internal clock  $\phi$  to low-speed operation mode, set bit 7 of the CPU mode register (address 00FB16) to "1."

### Oscillation Control (1) Stop mode

The built-in clock generating circuit is shown in Figure 78. When the STP instruction is executed, the internal clock  $\phi$  stops at HIGH. At the same time, timers 3 and 4 are connected by hardware and "FF16" is set in timer 3 and "0716" is set in timer 4. Select  $f(XIN)/16$  or  $f(XCIN)/16$  as the timer 3 count source (set both bit 0 of the timer mode register 2 and bit 6 at address 00C716 to "0" before the execution of the STP instruction). Moreover, set the timer 3 and timer 4 interrupt enable bits to disabled ("0") before execution of the STP instruction. The oscillator restarts when external interrupt is accepted. However, the internal clock  $\phi$  keeps its "H" level until timer 4 overflows, allowing time for oscillation stabilization when a ceramic resonator or a quartz-crystal oscillator is used.

### (2) Wait mode

When the WIT instruction is executed, the internal clock  $\phi$  stops in the "H" level but oscillation continues. This wait state is released at reset or when an interrupt is accepted (Note). Since oscillation does not stop, the next instruction can be executed at once.

**Note:** In the wait mode, the following interrupts are invalid.

- (1) VSYNC interrupt
- (2) OSD interrupt
- (3) Timers 1 and 2 interrupts using TIM2 pin input as count source
- (4) Timer 3 interrupt using TIM3 pin input as count source
- (5) Data slicer interrupt
- (6) Multi-master I<sup>2</sup>C-BUS interface interrupt
- (7)  $f(XIN)/4096$  interrupt
- (8) All timer interrupts using  $f(XIN)/2$  or  $f(XCIN)/2$  as count source
- (9) All timer interrupts using  $f(XIN)/4096$  or  $f(XCIN)/4096$  as count source
- (10) A-D conversion interrupt

### (3) Low-Speed Mode

If the internal clock is generated from the sub-clock (XCIN), a low power consumption operation can be realized by stopping only the main clock XIN. To stop the main clock, set bit 6 (CM6) of the CPU mode register (00FB16) to "1." When the main clock XIN is restarted, the program must allow enough time to for oscillation to stabilize.

Note that in low-power-consumption mode the XCIN-XCOU drivability can be reduced, allowing even lower power consumption. To reduce the XCIN-XCOU drivability, clear bit 5 (CM5) of the CPU mode register (00FB16) to "0." At reset, this bit is set to "1" and strong drivability is selected to help the oscillation to start. When an STP instruction is executed, set this bit to "1" by software before executing.

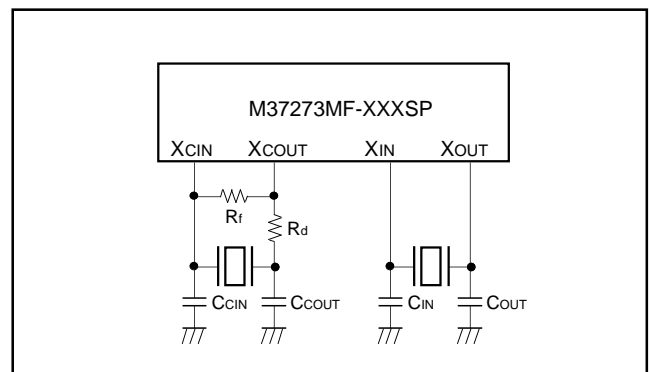


Fig. 77. Ceramic Resonator Circuit Example

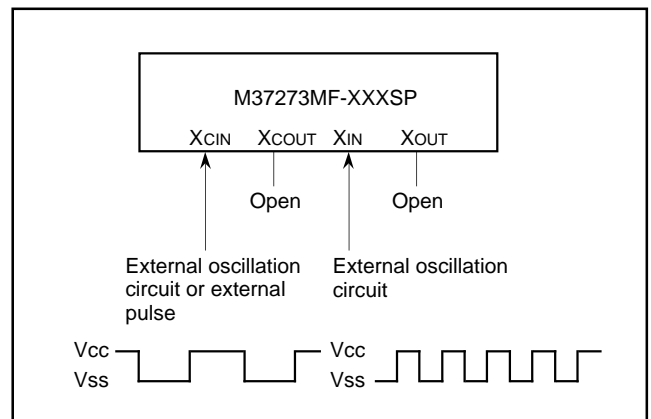
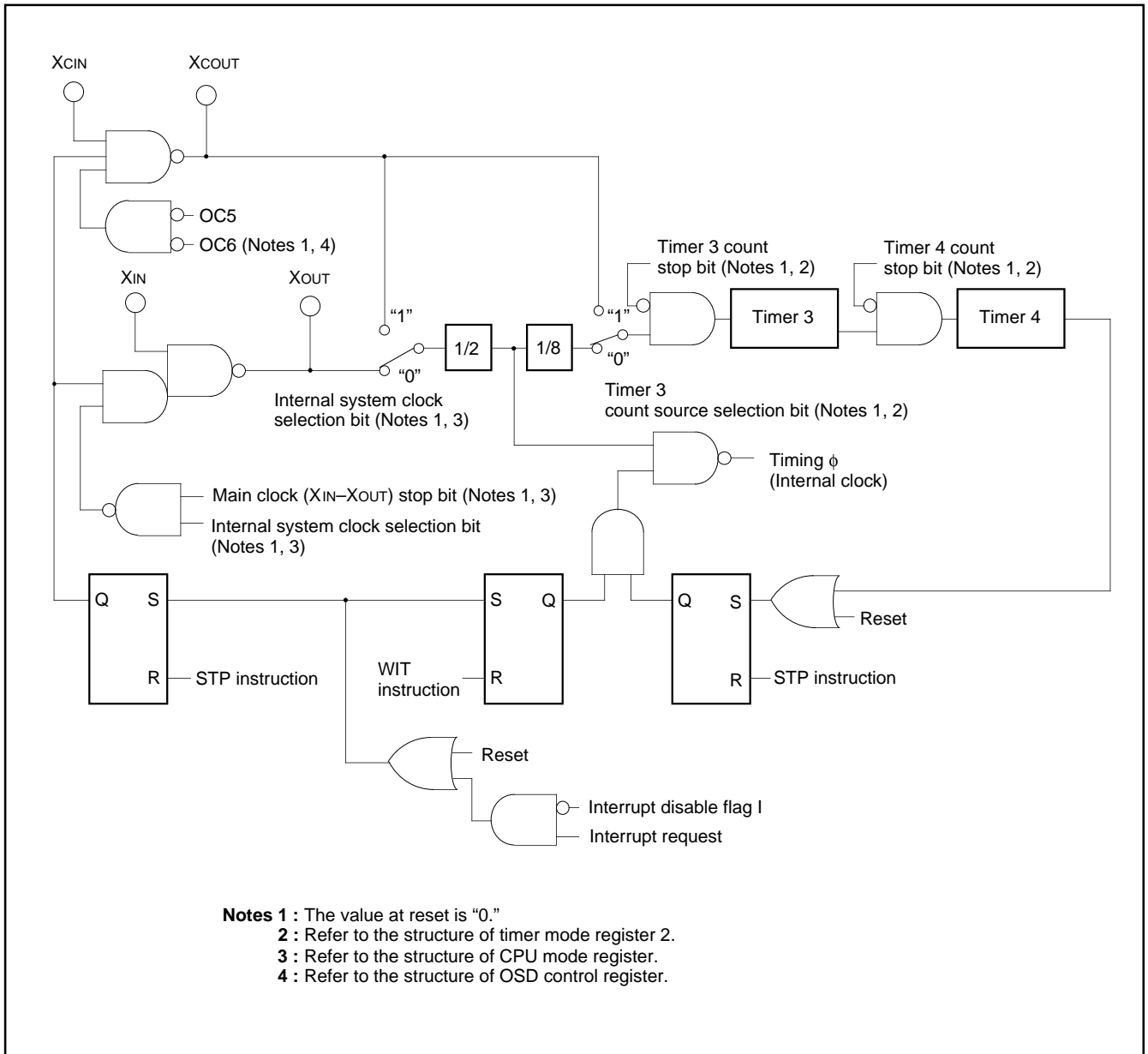


Fig. 78. External Clock Input Circuit Example

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- Notes 1 :** The value at reset is "0."  
**2 :** Refer to the structure of timer mode register 2.  
**3 :** Refer to the structure of CPU mode register.  
**4 :** Refer to the structure of OSD control register.

Fig. 89. Clock Generating Circuit Block Diagram

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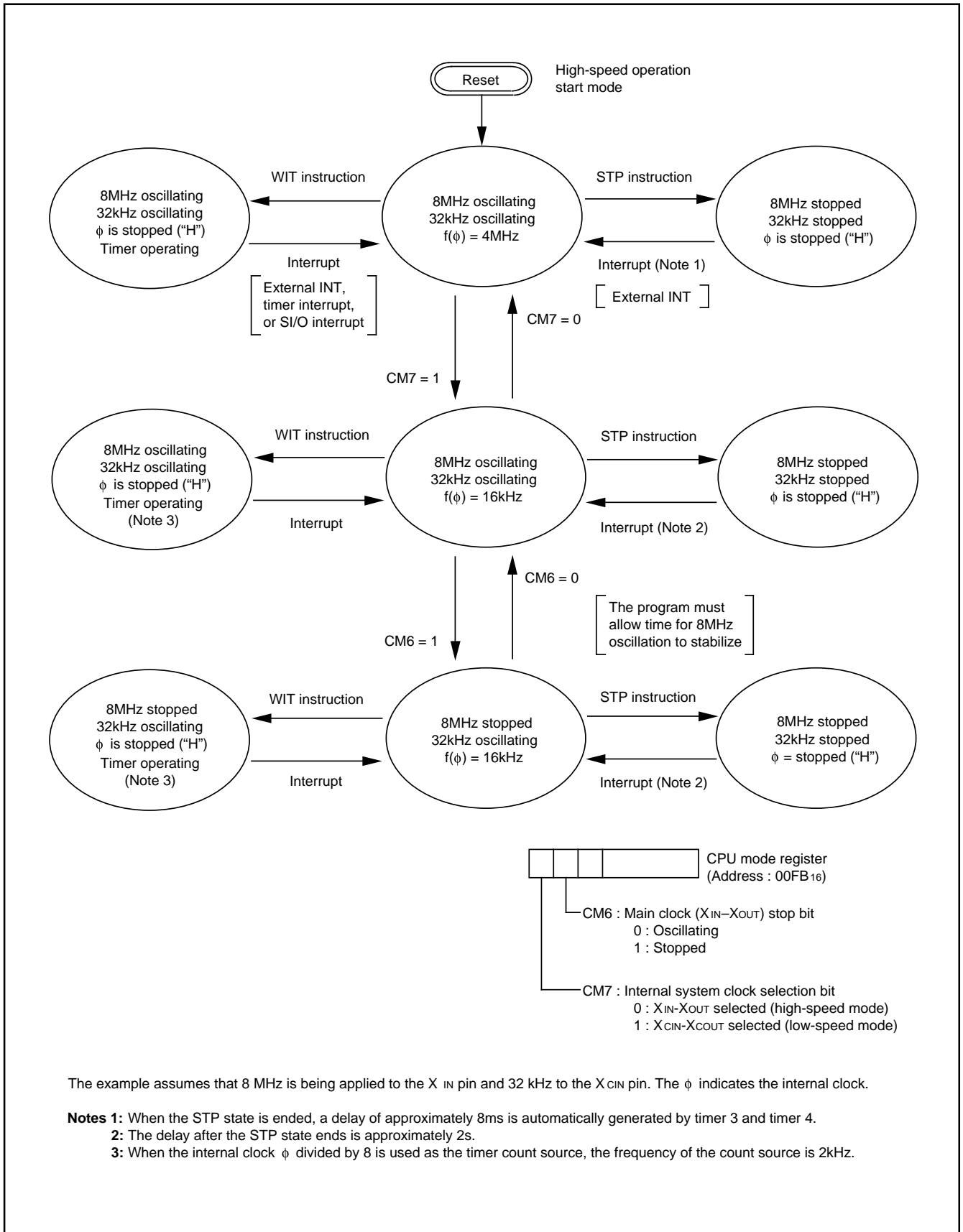


Fig. 90. State Transitions of System Clock

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## DISPLAY OSCILLATION CIRCUIT

The OSD oscillation circuit has a built-in clock oscillation circuits, so that a clock for OSD can be obtained simply by connecting an LC, a ceramic resonator across the pins OSC1 and OSC2. Which of the sub-clock or the OSD oscillation circuit is selected by setting bits 5 and 6 of the OSD control register (address 00D016).

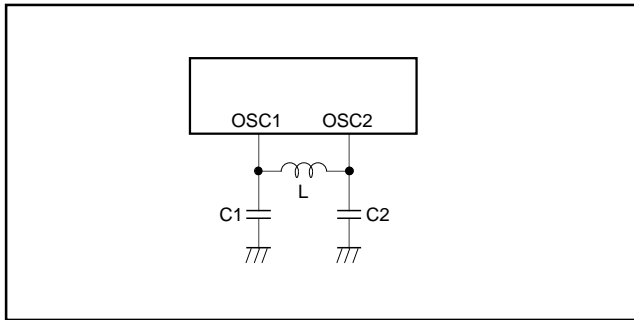


Fig. 91. Display Oscillation Circuit

## AUTO-CLEAR CIRCUIT

When a power source is supplied, the auto-clear function will operate by connecting the following circuit to the RESET pin.

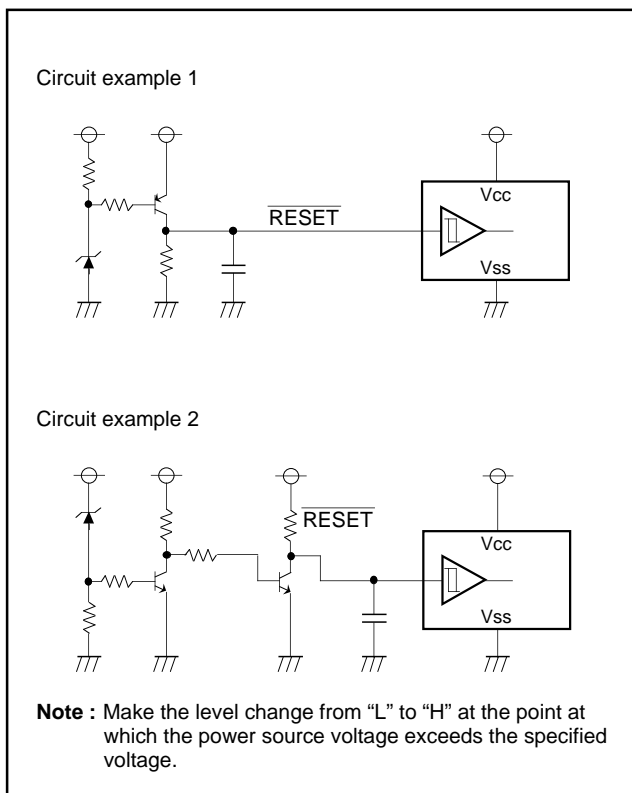


Fig. 92. Auto-clear Circuit Example

## ADDRESSING MODE

The memory access is reinforced with 17 kinds of addressing modes. Refer to SERIES 740 <Software> User's Manual for details.

## MACHINE INSTRUCTIONS

There are 71 machine instructions. Refer to SERIES 740 <Software> User's Manual for details.

## PROGRAMMING NOTES

- (1) The divide ratio of the timer is  $1/(n+1)$ .
- (2) Even though the BBC and BBS instructions are executed immediately after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. At least one instruction cycle is needed (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) After the ADC and SBC instructions are executed (in the decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instruction is executed.
- (4) An NOP instruction is needed immediately after the execution of a PLP instruction.
- (5) In order to avoid noise and latch-up, connect a bypass capacitor ( $\approx 0.1 \mu\text{F}$ ) directly between the VCC pin-VSS pin, AVCC pin-VSS pin, and the VCC pin-CNVSS pin, using a thick wire.

## DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- (1) Mask ROM Order Confirmation Form
- (2) Mask Specification Form
- (3) Data to be written to ROM, in EPROM form (32-pin DIP Type 27C101, three identical copies)

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**PROM Programming Method**

The built-in PROM of the One Time PROM version (blank) and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Product	Name of Programming Adapter
M37273EFSP	PCA7426G02

The PROM of the One Time PROM version (blank) is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 93 is recommended to verify programming.

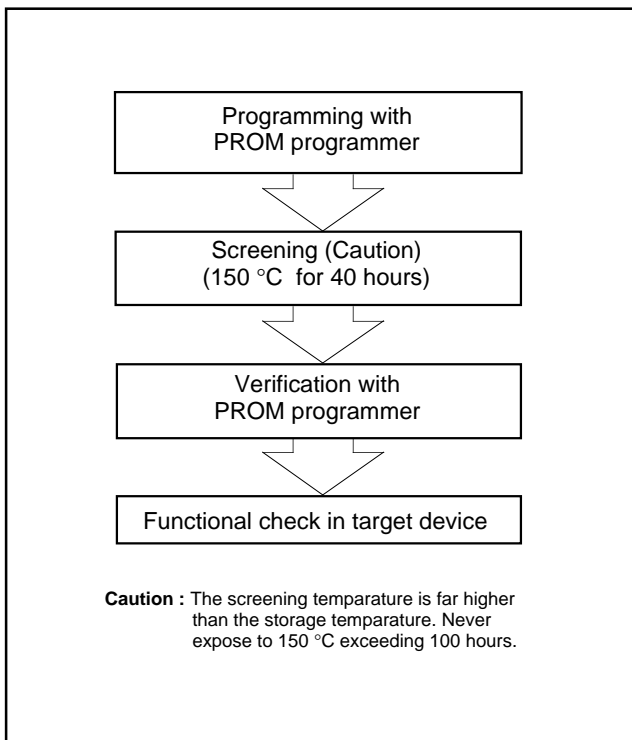


Fig. 93. Programming and testing of One Time PROM version

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**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
VCC, AVCC	Power source voltage VCC, AVCC	All voltages are based on Vss. Output transistors are cut off.	-0.3 to 6	V
Vi	Input voltage CNVss		-0.3 to 6	V
Vi	Input voltage P00-P07, P10-P17, P20-P27, P30, P31, XIN, P50, P51, RESET, CVIN		-0.3 to Vcc + 0.3	V
Vo	Output voltage P06, P07, P10-P17, P20-P27, P30, P31, P52-P57, P60-P67, XOUT		-0.3 to Vcc + 0.3	V
Vo	Output voltage P00-P05		-0.3 to 13	V
IOH	Circuit current P10-P17, P20-P27, P30, P31, P52-P57, P60-P67		0 to 1 (Note 1)	mA
IOL1	Circuit current P06, P07, P10, P15-P17, P20-P23, P26, P27, P52-P57, P60-P67		0 to 2 (Note 2)	mA
IOL2	Circuit current P11-P14		0 to 6 (Note 2)	mA
IOL3	Circuit current P00-P05		0 to 1 (Note 2)	mA
IOL4	Circuit current P24, P25, P30, P31		0 to 10 (Note 3)	mA
Pd	Power dissipation	Ta = 25 °C	550	mW
Topr	Operating temperature		-10 to 70	°C
Tstg	Storage temperature		-40 to 125	°C

**RECOMMENDED OPERATING CONDITIONS** (Ta = -10 °C to 70 °C, Vcc = 5 V ± 10 %, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
VCC, AVCC	Power source voltage (Note 4), During CPU, OSD, data slicer operation	4.5	5.0	5.5	V
VSS	Power source voltage	0	0	0	V
VIH1	HIGH input voltage P00-P07, P10-P17, P20-P27, P30, P31, P50, P51, Hsync, Vsync, RESET, XIN	0.8VCC		Vcc	V
VIH2	HIGH input voltage SCL1, SCL2, SDA1, SDA2 (When using I <sup>2</sup> C-BUS)	0.7Vcc		Vcc	V
VIL1	LOW input voltage P00-P07, P10-P17, P20-P27, P30, P31	0		0.4 Vcc	V
VIL2	LOW input voltage SCL1, SCL2, SDA1, SDA2, (When using I <sup>2</sup> C-BUS)	0		0.3 Vcc	V
VIL3	LOW input voltage (Note 6) P50, P51, RESET, XIN, OSC1, TIM2, TIM3, INT1, INT2, INT3, SIN, SCLK	0		0.2 Vcc	V
IOH	HIGH average output current (Note 1) P10-P17, P20-P27, P30, P31, P52-P57, P60-P67			1	mA
IOL1	LOW average output current (Note 2) P06, P07, P10, P15-P17, P20-P23, P26, P27, P52-P57, P60-P67			2	mA
IOL2	LOW average output current (Note 2) P11-P14			6	mA
IOL3	LOW average output current (Note 2) P00-P05			1	mA
IOL4	LOW average output current (Note 3) P24, P25, P30, P31			10	mA
f(XIN)	Oscillation frequency (for CPU operation) (Note 5) XIN	7.9	8.0	8.1	MHz
f(XCIN)	Oscillation frequency (for sub-clock operation) XCIN	29	32	35	kHz
fOSC	Oscillation frequency (for OSD) OSC1	26.5	27.0	27.0	MHz
fhs1	Input frequency TIM2, TIM3, INT1, INT2, INT3			100	kHz
fhs2	Input frequency SCLK			1	MHz
fhs3	Input frequency SCL1, SCL2			400	kHz
fhs4	Input frequency Horizontal sync. signal of video signal	15.262	15.734	16.206	kHz
Vi	Input amplitude video signal CVIN	1.5	2.0	2.5	V

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**ELECTRIC CHARACTERISTICS** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $f(X_{IN}) = 8\text{ MHz}$ ,  $T_a = -10\text{ }^\circ\text{C}$  to  $70\text{ }^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
I <sub>CC</sub>	Power source current	System operation	V <sub>CC</sub> = 5.5 V, f(X <sub>IN</sub> ) = 8 MHz	OSD OFF Data slicer OFF		15	30	mA
				OSD ON Data slicer ON		30	45	
			V <sub>CC</sub> = 5.5 V, f(X <sub>IN</sub> ) = 0, f(X <sub>CIN</sub> ) = 32kHz, OSD OFF, Data slicer OFF, Low-power dissipation mode set (CM <sub>5</sub> = "0", CM <sub>6</sub> = "1")			60	200	μA
		Wait mode	V <sub>CC</sub> = 5.5 V, f(X <sub>IN</sub> ) = 8 MHz			2	4	mA
			V <sub>CC</sub> = 5.5 V, f(X <sub>IN</sub> ) = 0, f(X <sub>CIN</sub> ) = 32kHz, Low-power dissipation mode set (CM <sub>5</sub> = "0", CM <sub>6</sub> = "1")			25	100	
Stop mode	V <sub>CC</sub> = 5.5 V, f(X <sub>IN</sub> ) = 0, f(X <sub>CIN</sub> ) = 0			1	10			
V <sub>OH</sub>	HIGH output voltage	P10–P17, P20–P27, P30, P31, P52–P57, P60–P67	V <sub>CC</sub> = 4.5 V I <sub>OH</sub> = –0.5 mA		2.4			V
V <sub>OL</sub>	LOW output voltage	P00–P07, P10, P15– P17, P20–P23, P26, P27, P52–P57, P60–P67	V <sub>CC</sub> = 4.5 V I <sub>OL</sub> = 0.5 mA				0.4	V
	LOW output voltage	P24, P25, P30, P31	V <sub>CC</sub> = 4.5 V I <sub>OL</sub> = 10.0 mA				3.0	
	LOW output voltage	P11–P14	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 3 mA I <sub>OL</sub> = 6 mA			0.4 0.6	
V <sub>T+</sub> –V <sub>T–</sub>	Hysteresis (Note 6)	P50, P51, INT1, INT2, INT3, TIM2, TIM3, S <sub>IN</sub> , S <sub>CLK</sub> , S <sub>CL1</sub> , S <sub>CL2</sub> , S <sub>DA1</sub> , S <sub>DA2</sub> , RESET	V <sub>CC</sub> = 5.0 V			0.5	1.3	V
I <sub>IZH</sub>	HIGH input leak current	P06, P07, P10–P17, P50, P51, P20–P27, P30, P31, RESET	V <sub>CC</sub> = 5.5 V V <sub>I</sub> = 5.5 V				5	μA
	HIGH input leak current	P00–P05	V <sub>CC</sub> = 5.5 V V <sub>I</sub> = 12 V				10	
I <sub>IZL</sub>	LOW input leak current	P00–P07, P10–P17, P20–P27, P30, P31, P50, P51, RESET	V <sub>CC</sub> = 5.5 V V <sub>I</sub> = 0 V				5	μA
R <sub>BS</sub>	I <sup>2</sup> C-BUS-BUS switch connection resistor (between S <sub>CL1</sub> and S <sub>CL2</sub> , S <sub>DA1</sub> and S <sub>DA2</sub> )		V <sub>CC</sub> = 4.5 V				130	Ω

**Notes 1:** The total current that flows out of the IC must be 20 mA or less.

**2:** The total input current to IC (I<sub>OL1</sub> + I<sub>OL2</sub> + I<sub>OL3</sub>) must be 30 mA or less.

**3:** The total average input current for ports P30, P31, P24, P25 to IC must be 20 mA or less.

**4:** Connect 0.1 μF or more capacitor externally between the power source pins V<sub>CC</sub>–V<sub>SS</sub> and AV<sub>CC</sub>–V<sub>SS</sub> so as to reduce power source noise.

Also connect 0.1 μF or more capacitor externally between the pins V<sub>CC</sub>–CNV<sub>SS</sub>.

**5:** Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit.

**6:** P06, P07, P15, P23, P24 have the hysteresis when these pins are used as interrupt input pins or timer input pins. P11–P14 have the hysteresis when these pins are used as multi-master I<sup>2</sup>C-BUS interface ports. P20, P22 have the hysteresis when these pins are used as serial I/O pins.

**7:** Pin names in each parameter is described as below.

(1) Dedicated pins: dedicated pin names.

(2) Duple-/triple-function ports

- When the same limits: I/O port name.

- When the limits of functions except ports are different from I/O port limits: function pin name.

**M37273MF-XXXSP**  
**M37273EFSP**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
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**A-D COMPARATOR CHARACTERISTICS**

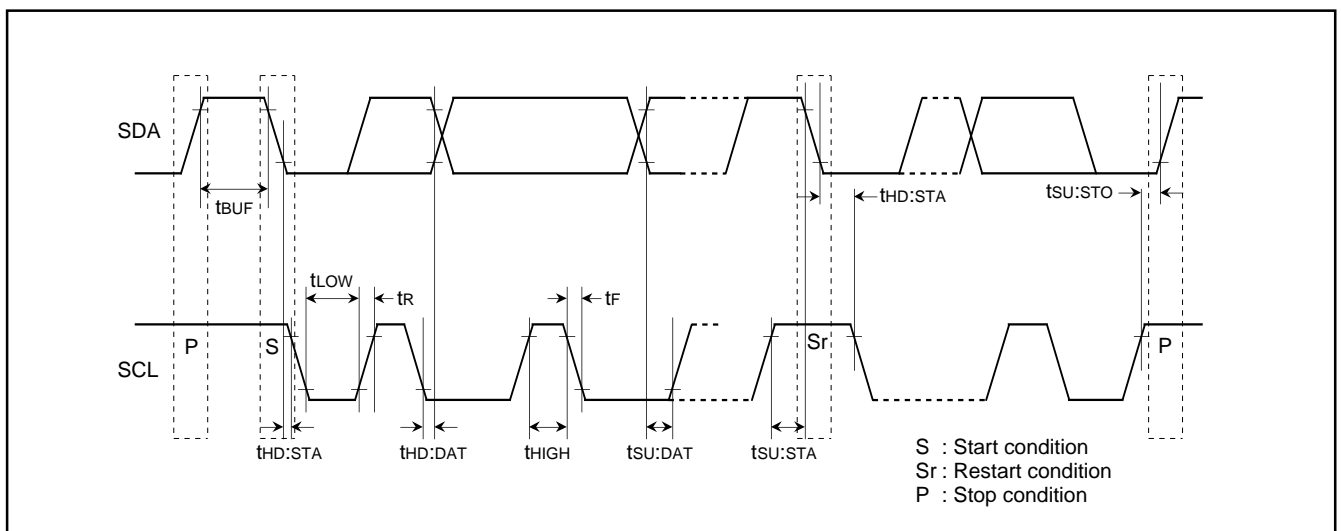
(V<sub>CC</sub> = 5 V ± 10 %, V<sub>SS</sub> = 0 V, f(X<sub>IN</sub>) = 8 MHz, T<sub>a</sub> = -10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				6	bits
—	Non-linearity error		0		±1	LSB
—	Differential non-linearity error		0		±0.9	LSB
VOT	Zero transition error	I <sub>OL</sub> (SUM) = 0mA	0		2	LSB
VFST	Full-scale transition error		0		-2	LSB

**MULTI-MASTER I<sup>2</sup>C-BUS BUS LINE CHARACTERISTICS**

Symbol	Parameter	Standard Clock Mode		High-speed Clock Mode		Unit
		Min.	Max.	Min.	Max.	
t <sub>BUF</sub>	Bus free time	4.7		1.3		μs
t <sub>HD:STA</sub>	Hold time for START condition	4.0		0.6		μs
t <sub>LOW</sub>	LOW period of SCL clock	4.7		1.3		μs
t <sub>R</sub>	Rising time of both SCL and SDA signals		1000	20+0.1C <sub>b</sub>	300	ns
t <sub>HD:DAT</sub>	Data hold time	0		0	0.9	μs
t <sub>HIGH</sub>	HIGH period of SCL clock	4.0		0.6		μs
t <sub>F</sub>	Falling time of both SCL and SDA signals		300	20+0.1C <sub>b</sub>	300	ns
t <sub>SU:DAT</sub>	Data set-up time	250		100		ns
t <sub>SU:STA</sub>	Set-up time for repeated START condition	4.7		0.6		μs
t <sub>SU:STO</sub>	Set-up time for STOP condition	4.0		0.6		μs

**Note:** C<sub>b</sub> = total capacitance of 1 bus line



**Fig. 94. Definition Diagram of Timing on Multi-master I<sup>2</sup>C-BUS**



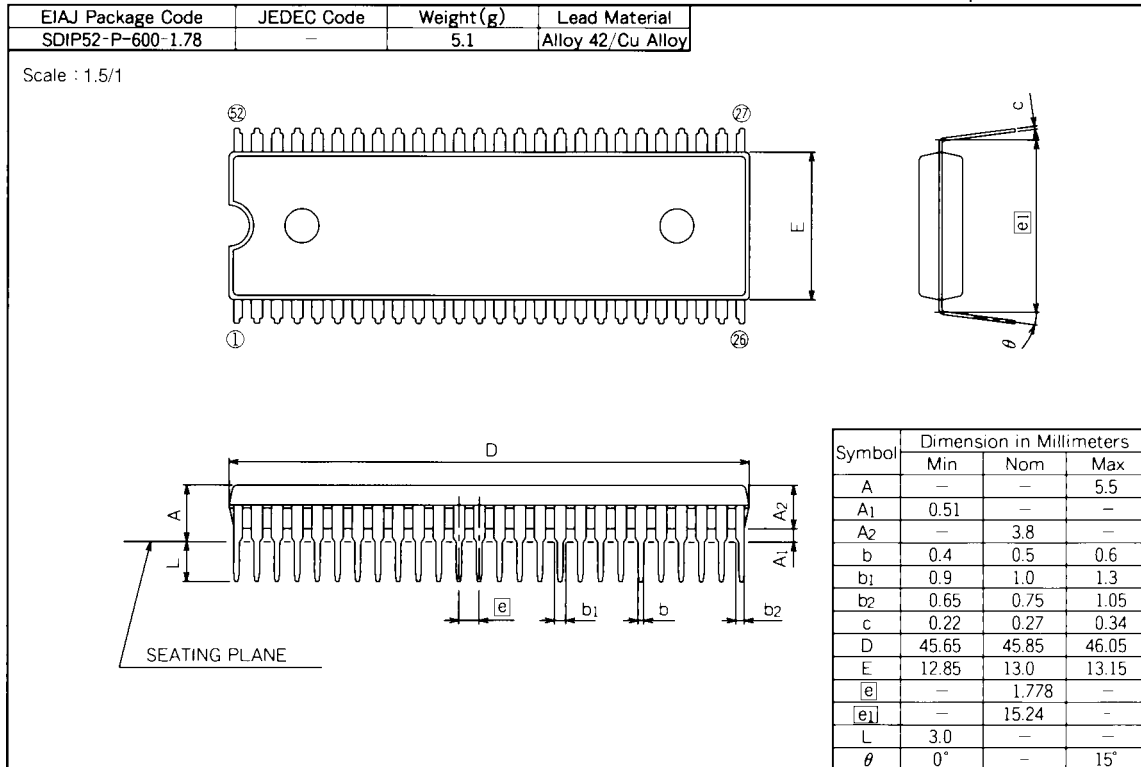
**M37273MF-XXXSP**  
**M37273EFSP**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
and ON-SCREEN DISPLAY CONTROLLER

**PACKAGE OUTLINE**

**52P4B**

Plastic 52pin 600mil SDIP



**M37273MF-XXXSP**  
**M37273EFSP**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
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GZZ-SH11-94B < 76A0 >

**740 FAMILY MASK ROM CONFIRMATION FORM**  
**SINGLE-CHIP MICROCOMPUTER M37273MF-XXXSP**  
**MITSUBISHI ELECTRIC**

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked \* .

* Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

\* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three EPROMs are required for each pattern.

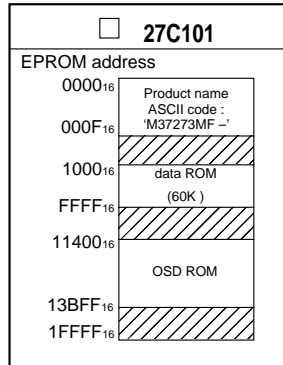
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM 

--	--	--	--

 (hexadecimal notation)

EPROM type (indicate the type used)



- (1) Set "FF<sub>16</sub>" in the shaded area and in the test data storing area for OSD ROM (refer to page 3/3). Moreover, set "00<sub>16</sub>" in the "transparent space" font data storing area. If writing data by mistake, a hindrance for ship may occur. Therefore, extreme care must be taken to verify that the specified data is stored in the corresponding area in the submitted EPROMs.
- (2) Write the ASCII codes that indicate the product name of "M37273MF-" to addresses 0000<sub>16</sub> to 000F<sub>16</sub>.

EPROM data check item (Confirm the EPROM data and check "✓" the appropriate box)

- Is "FF<sub>16</sub>" set in the shaded area and in the test data storing area for OSD ROM (refer to page 3/3)? → Yes
- Is "00<sub>16</sub>" set in the "transparent space" font data storing area (refer to page 3/3)? → Yes
- Are the ASCII codes that indicates the product name of "M37273MF-" to addresses 0000<sub>16</sub> to 000F<sub>16</sub>? → Yes

\* 2. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered. Fill the appropriate mark specification form (52P4B for M37273MF-XXXSP) and attach to the mask ROM confirmation form.

**M37273MF-XXXSP**  
**M37273EFSP**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
and ON-SCREEN DISPLAY CONTROLLER

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**740 FAMILY MASK ROM CONFIRMATION FORM**  
**SINGLE-CHIP MICROCOMPUTER M37273MF-XXXSP**  
**MITSUBISHI ELECTRIC**

**How to Write the Product Name and Character ROM Data onto EPROMs**

Addresses 0000<sub>16</sub> to 000F<sub>16</sub> store the product name, and addresses 11400<sub>16</sub> to 13BFF<sub>16</sub> store the character pattern. Both address and data are described in hexadecimal notation.

If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Please make sure the data is written correctly.

1. How to input the name of the product with the ASCII code: ASCII codes 'M37273MF-' are listed on the right. The addresses and data are in hexadecimal notation.	Address		Address
	0000 <sub>16</sub>	'M' = 4 D <sub>16</sub>	0008 <sub>16</sub>
	0001 <sub>16</sub>	'3' = 3 3 <sub>16</sub>	0009 <sub>16</sub>
	0002 <sub>16</sub>	'7' = 3 7 <sub>16</sub>	000A <sub>16</sub>
	0003 <sub>16</sub>	'2' = 3 2 <sub>16</sub>	000B <sub>16</sub>
	0004 <sub>16</sub>	'7' = 3 7 <sub>16</sub>	000C <sub>16</sub>
	0005 <sub>16</sub>	'3' = 3 3 <sub>16</sub>	000D <sub>16</sub>
	0006 <sub>16</sub>	'M' = 4 D <sub>16</sub>	000E <sub>16</sub>
0007 <sub>16</sub>	'F' = 4 6 <sub>16</sub>	000F <sub>16</sub>	

2. Inputting the character ROM

Input the character ROM data to character ROM. For the character ROM data, see the next page and on.

**M37273MF-XXXSP**  
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GZZ-SH11-94B < 76A0 >


**740 FAMILY MASK ROM CONFIRMATION FORM**  
**SINGLE-CHIP MICROCOMPUTER M37273MF-XXXSP**  
**MITSUBISHI ELECTRIC**

Font data must be stored in the proper OSD ROM address according to the following table.

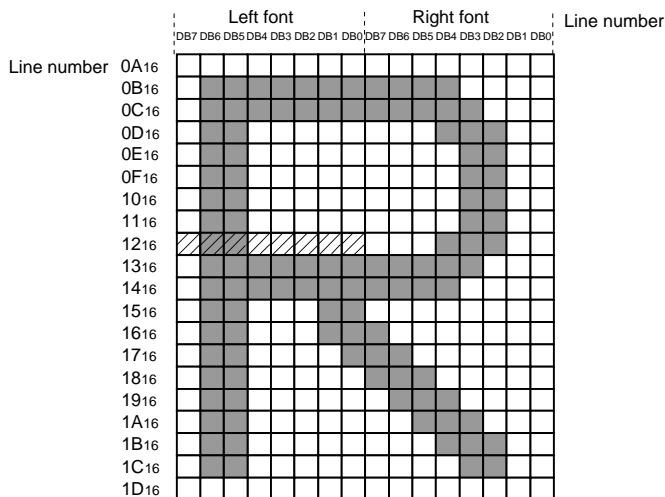
(1) OSD ROM address of character font data

OSD ROM address bit	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Line number / Character code / Font bit	1	0	0	Line number					Character code								Font bit

Line number = 0A<sub>16</sub> to 1D<sub>16</sub>  
 Character code = 00<sub>16</sub> to FF<sub>16</sub> (Do not set 7F<sub>16</sub> to 80<sub>16</sub>.)  
 Font bit = 0 : Left font  
           1 : Right font

Example ) The font data "60" (shaded area ) of the character code "AA<sub>16</sub>" is stored in address

$$1\ 0\ 0\ 1\ 0\ 0\ 1\ 0\ 1\ 0\ 1\ 0\ 1\ 0\ 1\ 0\ 1\ 0\ 1\ 0\ 0\ 1\ 0\ 0\ 2 = 12554_{16}$$



(1) Character code "AA<sub>16</sub>"

**Notes 1 :** The 80-byte addresses corresponding to the character code "7F<sub>16</sub>" and "80<sub>16</sub>" in OSD ROM are the test data storing area. Set "FF<sub>16</sub>" to the area (We stores the test data to this area and the different data from "FF<sub>16</sub>" is stored for the actual products.)  
 The test data storing area :  
 addresses 11000<sub>16</sub> + (4 + 2n) × 100<sub>16</sub> + FE<sub>16</sub> to 11000<sub>16</sub> + (5 + 2n) × 100<sub>16</sub> + 01<sub>16</sub>  
 (n = 0 to 19)

addresses 114FE <sub>16</sub> to 11501 <sub>16</sub>
addresses 116FE <sub>16</sub> to 11701 <sub>16</sub>
⋮
addresses 138FE <sub>16</sub> to 13901 <sub>16</sub>
addresses 13AFE <sub>16</sub> to 13B01 <sub>16</sub>

**2 :** The character code "09<sub>16</sub>" is used for "transparent space" when displaying Closed Caption. Therefore, set "00<sub>16</sub>" to the 40-byte addresses corresponding to the character code "09<sub>16</sub>."  
 The transparent space font data storing area :  
 addresses 11000<sub>16</sub> + (4 + 2n) × 100<sub>16</sub> + 12<sub>16</sub> to 11000<sub>16</sub> + (4 + 2n) × 100<sub>16</sub> + 13<sub>16</sub>  
 (n = 0 to 19)

addresses 11412 <sub>16</sub> and 11413 <sub>16</sub>
addresses 11612 <sub>16</sub> and 11613 <sub>16</sub>
⋮
addresses 13812 <sub>16</sub> and 13813 <sub>16</sub>
addresses 13A12 <sub>16</sub> and 13A13 <sub>16</sub>

**M37273MF-XXXSP**  
**M37273EFSP**

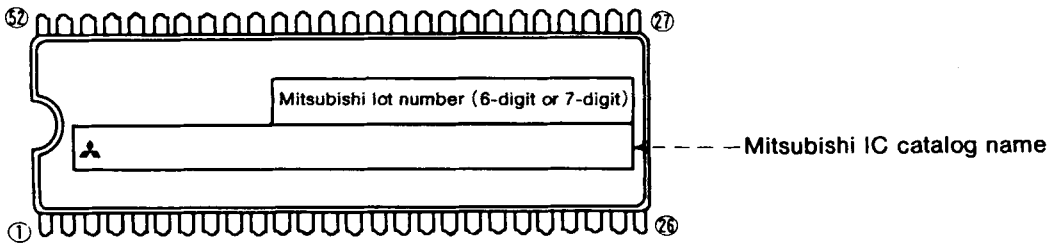
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
and ON-SCREEN DISPLAY CONTROLLER

**52P4B (52-PIN SHRINK DIP) MARK SPECIFICATION FORM**

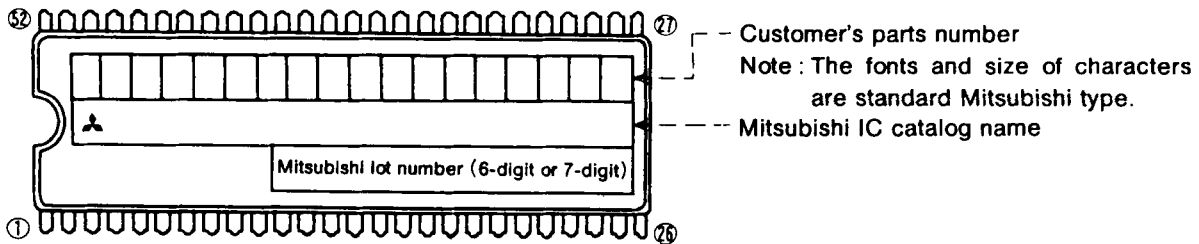
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

**A. Standard Mitsubishi Mark**



**B. Customer's Parts Number + Mitsubishi Catalog Name**



Note1: The mark field should be written right aligned.

2: The fonts and size of characters are standard Mitsubishi type.

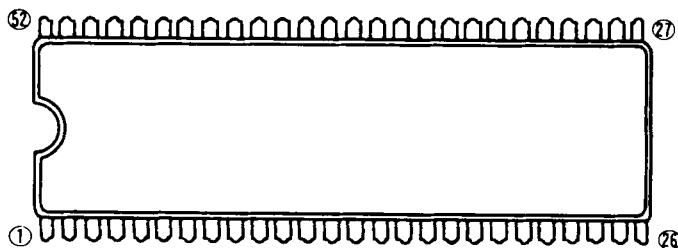
3: Customer's parts number can be up to 18 characters:

Only 0~9, A~Z, +, -, /, (, ), &, ©, . (period), and , (comma) are usable.

4: If the Mitsubishi logo is not required, check the box on the right.

Mitsubishi logo is not required

**C. Special Mark Required**



Note1: If the special mark is to be printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

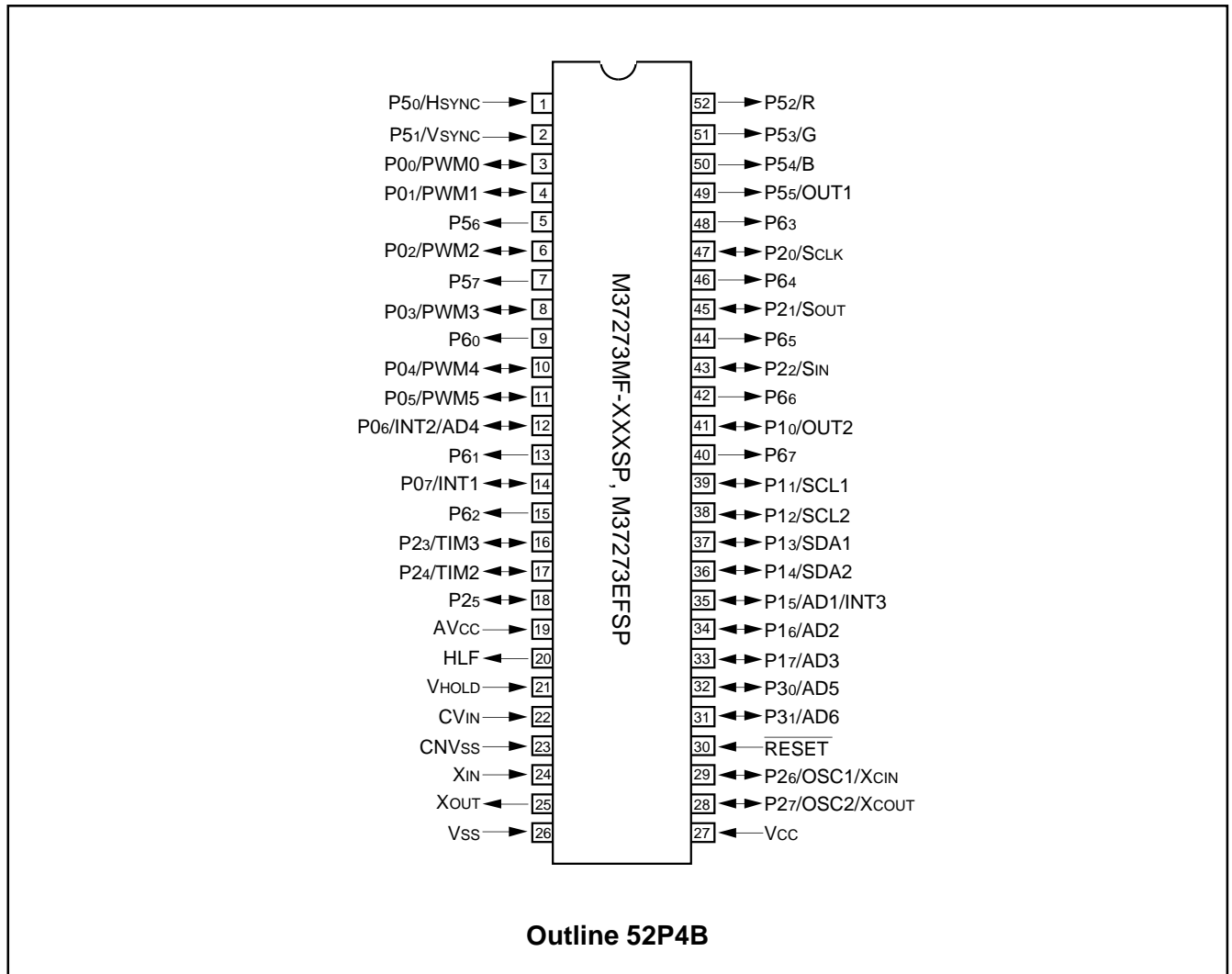
The standard Mitsubishi font is used for all characters except for a logo.

**M37273MF-XXXSP**  
**M37273EFSP**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
and ON-SCREEN DISPLAY CONTROLLER

<APPENDIX>

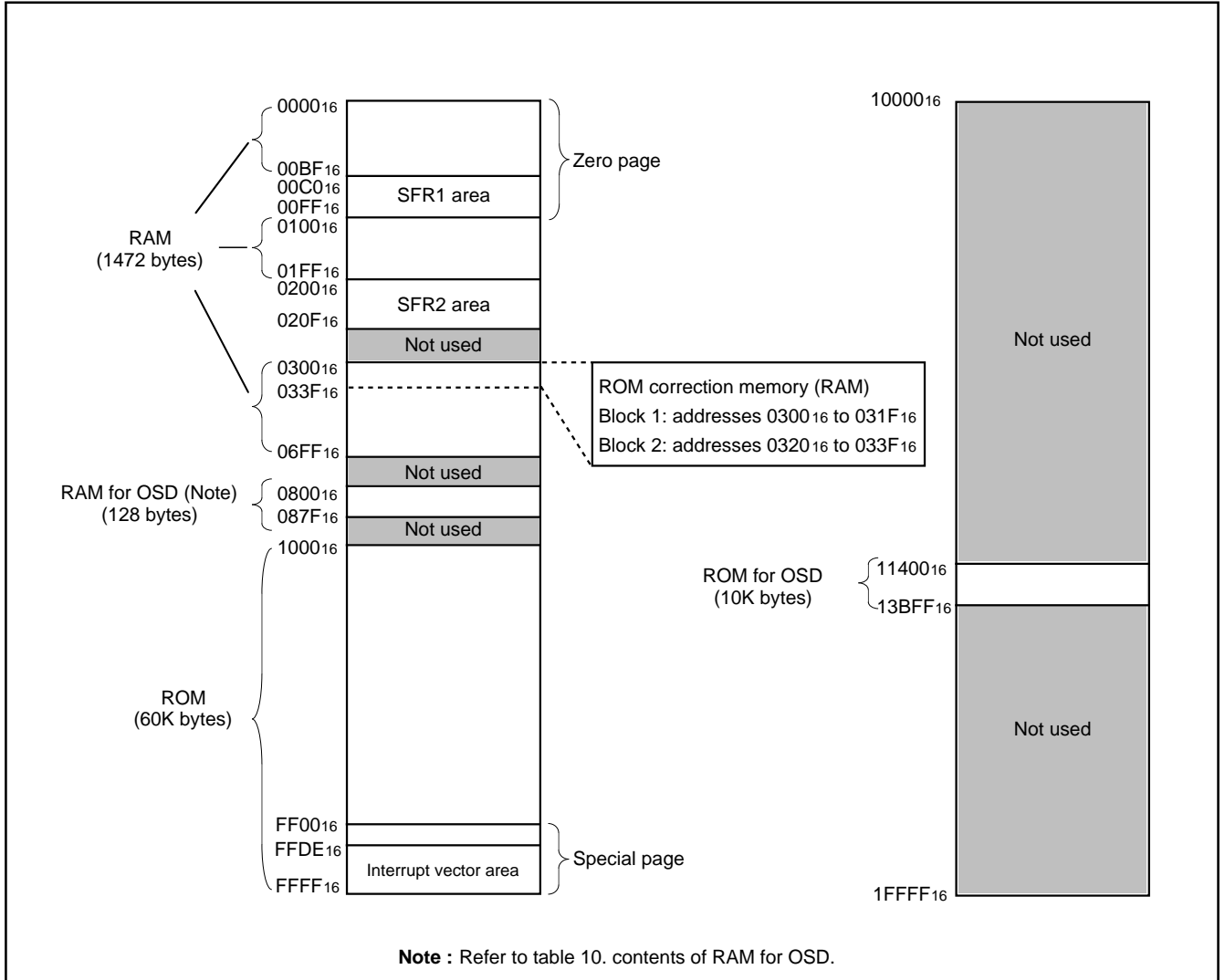
Pin Configuration (top view)



**M37273MF-XXXSP**  
**M37273EFSP**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
and ON-SCREEN DISPLAY CONTROLLER

**Memory Map**



**M37273MF-XXXSP**  
**M37273EFSP**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

**Memory Map of Special Function Register (SFR)**

■ SFR1 Area (addresses C0<sub>16</sub> to DF<sub>16</sub>)

<Bit allocation>

- : } Function bit
- Name : }
- : No function bit
- 0 : Fix this bit to "0" (do not write "1")
- 1 : Fix this bit to "1" (do not write "0")

<State immediately after reset>

- 0 : "0" immediately after reset
- 1 : "1" immediately after reset
- ? : Undefined immediately after reset

Address	Register	Bit allocation								State immediately after reset							
		b7							b0	b7							b0
C0 <sub>16</sub>	Port P0 (P0)																?
C1 <sub>16</sub>	Port P0 direction register (D0)																00 <sub>16</sub>
C2 <sub>16</sub>	Port P1 (P1)																?
C3 <sub>16</sub>	Port P1 direction register (D1)																00 <sub>16</sub>
C4 <sub>16</sub>	Port P2 (P2)																?
C5 <sub>16</sub>	Port P2 direction register (D2)																00 <sub>16</sub>
C6 <sub>16</sub>	Port P3 (P3)								P31 P30	0	0	0	0	0	0	?	?
C7 <sub>16</sub>	Port P3 direction register (D3)		T3SC					P31C P30C	P31D P30D								00 <sub>16</sub>
C8 <sub>16</sub>																	?
C9 <sub>16</sub>																	?
CA <sub>16</sub>	Port P5 (P5)																?
CB <sub>16</sub>	OSD port control register (PF)		PF7		PF5	PF4	PF3	PF2	0 0								00 <sub>16</sub>
CC <sub>16</sub>	Port P6 (P6)																00 <sub>16</sub>
CD <sub>16</sub>																	?
CE <sub>16</sub>	Caption data register 3 (CD3)		CDL27	CDL26	CDL25	CDL24	CDL23	CDL22	CDL21	CDL20							?
CF <sub>16</sub>	Caption data register 4 (CD4)		CDH27	CDH26	CDH25	CDH24	CDH23	CDH22	CDH21	CDH20							?
D0 <sub>16</sub>	OSD control register (OC)		0	OC6	OC5	OC4	OC3	OC2	OC1	OC0							00 <sub>16</sub>
D1 <sub>16</sub>	Horizontal position register (HP)			HP6	HP5	HP4	HP3	HP2	HP1	HP0							00 <sub>16</sub>
D2 <sub>16</sub>	Block control register 1 (BC1)		BC17	BC16	BC15	BC14	BC13	BC12	BC11	BC10							?
D3 <sub>16</sub>	Block control register 2 (BC2)		BC27	BC26	BC25	BC24	BC23	BC22	BC21	BC20							?
D4 <sub>16</sub>	Vertical position register 1 (VP1)		VP17	VP16	VP15	VP14	VP13	VP12	VP11	VP10							?
D5 <sub>16</sub>	Vertical position register 2 (VP2)		VP27	VP26	VP25	VP24	VP23	VP22	VP21	VP20							?
D6 <sub>16</sub>	Window register 1 (WN1)		WN17	WN16	WN15	WN14	WN13	WN12	WN11	WN10							?
D7 <sub>16</sub>	Window register 2 (WN2)		WN27	WN26	WN25	WN24	WN23	WN22	WN21	WN20							?
D8 <sub>16</sub>	I/O polarity control register (PC)		0	PC6	PC5	PC4	PC3	PC2	PC1	PC0							40 <sub>16</sub>
D9 <sub>16</sub>	Raster color register (RC)		RC7	0	0	RC4	RC3	RC2	RC1	RC0							00 <sub>16</sub>
DA <sub>16</sub>																	?
DB <sub>16</sub>																	?
DC <sub>16</sub>	Interrupt input polarity control register (RE)							INT3	INT2	INT1							00 <sub>16</sub>
DD <sub>16</sub>																	00 <sub>16</sub>
DE <sub>16</sub>																	00 <sub>16</sub>
DF <sub>16</sub>																	00 <sub>16</sub>



**M37273MF-XXXSP**  
**M37273EFSP**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

■ SFR1 Area (addresses E0<sub>16</sub> to FF<sub>16</sub>)

<Bit allocation >



□ : No function bit

0 : Fix this bit to "0" (do not write "1")

1 : Fix this bit to "1" (do not write "0")

<State immediately after reset >

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Undefined immediately after reset

Address	Register	Bit allocation								State immediately after reset								
		b7						b0		b7						b0		
E0 <sub>16</sub>	Data slicer control register 1 (DSC1)	0	1	1	0	0	DSC12	DSC11	DSC10	00 <sub>16</sub>								
E1 <sub>16</sub>	Data slicer control register 2 (DSC2)		0		DSC25	DSC24	DSC23		1	DSC20	? 0 ? 0 ? ? 0 ?							
E2 <sub>16</sub>	Caption data register 1 (CD1)	CDL17	CDL16	CDL15	CDL14	CDL13	CDL12	CDL11	CDL10	00 <sub>16</sub>								
E3 <sub>16</sub>	Caption data register 2 (CD2)	CDH17	CDH16	CDH15	CDH14	CDH13	CDH12	CDH11	CDH10	00 <sub>16</sub>								
E4 <sub>16</sub>	Clock run-in detect register (CRD)	CRD7	CRD6	CRD5	CRD4	CRD3				00 <sub>16</sub>								
E5 <sub>16</sub>	Data clock position register (DPS)	DPS7	DPS6	DPS5	DPS4	DPS3	0	1	0	0 0 0 0 1 0 0 1								
E6 <sub>16</sub>	Caption position register (CPS)	CPS7	CPS6	CPS5	CPS4	CPS3	CPS2	CPS1	CPS0	0 0 ? 0 0 0 0 0								
E7 <sub>16</sub>	Data slicer test register 2									00 <sub>16</sub>								
E8 <sub>16</sub>	Data slicer test register 1									00 <sub>16</sub>								
E9 <sub>16</sub>	Synchronous signal counter register (HC)			HC5	HC4	HC3	HC2	HC1	HC0	00 <sub>16</sub>								
EA <sub>16</sub>	Serial I/O register (SIO)									?								
EB <sub>16</sub>	Serial I/O mode register (SM)	0	SM6	SM5	0	SM3	SM2	SM1	SM0	00 <sub>16</sub>								
EC <sub>16</sub>	A-D control register 1 (AD1)				ADC14		ADC12	ADC11	ADC10	0 0 0 ? 0 0 0 0								
ED <sub>16</sub>	A-D control register 2 (AD2)			ADC25	ADC24	ADC23	ADC22	ADC21	ADC20	00 <sub>16</sub>								
EE <sub>16</sub>	Timer 5 (T5)									07 <sub>16</sub>								
EF <sub>16</sub>	Timer 6 (T6)									FF <sub>16</sub>								
F0 <sub>16</sub>	Timer 1 (T1)									FF <sub>16</sub>								
F1 <sub>16</sub>	Timer 2 (T2)									07 <sub>16</sub>								
F2 <sub>16</sub>	Timer 3 (T3)									FF <sub>16</sub>								
F3 <sub>16</sub>	Timer 4 (T4)									07 <sub>16</sub>								
F4 <sub>16</sub>	Timer mode register 1 (TM1)	TM17	TM16	TM15	TM14	TM13	TM12	TM11	TM10	00 <sub>16</sub>								
F5 <sub>16</sub>	Timer mode register 2 (TM2)	TM27	TM26	TM25	TM24	TM23	TM22	TM21	TM20	00 <sub>16</sub>								
F6 <sub>16</sub>	I <sup>2</sup> C data shift register (S0)	D7	D6	D5	D4	D3	D2	D1	D0	?								
F7 <sub>16</sub>	I <sup>2</sup> C address register (S0D)	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	RBW	00 <sub>16</sub>								
F8 <sub>16</sub>	I <sup>2</sup> C status register (S1)	MST	TRX	BB	PIN	AL	AAS	ADO	LRB	0 0 0 1 0 0 0 ?								
F9 <sub>16</sub>	I <sup>2</sup> C control register (S1D)	BSEL1	BSEL0	<sup>10</sup> BIT SAD	ALS	ESO	BC2	BC1	BC0	00 <sub>16</sub>								
FA <sub>16</sub>	I <sup>2</sup> C clock control register (S2)	ACK	ACK BIT	FAST MODE	CCR4	CCR3	CCR2	CCR1	CCR0	00 <sub>16</sub>								
FB <sub>16</sub>	CPU mode register (CPUM)	CM7	CM6	CM5	1	1	CM2	0	0	0 0 1 1 1 1 0 0								
FC <sub>16</sub>	Interrupt request register 1 (IREQ1)		IN3R	VSCR	OSDR	TM4R	TM3R	TM2R	TM1R	00 <sub>16</sub>								
FD <sub>16</sub>	Interrupt request register 2 (IREQ2)	0	TM56R	IICR	IN2R	CKR	SIR	DSR	IN1R	00 <sub>16</sub>								
FE <sub>16</sub>	Interrupt control register 1 (ICON1)		IN3E	VSCIE	OSDE	TM4E	TM3E	TM2E	TM1E	00 <sub>16</sub>								
FF <sub>16</sub>	Interrupt control register 2 (ICON2)	TM56C	TM56E	IICE	IN2E	CKE	SIE	DSE	IN1E	00 <sub>16</sub>								

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■ SFR2 Area (addresses 200<sub>16</sub> to 20F<sub>16</sub>)

<Bit allocation>

: } Function bit  
Name : }

: No function bit

0 : Fix this bit to "0"  
(do not write "1")

1 : Fix this bit to "1"  
(do not write "0")

<State immediately after reset>

0 : "0" immediately after reset

1 : "1" immediately after reset

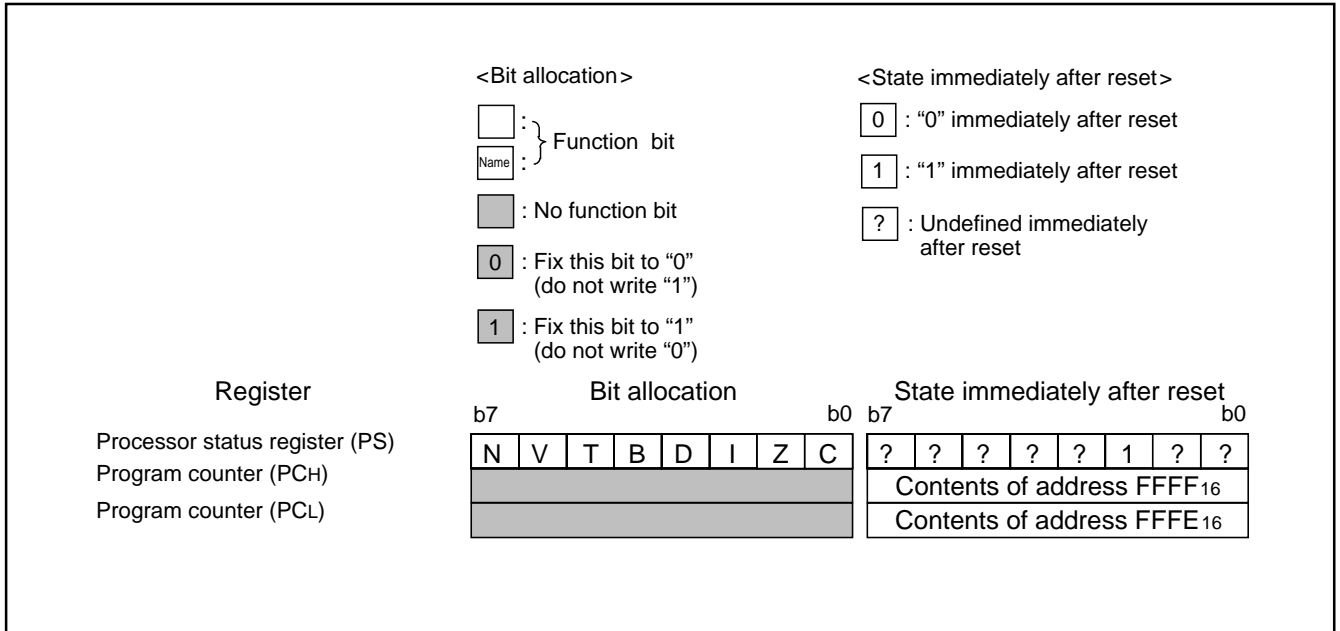
? : Undefined immediately  
after reset

Address	Register	Bit allocation								State immediately after reset									
		b7							b0	b7							b0		
200 <sub>16</sub>	PWM0 register (PWM0)																?		
201 <sub>16</sub>	PWM1 register (PWM1)																?		
202 <sub>16</sub>	PWM2 register (PWM2)																?		
203 <sub>16</sub>	PWM3 register (PWM3)																?		
204 <sub>16</sub>	PWM4 register (PWM4)																?		
205 <sub>16</sub>	PWM5 register (PWM5)																?		
206 <sub>16</sub>		00 <sub>16</sub>															?		
207 <sub>16</sub>		00 <sub>16</sub>															?		
208 <sub>16</sub>	PWM mode register 1 (PM1)						PM13										?		
209 <sub>16</sub>	PWM mode register 2 (PM2)	0	0	PM25	PM24	PM23	PM22	PM21	PM20						0	?	?	?	0
20A <sub>16</sub>	ROM correction address 1 (high-order)	ADH17	ADH16	ADH15	ADH14	ADH13	ADH12	ADH11	ADH10										
20B <sub>16</sub>	ROM correction address 1 (low-order)	ADL17	ADL16	ADL15	ADL14	ADL13	ADL12	ADL11	ADL10										
20C <sub>16</sub>	ROM correction address 2 (high-order)	ADH27	ADH26	ADH25	ADH24	ADH23	ADH22	ADH21	ADH20										
20D <sub>16</sub>	ROM correction address 2 (low-order)	ADL27	ADL26	ADL25	ADL24	ADL23	ADL22	ADL21	ADL20										
20E <sub>16</sub>	ROM correction enable register (RCR)								RC1	RC0								00 <sub>16</sub>	
20F <sub>16</sub>																		?	

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**Internal State of Processor Status Register and  
Program Counter at Reset**



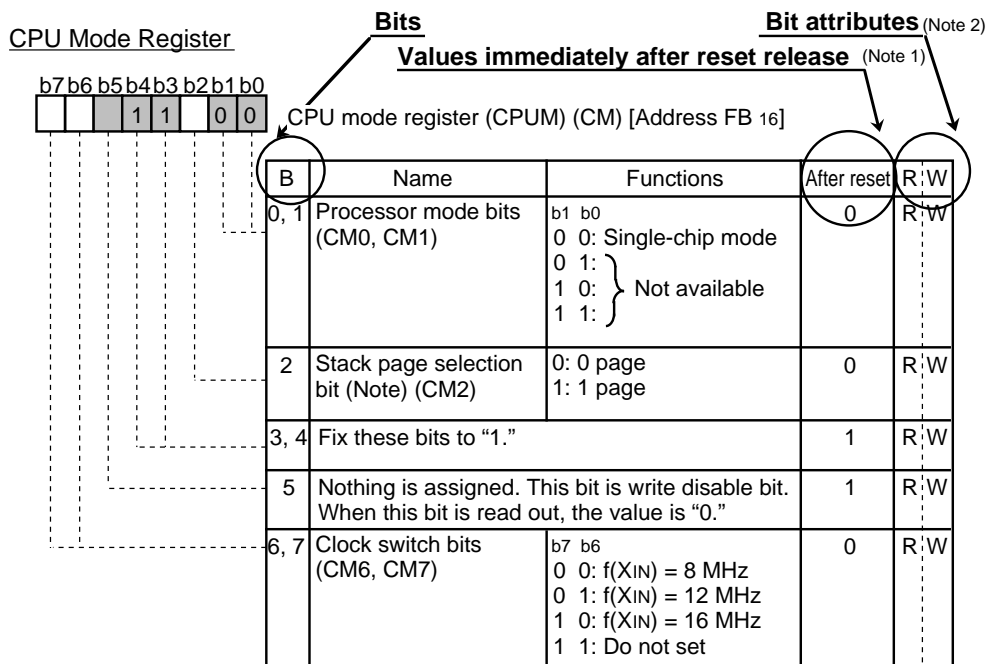
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**Structure of Register**

The figure of each register structure describes its functions, contents at reset, and attributes as follows:

**Example**



■ : Bit in which nothing is assigned

**Notes 1:** Values immediately after reset release

- 0....."0" after reset release
- 1....."1" after reset release
- ?.....Indeterminate after reset release

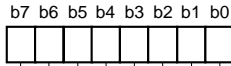
**2:** Bit attributes.....The attributes of control register bits are classified into 3 types : read-only, write-only and read and write. In the figure, these attributes are represented as follows :

- R.....Read
- W.....Write
- .....Read enabled
- .....Write enabled
- X.....Read disabled
- X.....Write disabled
- \*....."0" can be set by software, but "1" cannot be set.

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Port Pi Direction Register



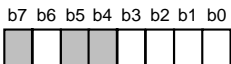
Port Pi direction register (PiD) (i=0 t2) [Addresses 00C1<sub>16</sub>, 00C3<sub>16</sub>, 00C5<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Port Pi direction register	0 : Port Pi <sub>0</sub> input mode 1 : Port Pi <sub>0</sub> output mode	0	R	W
1		0 : Port Pi <sub>1</sub> input mode 1 : Port Pi <sub>1</sub> output mode	0	R	W
2		0 : Port Pi <sub>2</sub> input mode 1 : Port Pi <sub>2</sub> output mode	0	R	W
3		0 : Port Pi <sub>3</sub> input mode 1 : Port Pi <sub>3</sub> output mode	0	R	W
4		0 : Port Pi <sub>4</sub> input mode 1 : Port Pi <sub>4</sub> output mode	0	R	W
5		0 : Port Pi <sub>5</sub> input mode 1 : Port Pi <sub>5</sub> output mode	0	R	W
6		0 : Port Pi <sub>6</sub> input mode 1 : Port Pi <sub>6</sub> output mode	0	R	W
7		0 : Port Pi <sub>7</sub> input mode 1 : Port Pi <sub>7</sub> output mode	0	R	W

Port Pi Direction Register

**Address 00C1<sub>16</sub>, 00C3<sub>16</sub>, 00C5<sub>16</sub>**

Port P3 Direction Register



Port P3 direction register (D3) [Address 00C7<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Port P3 direction register	0 : Port P3 <sub>0</sub> input mode 1 : Port P3 <sub>0</sub> output mode	0	R	W
1		0 : Port P3 <sub>1</sub> input mode 1 : Port P3 <sub>1</sub> output mode	0	R	W
2	Port P3 <sub>0</sub> output structure selection bit (P30C)	0 : CMOS output 1 : N-channel open-drain output	0	R	W
3	Port P3 <sub>1</sub> output structure selection bit (P30C)	0 : CMOS output 1 : N-channel open-drain output	0	R	W
4, 5, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
6	Timer 3 count source selection bit (T3SC)	Refer to Timer section.	0	R	W

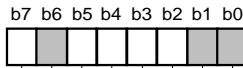
Port P3 Direction Register

**Address 00C7<sub>16</sub>**

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OSD Port Control Register



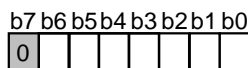
OSD port control register (PF) [Address 00CB<sub>16</sub>]

B	Name	Functions	After reset	R	W
0, 1	Fix these bits to "0."		0	R	W
2	Port P5 <sub>2</sub> output signal selection bit (PF2)	0 : R signal output 1 : Port P5 <sub>2</sub> output	0	R	W
3	Port P5 <sub>3</sub> output signal selection bit (PF3)	0 : G signal output 1 : Port P5 <sub>3</sub> output	0	R	W
4	Port P5 <sub>4</sub> output signal selection bit (PF4)	0 : B signal output 1 : Port P5 <sub>4</sub> output	0	R	W
5	Port P5 <sub>5</sub> output signal selection bit (PF5)	0 : OUT1 signal output 1 : Port P5 <sub>3</sub> output	0	R	W
6	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
7	Port P1 <sub>0</sub> output signal selection bit (PF7)	0 : Port P1 <sub>0</sub> output 1 : OUT2 signal output	0	R	W

OSD Port Control Register

**Address 00CB<sub>16</sub>**

OSD Control Register



OSD control register (OC) [Address 00D0<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	OSD control bit (OC0) (See note)	0 : All-blocks display off 1 : All-blocks display on	0	R	W
1	Automatic solid space control bit (OC1)	0 : OFF 1 : ON	0	R	W
2	Window control bit (OC2)	0 : OFF 1 : ON	0	R	W
3	CC mode clock selection bit (OC3)	0 : Data slicer clock 1 : Clock from OSC1 pin	0	R	W
4	OSD mode clock selection bit (OC4)	0 : Data slicer clock 1 : Clock from OSC1 pin	0	R	W
5, 6	OSC1 clock selection bit (OC5, OC6)	b6 b5 0 0: 32 kHz oscillating 0 1: Do not set. 1 0: LC oscillating, Ceramic oscillating 1 1: Do not set.	0	R	W
7	Fix this bit to "0."		0	R	W

**Note:** Even this bit is switched during display, the display screen remains unchanged until a rising (falling) of the next V SYNC.

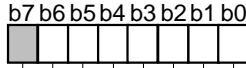
OSD Control Register

**Address 00D0<sub>16</sub>**

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
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Horizontal Position Register



Horizontal position register (HP) [Address 00D1<sub>16</sub>]

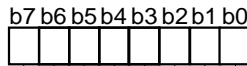
B	Name	Functions	After reset	R : W
0 to 6	Control bits of horizontal display start positions (HP <sub>0</sub> to HP <sub>6</sub> )	Horizontal display start positions 128 steps (00 <sub>16</sub> to 7F <sub>16</sub> ) (1 step is 4T <sub>osc</sub> )	0	R : W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R : —

**Note:** The setting value synchronizes with the V SYNC.

Horizontal Position Register

**Address 00D1<sub>16</sub>**

Block Control register i



Block control register i (BC<sub>i</sub>) (i=1, 2) [Addresses 00D2<sub>16</sub> and 00D3<sub>16</sub>]

B	Name	Functions	After reset	R : W																																									
0, 1	Display mode selection bits (BC <sub>i0</sub> , BC <sub>i1</sub> ) (See note 1)	<table border="0"> <tr> <td>b1</td> <td>b0</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>0: Display OFF</td> </tr> <tr> <td>0</td> <td>1</td> <td>1: CC mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>0: OSD mode (Border OFF)</td> </tr> <tr> <td>1</td> <td>1</td> <td>1: OSD mode (Border ON)</td> </tr> </table>	b1	b0		0	0	0: Display OFF	0	1	1: CC mode	1	0	0: OSD mode (Border OFF)	1	1	1: OSD mode (Border ON)	Indeterminate	R : W																										
b1	b0																																												
0	0	0: Display OFF																																											
0	1	1: CC mode																																											
1	0	0: OSD mode (Border OFF)																																											
1	1	1: OSD mode (Border ON)																																											
2, 3	Dot size selection bits (BC <sub>i2</sub> , BC <sub>i3</sub> ) (See note 2 and 3)	<table border="0"> <tr> <td>b4</td> <td>b3</td> <td>b2</td> <td>Pre-divide Ratio</td> <td>Dot Size</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td rowspan="3">× 2</td> <td>1T<sub>c</sub> × 1/2H</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1T<sub>c</sub> × 1H</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>2T<sub>c</sub> × 2H</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td></td> <td>3T<sub>c</sub> × 3H</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td rowspan="3">× 3</td> <td>1T<sub>c</sub> × 1/2H</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1T<sub>c</sub> × 1H</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>2T<sub>c</sub> × 2H</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td></td> <td>3T<sub>c</sub> × 3H</td> </tr> </table>	b4	b3	b2	Pre-divide Ratio	Dot Size	0	0	0	× 2	1T <sub>c</sub> × 1/2H	0	0	1	1T <sub>c</sub> × 1H	0	1	0	2T <sub>c</sub> × 2H	0	1	1		3T <sub>c</sub> × 3H	1	0	0	× 3	1T <sub>c</sub> × 1/2H	1	0	1	1T <sub>c</sub> × 1H	1	1	0	2T <sub>c</sub> × 2H	1	1	1		3T <sub>c</sub> × 3H	Indeterminate	R : W
b4	b3	b2	Pre-divide Ratio	Dot Size																																									
0	0	0	× 2	1T <sub>c</sub> × 1/2H																																									
0	0	1		1T <sub>c</sub> × 1H																																									
0	1	0		2T <sub>c</sub> × 2H																																									
0	1	1		3T <sub>c</sub> × 3H																																									
1	0	0	× 3	1T <sub>c</sub> × 1/2H																																									
1	0	1		1T <sub>c</sub> × 1H																																									
1	1	0		2T <sub>c</sub> × 2H																																									
1	1	1		3T <sub>c</sub> × 3H																																									
4	Pre-divide ratio selection bit (BC <sub>i4</sub> ) (See note 2 and 3)		Indeterminate	R : W																																									
5	OUT1/OUT2 output control bit (BC <sub>i5</sub> ) (See note 1)	0: OUT1 output control 1: OUT2 output control	Indeterminate	R : W																																									
6	Vertical display start position control bit (BC <sub>i6</sub> )	BC <sub>16</sub> : Block 1 BC <sub>26</sub> : Block 1	Indeterminate	R : W																																									
7	Window top/bottom boundary control bit (BC <sub>i7</sub> )	BC <sub>17</sub> : Window top boundary BC <sub>27</sub> : Window bottom boundary	Indeterminate	R : W																																									

**Notes 1:** Bit RA<sub>3</sub> of OSD RAM controls OUT1 output when bit 5 is "0."  
Bit RA<sub>3</sub> of OSD RAM controls OUT2 output when bit 5 is "1."  
**2:** T<sub>c</sub> : OSD clock cycle divided in the pre-divide circuit  
**3:** H : H<sub>SYNC</sub>

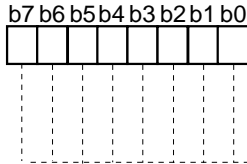
Block Control Register

**Address 00D2<sub>16</sub>, 00D3<sub>16</sub>**

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Vertical Position Register i



Vertical position register i (VPi) (i = 1 and 2) [Addresses 00D4<sub>16</sub>, 00D5<sub>16</sub>]

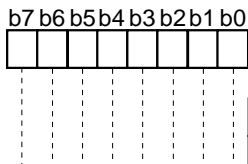
B	Name	Functions	After reset	R : W
0 to 7	Control bits of vertical display start positions (VPi0 to VPi7) (See note)	Vertical display start positions (low-order 8 bits) TH X (setting value of BCi6 × 16 <sup>2</sup> + setting value of low-order 4 bits of VPi × 16 <sup>1</sup> + setting value of low-order 4 bits of VPi × 16 <sup>0</sup> )	Indeterminate	R : W

**Note:** Set values except "00 16" to VPi when BCi6 is "0."

Vertical Position Register

**Address 00D4<sub>16</sub>, 00D5<sub>16</sub>**

Window Register 1



Window register 1 (WN1) [Addresses 00D6<sub>16</sub>]

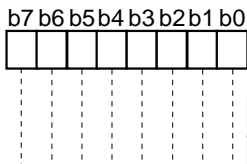
B	Name	Functions	After reset	R : W
0 to 7	Control bits of window top boundary (WN10 to WN17) (See note 1)	Top boundary position (low-order 8 bits) TH X (setting value of BC17 × 16 <sup>2</sup> + setting value of low-order 4 bits of WN1 × 16 <sup>1</sup> + setting value of low-order 4 bits of WN1 × 16 <sup>0</sup> )	Indeterminate	R : W

**Notes 1:** Set values except "00 16" to the WN1 when BC17 is "0."  
**2:** TH is cycle of HSYNC.  
**3:** BC17 is bit 7 of the clock control register 1.

Window Register 1

**Address 00D6<sub>16</sub>**

Window Register 2



Window register 2 (WN2) [Addresses 00D7<sub>16</sub>]

B	Name	Functions	After reset	R : W
0 to 7	Control bits of window bottom boundary (WN20 to WN27) (See note 1)	Bottom boundary position (high-order 2 bits) TH X (setting value of BC17 × 16 <sup>2</sup> + setting value of low-order 4 bits of WN2 × 16 <sup>1</sup> + setting value of low-order 4 bits of WN2 × 16 <sup>0</sup> )	Indeterminate	R : W

**Notes 1:** Set values fit for the following condition: WN1 < WN2.  
**2:** TH is cycle of HSYNC.  
**3:** BC27 is bit 7 of the block control register 2.

Window Register 2

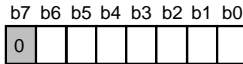
**Address 00D7<sub>16</sub>**



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I/O Polarity Control Register



I/O polarity control register (PC) [Address 00D8<sub>16</sub>]

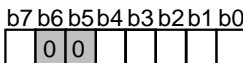
B	Name	Functions	After reset	R	W
0	H <sub>SYNC</sub> input polarity switch bit (PC0)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
1	V <sub>SYNC</sub> input polarity switch bit (PC1)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
2	R, G, B output polarity switch bit (PC2)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
3	OUT1 output polarity switch bit (PC3)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
4	OUT2 output polarity switch bit (PC4)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
5	Display dot line selection bit (PC5) (See note)	0 : "□" at even field "▨" at odd field 1 : "▨" at even field "□" at odd field	0	R	W
6	Field determination flag (PC6)	0 : Even field 1 : Odd field	1	R	—
7	Fix this bit to "0."		0	R	W

**Note:** Refer to the corresponding figure (P63).

I/O Polarity Control Register

**Address 00D8<sub>16</sub>**

Raster Color Register



Raster color register (RC) [Address 00D9<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Raster color R control bit (RC0)	0 : No output 1 : Output	0	R	W
1	Raster color G control bit (RC1)	0 : No output 1 : Output	0	R	W
2	Raster color B control bit (RC2)	0 : No output 1 : Output	0	R	W
3	Raster color OUT1 control bit (RC3)	0 : No output 1 : Output	0	R	W
4	Raster color OUT2 control bit (RC4)	0 : No output 1 : Output	0	R	W
5, 6	Fix these bits to "0."		0	R	W
7	Port function selection bit (RC7)	0 : OSC1/X <sub>CIN</sub> , OSC2/X <sub>COU</sub> 1 : P26, P27	0	R	W

**Note:** Either OSD clock source or 32 kHz oscillating clock is selected by bits 5 and 6 of the OSD control register.

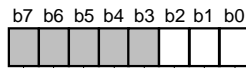
Raster Color Register

**Address 00D9<sub>16</sub>**

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
and ON-SCREEN DISPLAY CONTROLLER

**Interrupt Input Polarity Register**



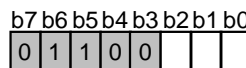
Interrupt input polarity register (RE) [Address 00DC<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	INT1 polarity switch bit (INT1)	0 : Positive polarity 1 : Negative polarity	0	R	W
1	INT2 polarity switch bit (INT2)	0 : Positive polarity 1 : Negative polarity	0	R	W
2	INT3 polarity switch bit (INT3)	0 : Positive polarity 1 : Negative polarity	0	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Interrupt Input Polarity Register

**Address 00DC<sub>16</sub>**

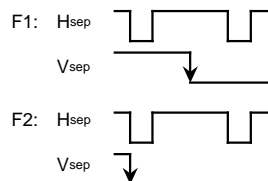
**Data Slicer Control Register 1**



Data slicer control register 1(DSC1) [Address 00E0<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Data slicer and timing signal generating circuit control bit (DSC10)	0: Stopped 1: Operating	0	R	W
1	Selection bit of data slice reference voltage generating field (DSC11)	0: F2 1: F1	0	R	W
2	Reference clock source selection bit (DSC12)	0: Video signal 1: HSYNC signal	0	R	W
3, 4, 7	Fix these bits to "0."		0	R	W
5, 6	Fix these bits to "1."		0	R	W

Definition of fields 1 (F1) and 2 (F2)



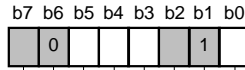
Data Slicer Control Register 1

**Address 00E0<sub>16</sub>**

**M37273MF-XXXSP**  
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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
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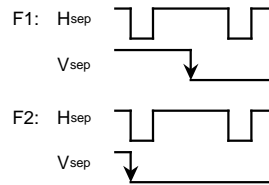
**Data Slicer Control Register 2**



Data slicer control register 2 (DSC2) [Address 00E1<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Caption data latch completion flag 1 (DSC20)	0: Data is not latched yet and a clock-run-in is not determined. 1: Data is latched and a clock-run-in is determined.	Indeterminate	R	—
1	Fix this bit to "1."		0	R	W
2, 7	Test bit	Read-only	Indeterminate	R	—
3	Field determination flag (DSC23)	0: F2 1: F1	Indeterminate	R	—
4	Vertical synchronous signal (V <sub>sep</sub> ) generating method selection bit (DSC24)	0: Method (1) 1: Method (2)	0	R	W
5	V-pulse shape determination flag (DSC25)	0: Match 1: Mismatch	Indeterminate	R	—
6	Fix this bit to "0."		0	R	W

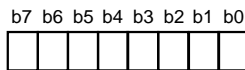
Definition of fields 1 (F1) and 2 (F2)



Data Slicer Control Register 2

**Address 00E1<sub>16</sub>**

**Clock Run-in Detect Register**



Clock run-in detect register (CRD) [Address 00E4<sub>16</sub>]

B	Name	Functions	After reset	R	W
0 to 2	Test bits	Read-only	0	R	—
3 to 7	Clock run-in detection bit (CRD3 to CRD7)	Number of reference clocks to be counted in one clock run-in pulse period.	0	R	—

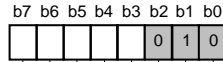
Clock Run-in Detection Register

**Address 00E4<sub>16</sub>**

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Data Clock Position Register



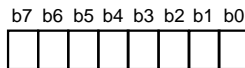
Data clock position register (DPS) [Address 00E5<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Fix these bits to "0."		1	R	W
2			0		
1	Fix this bit to "1."		0	R	W
3	Data clock position set bits (DPS3 to DPS7)		1	R	W
4 to 7			0		

Data Clock Position Register

**Address 00E5<sub>16</sub>**

Caption Position Register



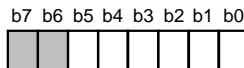
Caption Position Register (CPS) [Address 00E6<sub>16</sub>]

B	Name	Functions	After reset	R	W
0 to 4	Caption position bits (CPS0 to CPS4)		0	R	W
5	Caption data latch completion flag 2 (CPS1)	0: Data is not latched yet and a clock-run-in is not determined. 1: Data is latched and a clock-run-in is determined.	Indeterminate	R	—
6, 7	Slice line mode specification bits (in 1 field) (CPS6, CPS7)	Refer to the corresponding Table (P33).	0	R	W

Caption Position Register

**Address 00E6<sub>16</sub>**

Sync Pulse Counter Register



Sync pulse counter register (HC) [Address 00E9<sub>16</sub>]

B	Name	Functions	After reset	R	W
0 to 4	Count value (HC0 to HC4)		0	R	—
5	Count source (HC5)	0: H <sub>sync</sub> signal 1: Composite sync signal <Count time> $f(X_{IN})/2^{13}$ (1024 $\mu$ s, $f(X_{IN}) = 8$ MHz)	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

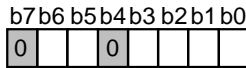
Sync Pulse Counter Register

**Address 00E9<sub>16</sub>**

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
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Serial I/O Mode Register



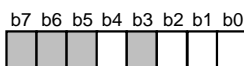
Serial I/O mode register (SM) [Address 00EB16]

B	Name	Functions	After reset	R	W
0, 1	Internal synchronous clock selection bits (SM0, SM1)	b1 b0 0 0: f(X <sub>IN</sub> )/4 or f(X <sub>CIN</sub> )/4 0 1: f(X <sub>IN</sub> )/16 or f(X <sub>CIN</sub> )/16 1 0: f(X <sub>IN</sub> )/32 or f(X <sub>CIN</sub> )/32 1 1: f(X <sub>IN</sub> )/64 or f(X <sub>CIN</sub> )/64	0	R	W
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R	W
3	Port function selection bit (SM3)	0: P20, P21 1: SCLK, SOUT	0	R	W
4, 7	Fix these bits to "0."		0	R	W
5	Transfer direction selection bit (SM5)	0: LSB first 1: MSB first	0	R	W
6	Transfer clock input pin selection bit (SM6)	0: Input signal from S <sub>IN</sub> pin 1: Input signal from S <sub>OUT</sub> pin	0	R	W

Serial I/O Mode Register

**Address 00EB16**

A-D Control Register 1



A-D control register 1 (AD1) [Address 00EC16]

B	Name	Functions	After reset	R	W
0 to 2	Analog input pin selection bits (ADC10 to ADC12)	b2 b1 b0 0 0 0: AD1 0 0 1: AD2 0 1 0: AD3 0 1 1: AD4 1 0 0: AD5 1 0 1: AD6 1 1 0: } Do not set. 1 1 1: }	0	R	W
3, 5 to 7	Nothing is assigned. This bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
4	Storage bit of comparison result (ADM4)	0: Input voltage < reference voltage 1: Input voltage > reference voltage	Indeterminate	R	W

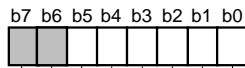
AD Control Register 1

**Address 00EC16**

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
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A-D Control Register 2



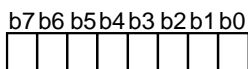
A-D control register 2 (AD2) [Address 00ED16]

B	Name	Functions	After reset	R	W
0 to 5	D-A converter set bits (ADC20 to ADC25)	b5 b4 b3 b2 b1 b0 Reference voltage Vref 0 0 0 0 0 0 : 1/128Vcc 0 0 0 0 0 1 : 3/128Vcc 0 0 0 0 1 0 : 5/128Vcc ⋮ 1 1 1 1 0 1 : 123/128Vcc 1 1 1 1 1 0 : 125/128Vcc 1 1 1 1 1 1 : 127/128Vcc	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

AD Control Register 2

**Address 00ED16**

Timer Mode Register 1



Timer mode register 1 (TM1) [Address 00F416]

B	Name	Functions	After reset	R	W
0	Timer 1 count source selection bit 1 (TM10)	0: f(XIN)/16 or f(XCIN)/16 (Note) 1: Count source selected by bit 5 of TM1	0	R	W
1	Timer 2 count source selection bit 1 (TM11)	0: Count source selected by bit 4 of TM1 1: External clock from TIM2 pin	0	R	W
2	Timer 1 count stop bit (TM12)	0: Count start 1: Count stop	0	R	W
3	Timer 2 count stop bit (TM13)	0: Count start 1: Count stop	0	R	W
4	Timer 2 count source selection bit 2 (TM14)	0: f(XIN)/16 or f(XCIN)/16 (See note) 1: Timer 1 overflow	0	R	W
5	Timer 1 count source selection bit 2 (TM15)	0: f(XIN)/4096 or f(XCIN)/4096 (See note) 1: External clock from TIM2 pin	0	R	W
6	Timer 5 count source selection bit 2 (TM16)	0: Timer 2 overflow 1: Timer 4 overflow	0	R	W
7	Timer 6 internal count source selection bit (TM17)	0: f(XIN)/16 or f(XCIN)/16 (See note) 1: Timer 5 overflow	0	R	W

**Note:** Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register.

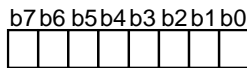
Timer Mode Register 1

**Address 00F416**

**M37273MF-XXXSP**  
**M37273EFSP**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
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Timer Mode Register 2



Timer mode register 2 (TM2) [Address 00F5<sub>16</sub>]

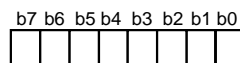
B	Name	Functions	After reset	R	W
0	Timer 3 count source selection bit (TM20)	(b6 at address 00C7 <sub>16</sub> ) b0 0 0 : f(X <sub>IN</sub> )/16 or f(X <sub>CIN</sub> )/16 (See note) 0 1 : f(X <sub>CIN</sub> ) 1 0 : } External clock from TIM3 pin 1 1 : }	0	R	W
1, 4	Timer 4 count source selection bits (TM21, TM24)	b4 b1 0 0 : Timer 3 overflow signal 0 1 : f(X <sub>IN</sub> )/16 or f(X <sub>CIN</sub> )/16 (See note) 1 0 : f(X <sub>IN</sub> )/2 or f(X <sub>CIN</sub> )/2 (See note) 1 1 : f(X <sub>CIN</sub> )	0	R	W
2	Timer 3 count stop bit (TM22)	0: Count start 1: Count stop	0	R	W
3	Timer 4 count stop bit (TM23)	0: Count start 1: Count stop	0	R	W
5	Timer 5 count stop bit (TM25)	0: Count start 1: Count stop	0	R	W
6	Timer 6 count stop bit (TM26)	0: Count start 1: Count stop	0	R	W
7	Timer 5 count source selection bit 1 (TM27)	0: f(X <sub>IN</sub> )/16 or f(X <sub>CIN</sub> )/16 (See note) 1: Count source selected by bit 6 of TM1	0	R	W

**Note:** Either f(X<sub>IN</sub>) or f(X<sub>CIN</sub>) is selected by bit 7 of the CPU mode register.

Timer Mode Register 2

**Address 00F5<sub>16</sub>**

I<sup>2</sup>C Data Shift Register



I<sup>2</sup>C data shift register1(S0) [Address 00F6<sub>16</sub>]

B	Name	Functions	After reset	R	W
0 to 7	D0 to D7	This is an 8-bit shift register to store receive data and write transmit data.	Indeterminate	R	W

**Note:** To write data into the I<sup>2</sup>C data shift register after setting the MST bit to "0" (slave mode), keep an interval of 8 machine cycles or more.

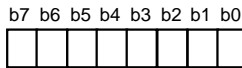
I<sup>2</sup>C Data Shift Register

**Address 00F6<sub>16</sub>**

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
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**I<sup>2</sup>C Address Register**



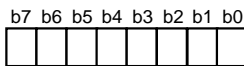
I<sup>2</sup>C address register (S0D) [Address 00F7<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Read/write bit (RBW)	0: Read 1: Write	0	R	—
1 to 7	Slave address (SAD0 to SAD6)	The address data transmitted from the master is compared with the contents of these bits.	0	R	W

I<sup>2</sup>C Address register

**Address 00F7<sub>16</sub>**

**I<sup>2</sup>C Status Register**



I<sup>2</sup>C status register (S1) [Address 00F8<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Last receive bit (LRB) (See note)	0 : Last bit = "0" 1 : Last bit = "1"	Indeterminate	R	—
1	General call detecting flag (AD0) (See note)	0 : No general call detected 1 : General call detected	0	R	—
2	Slave address comparison flag (AAS) (See note)	0 : Address mismatch 1 : Address match	0	R	—
3	Arbitration lost detecting flag (AL) (See note)	0 : Not detected 1 : Detected	0	R	—
4	I <sup>2</sup> C-BUS interface interrupt request bit (PIN)	0 : Interrupt request issued 1 : No interrupt request issued	0	R	—
5	Bus busy flag (BB)	0 : Bus free 1 : Bus busy	0	R	W
6, 7	Communication mode specification bits (TRX, MST)	b7 b6 0 0 : Slave receive mode 0 1 : Slave transmit mode 1 0 : Master receive mode 1 1 : Master transmit mode	0	R	W

**Note :** These bits and flags can be read out, but cannot be written.

I<sup>2</sup>C Status Register

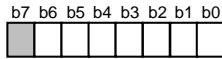
**Address 00F8<sub>16</sub>**



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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
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I<sup>2</sup>C Control Register



I<sup>2</sup>C control register (S1D) [Address 00F9<sub>16</sub>]

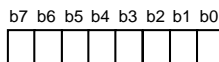
B	Name	Functions	After reset	R : W
0 to 2	Bit counter (Number of transmit/receive bits) (BC0 to BC2)	b2 b1 b0 0 0 0 : 8 0 0 1 : 7 0 1 0 : 6 0 1 1 : 5 1 0 0 : 4 1 0 1 : 3 1 1 0 : 2 1 1 1 : 1	0	R : W
3	I <sup>2</sup> C-BUS interface use enable bit (ESO)	0 : Disabled 1 : Enabled	0	R : W
4	Data format selection bit (ALS)	0 : Addressing mode 1 : Free data format	0	R : W
5	Addressing format selection bit (10BIT SAD)	0 : 7-bit addressing format 1 : 10-bit addressing format	0	R : W
6, 7	Connection control bits between I <sup>2</sup> C-BUS interface and ports	b7 b6 Connection port (See note) 0 0 : None 0 1 : SCL1, SDA1 1 0 : SCL2, SDA2 1 1 : SCL1, SDA1 SCL2, SDA2	0	R : W

**Note:** When using ports P1<sub>1</sub>-P1<sub>4</sub> as I<sup>2</sup>C-BUS interface, the output structure changes automatically from CMOS output to N-channel open-drain output.

I<sup>2</sup>C Control register

**Address 00F9<sub>16</sub>**

I<sup>2</sup>C Clock Control Register



I<sup>2</sup>C clock control register (S2) [Address 00FA<sub>16</sub>]

B	Name	Functions	After reset	R : W		
0 to 4	SCL frequency control bits (CCR0 to CCR4)	Setup value of CCR4-CCR0	Standard clock mode	High speed clock mode	0	R : W
		00 to 02	Setup disabled	Setup disabled		
		03	Setup disabled	333		
		04	Setup disabled	250		
		05	100	400 (See note)		
		06	83.3	166		
		⋮	500/CCR value	1000/CCR value		
		1D	17.2	34.5		
		1E	16.6	33.3		
		1F	16.1	32.3		
			(at φ = 4 MHz, unit : kHz)			
5	SCL mode specification bit (FAST MODE)	0 : Standard clock mode 1 : High-speed clock mode	0	R : W		
6	ACK bit (ACK BIT)	0 : ACK is returned. 1 : ACK is not returned.	0	R : W		
7	ACK clock bit (ACK)	0 : No ACK clock 1 : ACK clock	0	R : W		

**Note:** At 4000kHz in the high-speed clock mode, the duty is as below .  
"0" period : "1" period = 3 : 2  
In the other cases, the duty is as below.  
"0" period : "1" period = 1 : 1

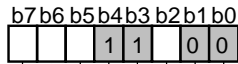
I<sup>2</sup>C Clock Control Register

**Address 00FA<sub>16</sub>**

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
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CPU Mode Register



CPU mode register (CPUM (CM)) [Address FB16]

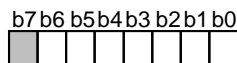
B	Name	Functions	After reset	R : W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: } Not available 1 0: } 1 1: }	0	R : W
2	Stack page selection bit (CM2) (See note)	0: 0 page 1: 1 page	1	R : W
3, 4	Fix these bits to "1."		1	R : W
5	XcOUT drivability selection bit (CM5)	0: LOW drive 1: HIGH drive	1	R : W
6	Main Clock (XIN-XOUT) stop bit (CM6)	0: Oscillating 1: Stopped	0	R : W
7	Internal system clock selection bit (CM7)	0: XIN-XOUT selected (high-speed mode) 1: XCIN-XCOUT selected (high-speed mode)	0	R : W

**Note:** This bit is set to "1" after the reset release.

CPU Mode Register

**Address 00FB16**

Interrupt Request Register 1



Interrupt request register 1 (IREQ1) [Address 00FC16]

B	Name	Functions	After reset	R : W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R : *
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R : *
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R : *
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R : *
4	OSD interrupt request bit (OSDR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R : *
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R : *
6	INT3 interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R : *
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R : —

\*: "0" can be set by software, but "1" cannot be set.

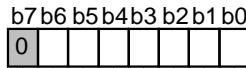
Interrupt Request Register 1

**Address 00FC16**

**M37273MF-XXXSP**  
**M37273EFSP**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER  
and ON-SCREEN DISPLAY CONTROLLER

Interrupt Request Register 2



Interrupt request register 2 (IREQ2) [Address 00FD<sub>16</sub>]

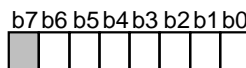
B	Name	Functions	After reset	R : W
0	INT1 interrupt request bit (INIR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R : *
1	Data slicer interrupt request bit (DSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R : *
2	Serial I/O interrupt request bit (S1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R : *
3	f(XIN)/4096 interrupt request bit (CKR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R : *
4	INT2 interrupt request bit (IN2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R : *
5	Multi-master I <sup>2</sup> C-BUS interrupt request bit (IICR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R : *
6	Timer 5 • 6 interrupt request bit (TM56R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R : *
7	Fix this bit to "0."		0	R : W

\*: "0" can be set by software, but "1" cannot be set.

Interrupt Request Register 2

**Address 00FD<sub>16</sub>**

Interrupt Control Register 1



Interrupt control register 1 (ICON1) [Address 00FE<sub>16</sub>]

B	Name	Functions	After reset	R : W
0	Timer 1 interrupt enable bit (TM1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R : W
1	Timer 2 interrupt enable bit (TM2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R : W
2	Timer 3 interrupt enable bit (TM3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R : W
3	Timer 4 interrupt enable bit (TM4E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R : W
4	OSD interrupt enable bit (OSDE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R : W
5	VSYNC interrupt enable bit (VSCE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R : W
6	INT3 interrupt enable bit (IN3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R : W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R : —

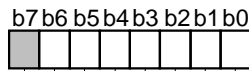
Interrupt Control Register 1

**Address 00FE<sub>16</sub>**

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Interrupt Control Register 2



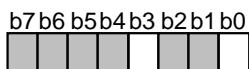
Interrupt control register 2 (ICON2) [Address 00FF<sub>16</sub>]

B	Name	Functions	After reset	R : W
0	INT1 interrupt enable bit (IN1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R : W
1	Data slicer interrupt enable bit (DSE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R : W
2	Serial I/O interrupt enable bit (SIE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R : W
3	f(XIN)/4096 interrupt enable bit (CKE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R : W
4	INT2 interrupt enable bit (IN2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R : W
5	Multi-master I <sup>2</sup> C-BUS interface interrupt enable bit (IICE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R : W
6	Timer 5 • 6 interrupt enable bit (TM56E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R : W
7	Timer 5 • 6 interrupt switch bit (TM56C)	0 : Timer 5 1 : Timer 6	0	R : W

Interrupt Control Register 2

**Address 00FF<sub>16</sub>**

PWM Mode Register 1



PWM mode register 1 (PM1) [Address 0208<sub>16</sub>]

B	Name	Functions	After reset	R : W
0	PWM counts source selection bit (PM10)	0 : Count source supply 1 : Count source stop	0	R : W
1, 2 4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		Indeterminate	R : —
3	PWM output polarity selection bit (PM13)	0 : Positive polarity 1 : Negative polarity	0	R : W

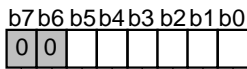
PWM Mode Register 1

**Address 0208<sub>16</sub>**

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PWM Mode Register 2



PWM mode register 2 (PM2) [Address 0209<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	P0 <sub>0</sub> /PWM0 output selection bit (PM2 <sub>0</sub> )	0 : P0 <sub>0</sub> output 1 : PWM0 output	0	R	W
1	P0 <sub>1</sub> /PWM1 output selection bit (PM2 <sub>1</sub> )	0 : P0 <sub>1</sub> output 1 : PWM1 output	0	R	W
2	P0 <sub>2</sub> /PWM2 output selection bit (PM2 <sub>2</sub> )	0 : P0 <sub>2</sub> output 1 : PWM2 output	0	R	W
3	P0 <sub>3</sub> /PWM3 output selection bit (PM2 <sub>3</sub> )	0 : P0 <sub>3</sub> output 1 : PWM3 output	0	R	W
4	P0 <sub>4</sub> /PWM4 output selection bit (PM2 <sub>4</sub> )	0 : P0 <sub>4</sub> output 1 : PWM4 output	0	R	W
5	P0 <sub>5</sub> /PWM5 output selection bit (PW2 <sub>5</sub> )	0: P0 <sub>5</sub> output 1: PWM5 output	0	R	W
6, 7	Fix these bits to "0."		0	R	W

PWM Mode Register 2

**Address 0209<sub>16</sub>**

ROM Correction Enable Register



ROM correction enable register (RCR) [Address 020E<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Block 1 enable bit (RC <sub>0</sub> )	0: Disabled 1: Enabled	0	R	W
1	Block 2 enable bit (RC <sub>1</sub> )	0: Disabled 1: Enabled	0	R	W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

ROM Correction Enable Register

**Address 020E<sub>16</sub>**

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REVISION DESCRIPTION LIST

M37273MF-XXXSP, M37273EFSP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	971130