KM4216C258

CMOS VIDEO RAM

256K x 16 Bit CMOS Video RAM

FEATURES

- Dual port Architecture
  256K x 16 bits RAM port
  512 x 16 bits SAM port
- Performance range :

Parameter \ Speed		-5	-6	-7
RAM access time (t_{RAC})		50ns	60ns	70ns
RAM access time (t_{CAC})		15ns	15ns	20ns
RAM cycle time (t_{RC})		85ns	104ns	130ns
RAM page cycle (t_{HPC})		20ns	24ns	28ns
SAM access time (t_{SCA})		15ns	15ns	17ns
SAM cycle time (t_{SCC})		18ns	18ns	20ns
RAM active corrent	KM4216C258	130m	120m	110m
SAM active current	KM4216C258	40mA	50mA	45mA

- Fast Page Mode with Extended Data Out
- RAM Read, Write, Read-Modify-Write
- Serial Read (SR)
- Read / Real time read transfer (RT, RRT)
- Split Read Transfer with Stop Operation (SRT)
- 2 $\overline{CAS}$ Byte / Word Read / Write Operation
- 8 Column Block Write (BW) and Write-per-Bit
  with Masking Operation (New and Old Mask)
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh
- Common Data I/O Using three state RAM Output Control
- All Inputs and Outputs TTL Compatible
- Refresh : 512 Cycle/8ms
- Single +5V $\pm$ 10% Supply Voltage
- Plastic 64-Pin 525mil SSOP (0.8mm pin pitch)

GENERAL DESCRIPTION

The Samsung KM4216C258 is a CMOS 256K x 16 bit Dual Port DRAM. It consists of a 256K x 16 dynamic random access memory (RAM) port and 512 x 16 static serial access memory (SAM) port. The RAM and SRAM port operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 8192 bits. It operates like a conventional 256K x 16 CMOS DRAM. The RAM port has a write per bit mask capability. Data may be written with New and Old Mask. The RAM port has a Fast Page mode access with Extended Data out, Byte/Word write operation and Block Write capabilities.

The SAM port consists of sixteen 512 bit high speed shift registers that are connected to the RAM array through a 8192 bit data transfer gate. The SAM port has serial read capability.

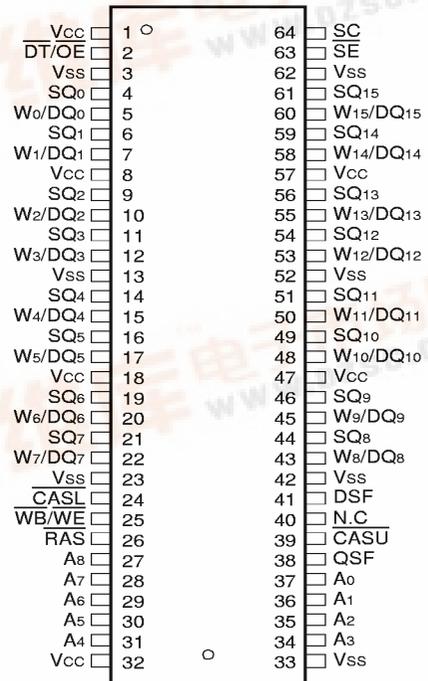Data may be internally transferred from the RAM to SAM port using read, and programmable (Stop Register) Split Transfers. Refresh is accomplished by familiar DRAM refresh modes. The KM4216C258 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

All inputs and I/O s are TTL level compatible. All address lines and data inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

PIN CONFIGURATION (TOP VIEWS)
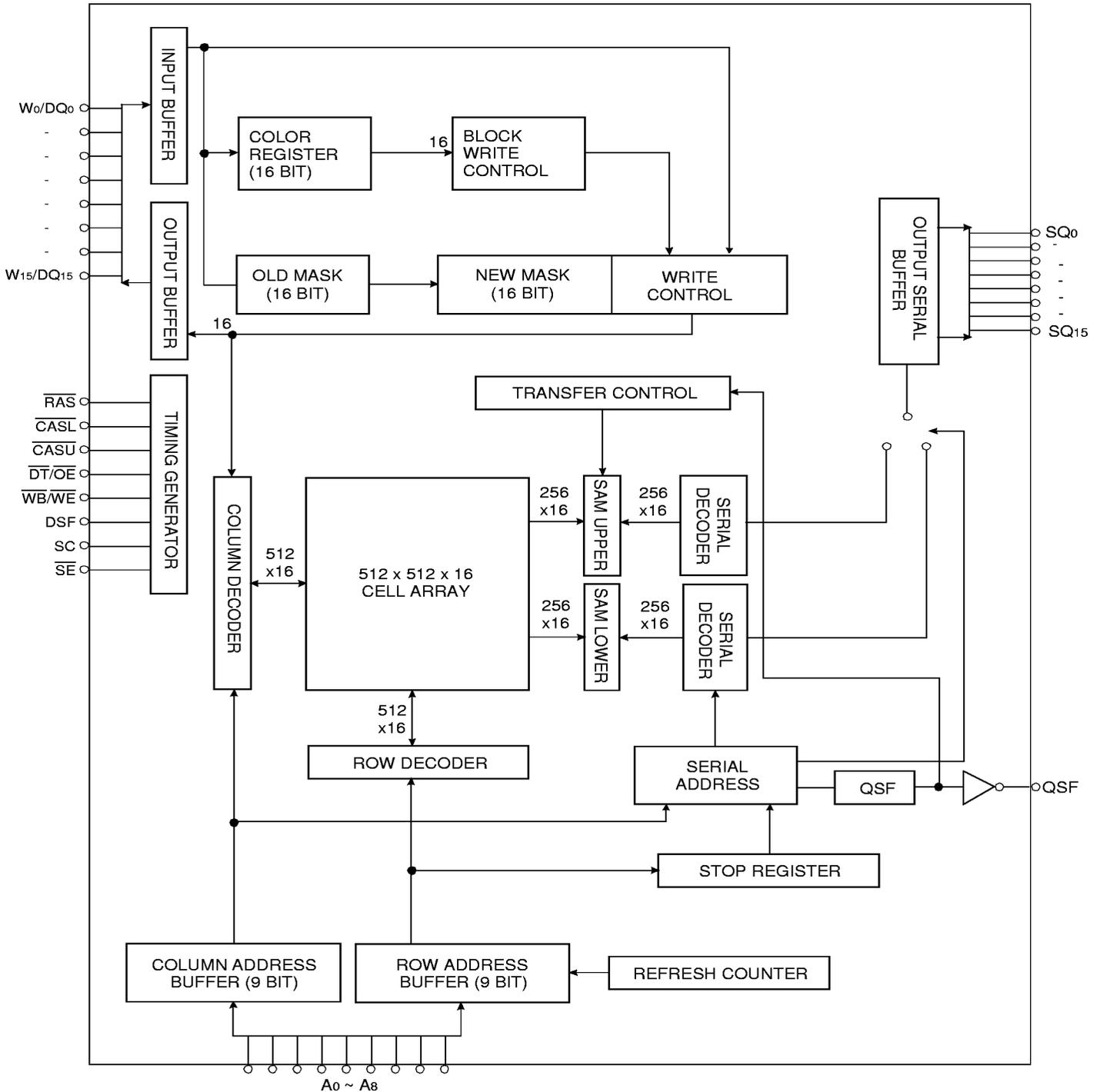
64-Pin 525 mil SSOP

Left	Pin		Pin	Right
V_{CC}	1		64	SC
$\overline{DT}$/$\overline{OE}$	2		63	$\overline{SE}$
V_{SS}	3		62	V_{SS}
SQ$_0$	4		61	SQ$_{15}$
W$_0$/DQ$_0$	5		60	W$_{15}$/DQ$_{15}$
SQ$_1$	6		59	SQ$_{14}$
W$_1$/DQ$_1$	7		58	W$_{14}$/DQ$_{14}$
V_{CC}	8		57	V_{CC}
SQ$_2$	9		56	SQ$_{13}$
W$_2$/DQ$_2$	10		55	W$_{13}$/DQ$_{13}$
SQ$_3$	11		54	SQ$_{12}$
W$_3$/DQ$_3$	12		53	W$_{12}$/DQ$_{12}$
V_{SS}	13		52	V_{SS}
SQ$_4$	14		51	SQ$_{11}$
W$_4$/DQ$_4$	15		50	W$_{11}$/DQ$_{11}$
SQ$_5$	16		49	SQ$_{10}$
W$_5$/DQ$_5$	17		48	W$_{10}$/DQ$_{10}$
V_{CC}	18		47	V_{CC}
SQ$_6$	19		46	SQ$_9$
W$_6$/DQ$_6$	20		45	W$_9$/DQ$_9$
SQ$_7$	21		44	SQ$_8$
W$_7$/DQ$_7$	22		43	W$_8$/DQ$_8$
V_{SS}	23		42	V_{SS}
$\overline{CASL}$	24		41	DSF
$\overline{WB}$/$\overline{WE}$	25		40	N.C
$\overline{RAS}$	26		39	$\overline{CASU}$
A$_8$	27		38	QSF
A$_7$	28		37	A$_0$
A$_6$	29		36	A$_1$
A$_5$	30		35	A$_2$
A$_4$	31		34	A$_3$
V_{CC}	32		33	V_{SS}

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PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTION
$\overline{RAS}$	IN	Row address strobe. $\overline{RAS}$ is used to clock in the 9 row bits for another input signal. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high"
$\overline{CASL}, \overline{CASU}$	IN	Column address strobe. $\overline{CASL}$, $\overline{CASU}$ are used to clock in the 9 column address bits as a strobe forthe DSF inputs and used to Byte/Word Read, Write Operation.
Address	IN	Address inputs for the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 262,144 available. 9 row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following 9 column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).
$\overline{WB}/\overline{WE}$	IN	The $\overline{WB}/\overline{WE}$ input is a multi-function pin. When $\overline{WB}/\overline{WE}$ is "High" at the falling edge of $\overline{RAS}$, during RAM port operation, it is used to write data into the memory array in the same as a standard DRAM. When $\overline{WB}/\overline{WE}$ is "Low" at the falling edge of $\overline{RAS}$, during RAM port operation, the W-P-B function is enabled.
$\overline{DT}/\overline{OE}$	IN	The $\overline{DT}/\overline{OE}$ input is also a multi-function pin. Enables an internal Transfer operation at the falling edge of $\overline{RAS}$ when Transfer is enable.
DSF	IN	DSF is used to indicate which special functions (BW, FW, Split Transfer, etc.) are used for a particular access cycle.
Wi/DQi	IN/OUT	Data I/O for DRAM access. These pins act as inputs for Mask and register load cycles, DQ Mask and Column Mask for BW.
SC	IN	Clock input to the serial address counter and data latch for the SAM register.
SQi	OUT	Serial output pin for serial read.(Serial write is not supported)
QSF	OUT	QSF indicates which half of the SAM is being accessed. Low if address is 0~255, High if address is 256~511.
$\overline{SE}$	IN	In a serial read cycle, $\overline{SE}$ is used as an output control. When $\overline{SE}$ is "High", serial access is disabled, however, the serial address pointer is still incremented while SC is clocked.
Vcc	SUPPLY	Power supply
Vss	SUPPLY	Ground

FUNCTIONAL BLOCK DIAGRAM

FUNCTION TRUTH TABLE

Mnemonic Code	RAS ⎍				CAS ⎍	Address		DQi Input		Register		Function
	CAS	DT/OE	WE	DSF	DSF	RAS	CAS	RAS	CAS/WE	Mask	Color	
CBRS (Note 1,3)	0	X	0	1	-	Stop (Note4)	-	X	-	-	-	CBR Refresh/Stop (No reset)
CBRN (Note 1)	0	X	1	1	-	X	-	X	-	-	-	CBR Refresh (No reset)
CBRR (Note 1)	0	X	X	0	-	X	-	X	-	-	-	CBR Refresh (Option reset)
ROR	1	1	X	0	-	Row	-	X	-	-	-	RAS - only Refresh
RT	1	0	1	0	X	Row	Tap	X	X	-	-	Read Transfer
SRT	1	0	1	1	X	Row	Tap	X	X	-	-	Split Read Transfer
RWM	1	1	0	0	0	Row	Col.	WMi	Data	Use	-	Masked Write (New / Old Mask)
BWM	1	1	0	0	1	Row	Col.	WMi	Column Mask	Use	Use	Masked Block Write (New / Old Mask)
RW	1	1	1	0	0 (Note6)	Row	Col.	X	Data	-	-	Read or Write
BW	1	1	1	0	1	Row	Col.	X	Column Mask	-	Use	Block Write
LMR (Note 2)	1	1	1	1	0	Row (Note7)	X	X	WMi	Load (Note5)	-	Load(Old) Mask Register set Cycle
LCR	1	1	1	1	1	Row (Note7)	X	X	Color	-	Load	Load Color Register set Cycle

X : Don t Care, - : Not Applicable, Tap : SAM Start (Column) Address, WMi : Write Mask Data (i=0 ~15)
RAS only refresh does not reset Stop or LMR functions.

Notes :

(1) CBRS, CBRN and CBRR all perform CAS-before-RAS refresh cycles. CBRR is used to reset all options and either
    CBRS or CBRN is used to continue to refresh the RAM without clearing any of the options.
(2) After LMR cycle, RWM and BWM use old mask. (Use CBRR reset to new mask, use CBRS or CBRN to perform
    CAS-before-RAS refresh while using Old mask)
(3) After CBRS cycle, SRT use Stop Register as a boundary address.
(4) Stop defines the column on which shift out moves to the other half of the SAM.
(5) After LMR, Mask Register is only changed by the another LMR or CBRR cycle.
(6) In the case of read cycle, DSF is don t care
(7) The Row that is addressed will be refreshed, but a Row address is not required.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating KM4216C256	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on Supply Relative to Vss	V_{CC}	-1 to + 7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power dissipation	P_D	1	W
Short circuit output current	Ios	50	mA

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage Reference to Vss, T_A = 0 to 70°C)

Item	Symbol	KM4216C258			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1V	V
Input Low Voltage	V_{IL}	- 1.0	-	0.8	V

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current { Any Input $0 \leq V_{IN} \leq V_{CC}$ +0.5V, all other pins not under test = 0 volts.}	I_{IL}	-10	10	uA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	I_{OL}	-10	10	uA
Output High Voltage Level (RAM I_{OH}=-2mA, SAM I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL}= 2mA, SAM I_{OL}= 2mA)	V_{OL}	-	0.4	V

CAPACITANCE (V_{CC} = 5V, f=1MHz, T_A=25 °C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0 ~ A_8)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, $\overline{DT/OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0 ~ W_{15}/DQ_{15})	C_{DQ}	2	7	pF
Output Capacitance (SQ_0~SQ_{15}, QSF)	C_{SQ}	2	7	pF

DC AND OPERATING CHARACTERISTICS
(Recommended operating conditions unless otherwise noted)

Parameter (RAM Port)	SAM port	Symbol	KM4216C258			Unit
			-5	-6	-7	
Operating Current*1	Standby *2	I_{CC1}	130	120	110	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min)	Active	I_{CC1} A	170	160	145	mA
Standby Current	Standby *2	I_{CC2}	10	10	10	mA
($\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ = V_{IH}, DSF=V_{IL})	Active	I_{CC2} A	55	50	45	mA
$\overline{RAS}$ Only Refresh Current *1	Standby *2	I_{CC3}	130	120	110	mA
($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	Active	I_{CC3} A	170	160	145	mA
Extended Fast Page Mode Current *1	Standby *2	I_{CC4}	130	120	110	mA
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min)	Active	I_{CC4} A	170	160	145	mA
$\overline{CAS}$- Before-$\overline{RAS}$ Refresh Current *1	Standby *2	I_{CC5}	130	120	110	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min)	Active	I_{CC5} A	170	160	145	mA
Data Transfer Current *1	Standby *2	I_{CC6}	160	140	130	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min)	Active	I_{CC6} A	190	180	165	mA
Block Write Cycle Current *1	Standby *2	I_{CC7}	130	120	110	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min)	Active	I_{CC7} A	170	160	145	mA
Color Register Load Current *1	Standby *2	I_{CC8}	120	110	90	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min)	Active	I_{CC8} A	170	140	125	mA

Note *1. Real values dependent on output loading and cycle rates. Specified values are obtained with the output open.
Icc is specified as average current.
In I_{CC1}, I_{CC3}, I_{CC6}, I_{CC7}, I_{CC8}, address transition should be changed only once while $\overline{RAS}$ = V_{IL}
In I_{CC4}, Address transition should be changed only once while $\overline{CAS}$ = V_{IH}
*2. SAM standby condition : $\overline{SE}$ ≥ V_{IH}, SC ≤ V_{IL} or ≥ V_{IH}

AC CHARACTERISTICS (0 °C ≤ TA ≤ 70 °C, KM4216C258 : Vcc=5.0V ± 10%)

Parameter	Symbol	-5*Note13 Min	-5*Note13 Max	-6 Min	-6 Max	-7 Min	-7 Max	Unit	Notes
Random read or write cycle time	tRC	85		104		124		ns	
Read-modify-write cycle time	tRWC	135		140		170		ns	
Hyper page mode cycle time	tHPC	20		25		30		ns	21
		25		30		35		ns	22
Hyper page read-modify-write cycle time	tHPRWC	66		70		74		ns	21
		72		76		81		ns	22
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,5,11
Access time from $\overline{CAS}$	tCAC		15		15		20	ns	3,5,6
Access time from column address	tAA		25		30		35	ns	3,11
Access time from $\overline{CAS}$ Precharge	tCPA		30		35		40	ns	3
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay	tOFF	3	15	3	15	3	15	ns	7
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	100K	60	100K	70	100K	ns	
$\overline{RAS}$ hold time	tRSH	15		15		20		ns	
$\overline{CAS}$ hold time	tCSH	45		45		55		ns	
$\overline{CAS}$ pulse width	tCAS	10	10K	10	10K	10	10K	ns	21
		15		15		15		ns	22
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	15	35	15	45	15	50	ns	5
$\overline{RAS}$ to column addr. delay time	tRAD	12	25	12	30	12	35	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
$\overline{CAS}$ precharge time (CBR Counter test cycle)	tCPT	15		20		25		ns	
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	6		10		10		ns	16
Output hold time from $\overline{CAS}$	tDOH	3		3		3		ns	
Row addr. set-up time	tASR	0		0		0		ns	
Row addr. hold time	tRAH	8		10		10		ns	
Column addr. set-up time	tASC	0		0		0		ns	15
Column addr. hold time	tCAH	8		10		12		ns	15
Column addr. to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Output buffer turn off delay from $\overline{WB}/\overline{WE}$	tWEZ	3	15	3	15	3	15	ns	7
Write command pulse width	tWPZ	10		10		10		ns	7
Write command hold time	tWCH	10		10		10		ns	
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5 Min	-5 Max	-6 Min	-6 Max	-7 Min	-7 Max	Unit	Notes
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		ns	18
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	8		10		12		ns	10
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	tCWD	35		40		45		ns	8,17
$\overline{RAS}$ to $\overline{WE}$ delay	tRWD	80		85		95		ns	8
Column addr. to $\overline{WE}$ delay time	tAWD	45		50		55		ns	8
$\overline{CAS}$ set-up time (CBR refresh)	tCSR	5		5		5		ns	19
$\overline{CAS}$ hold time (CBR refresh)	tCHR	10		10		10		ns	20
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		ns	
Access time from output enable	tOEA		15		15		20	ns	
Output enable to data input delay	tOED	10		15		15		ns	7
Output buffer turn-off delay from $\overline{OE}$	tOEZ	3	15	3	15	3	15	ns	
Output enable command hold time	tOEH	15		15		15		ns	
Data to $\overline{CAS}$ delay	tDZC	0		0		0		ns	
Data to output enable delay	tDZO	0		0		0		ns	
Refresh period (512 cycle)	tREF		8		8		8	ms	
$\overline{WB}$ set-up time	tWSR	0		0		0		ns	
$\overline{WB}$ hold time	tRWH	8		10		10		ns	
DSF set-up time referenced to $\overline{RAS}$	tFSR	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$	tRFH	8		10		10		ns	
DSF set-up time referenced to $\overline{CAS}$	tFSC	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	tCFH	8		10		15		ns	
Write per bit mask data set-up time	tMS	0		0		0		ns	
Write per bit mask data hold time	tMH	8		10		10		ns	
$\overline{DT}$ high set-up time	tTHS	0		0		0		ns	
$\overline{DT}$ high hold time	tTHH	8		10		10		ns	
$\overline{DT}$ low set-up time	tTLS	0		0		0		ns	
$\overline{DT}$ low hold time	tTLH	8		10		10		ns	
$\overline{DT}$ low hold referenced to $\overline{RAS}$ (RRT)	tRTH	45		50		60		ns	
$\overline{DT}$ low hold referenced to $\overline{CAS}$ (RRT)	tCTH	15		15		20		ns	
$\overline{DT}$ low hold refer. to column address (RRT)	tATH	20		20		25		ns	
$\overline{DT}$ precharge time	tTP	20		20		20		ns	
$\overline{RAS}$ to first SC delay (Read Transfer)	tRSD	50		60		70		ns	
$\overline{CAS}$ to first SC delay (Read Transfer)	tCSD	20		25		30		ns	
Col. Addr. to first SC delay (Read Transfer)	tASD	25		30		35		ns	
Last SC to $\overline{DT}$ lead time	tTSL	5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{DT}$ to first SC delay time (Read Transfer)	tTSD	10		10		10		ns	
Last SC to $\overline{RAS}$ set-up time	tSRS	20		20		20		ns	
SC cycle time	tSCC	18		18		20		ns	14
SC pulse width (SC high time)	tSC	5		5		7		ns	
SC precharge (SC low time)	tSCP	5		5		7		ns	
Access time from SC	tSCA		15		15		17	ns	4
Serial output hold time from SC	tSOH	3		3		5		ns	
Access time from $\overline{SE}$	tSEA		15		15		17	ns	4
$\overline{SE}$ pulse width	tSE	20		20		20		ns	
$\overline{SE}$ precharge time	tSEP	20		20		20		ns	
Serial output turn-off from $\overline{SE}$	tSEZ	0	15	0	15	0	15	ns	7
Split transfer set-up time	tSTS	20		20		25		ns	
Split transfer hold time	tSTH	20		20		25		ns	
SC-QSF delay time	tSQD		20		20		25	ns	
$\overline{DT}$-QSF delay time	tTQD		20		20		25	ns	
$\overline{RAS}$-QSF delay time	tRQD		65		70		75	ns	
$\overline{CAS}$-QSF delay time	tCQD		35		35		35	ns	
$\overline{DT}$ to $\overline{RAS}$ precharge time	tTRP	40		40		50		ns	
$\overline{DT}$ high pulse width	tOEP	5		5		5		ns	
$\overline{DT}$ high hold time from $\overline{CAS}$ high	tOEHC	5		5		5		ns	
$\overline{OE}$ to high set-up time	tOCH	5		5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$, 8 SC cycles before proper device operation is achieved. ($\overline{DT/OE}$ = High) If the internal refresh counter is used, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.
2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH (min) and VIL (max), and are assumed to be 2ns for all input signals.
   Input signal transition from 0V to 3V for AC timing.
3. RAM port outputs are measured with a load equivalent to 1 TTL load and 50pF.
   DOUT comparator level : VOH/VOL = 2.0V / 0.8V.
4. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
   DOUT comparator level : VOH/VOL = 2.0V / 0.8V.

5. Operation within the tRCD (max) limit insures that tRAC (max) can be met. The tRCD (max) is specified as a reference point only: If tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
6. Assumes that tRCD ≥ tRCD (max).
7. This parameters define the time at which the output achieves the open circuit condition and are not referenced to VOH or VOL.
8. tWCS, tRWD, tCWD, tCPWD and tAWD are nonrestrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS ≥ tWCS (min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If tCWD ≥ tCWD(min), tRWD ≥ tRWD(min), tCPWD ≥ tCPWD(min), and tAWD ≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.

NOTES

9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

11. Operation within the t_{RAD} (max) limit insured that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

12. Power must be applied to the $\overline{RAS}$ and $\overline{DT/OE}$ input signal to pull them high before or at the same time as the V_{CC} supply is turned on.

After power-up, initial status of chip is described below.

Pin or Register	Status
QSF	Hi-Z
Color Register	Don t Care
Write Mask Register	Don t Care
Tap Pointer	Invalid
Stop Register	Default Case
Wi/DQi	Hi-Z
SAM Port	Hi-Z
SQi	Hi-Z

13. Recommended operating input condition :
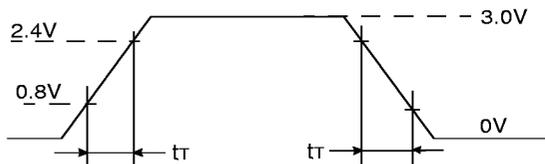
Input pulse levels are from 0.0V to 3.0Volts.
All timing measurements are referenced from V_{IL} (max) and V_{IH} (min) with transition time = 2ns

14. Assume t_T = 3ns.

15. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge

16. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

17. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

18. t_{CWL} is specified from $\overline{WB/WE}$ falling edge to the earlier $\overline{CAS}$ rising edge.
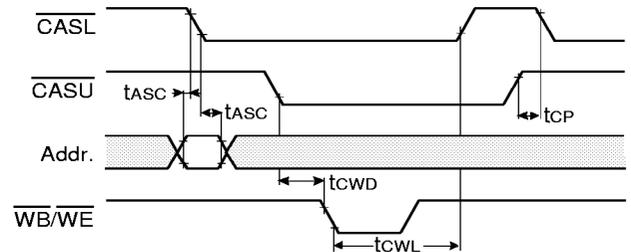
19. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

20. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.
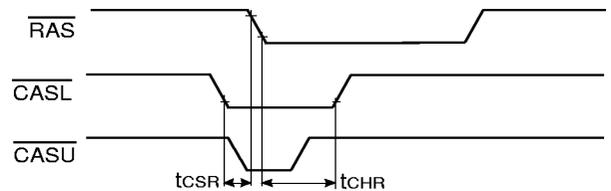
21. $t_{ASC} \geq t_{CP}$(min), at Normal cycle, Assum t_T=2.0ns

22. $t_{ASC} < t_{CP}$ (min), at Normal cycle or any condition at Block write cycle, Assume t_T=2ns

DEVICE OPERATIONS

The KM4216C258 contains 4,194,304 memory locations.
Eighteen address bits are required to address a particular 16 bit word in the memory array. Since the KM4216C258 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe (RAS), the column address strobe (CAS) and the valid row and column address inputs.

Operation of the KM4216C258 begins by strobing in a valid row address with RAS while CAS remains high. Then the address on the 9 address input pins are changed from a row address to a column address, and are strobed by CAS.

This is the beginning of any KM4216C/V256 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationship. The cycle is terminated when both RAS and CAS have returned to the high state. Another cycle can be initiated after RAS remains high long enough to satisfy the RAS precharge time(tRP) requirement.

RAS and CAS Timing

The minimum RAS and CAS pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing RAS low, it must not be aborted prior to satisfying the minimum RAS and CAS pulse widths. In addition, a new cycle must not begin until the minimum RAS precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM4216C258 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirement, loss of data integrity can occur.

RAM Read

A RAM read cycle is achieved by maintaining WB/WE high during a RAS / CAS cycle. The access time is normally specified with respect to the falling edge of RAS. But the access time also depends on the falling edge of CAS and on the valid column address transition.

If CAS goes low before tRCD(max) and if the column address is valid before tRAD (max) then the access time to valid data is specified by tRAC. However, If CAS goes low after tRCD(max) or the column address becomes valid after tRAD(max), access is specified by tCAC or tAA.

The KM4216C258 has common data I/O pins. The DT/OE has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, DT/OE must be low for the period of time defined by tOEA.

Extended Data Out

In the conventional RAM Read cycle, Dout buffer is designed to make turn-off by the rising edge of CAS. the KM4216C258 offers an accelerated Fast Page Mode cycle by eliminating output disable from CAS high. This is called "Extended Data Output (or Hyper Page) mode". Data outputs are disabled at WB/WE = Low, DT/OE = High and tOFF time after RAS and CAS are high The tOFF time is referenced from rising edge of RAS or CAS, whichever occurs later (see Figure 1). What the output buffer is disabling during DT/OE = high is to use bank selection in the frame buffer memory using common I/O line, Read, Write and Read-modify-write cycles are available during the extended data out mode.
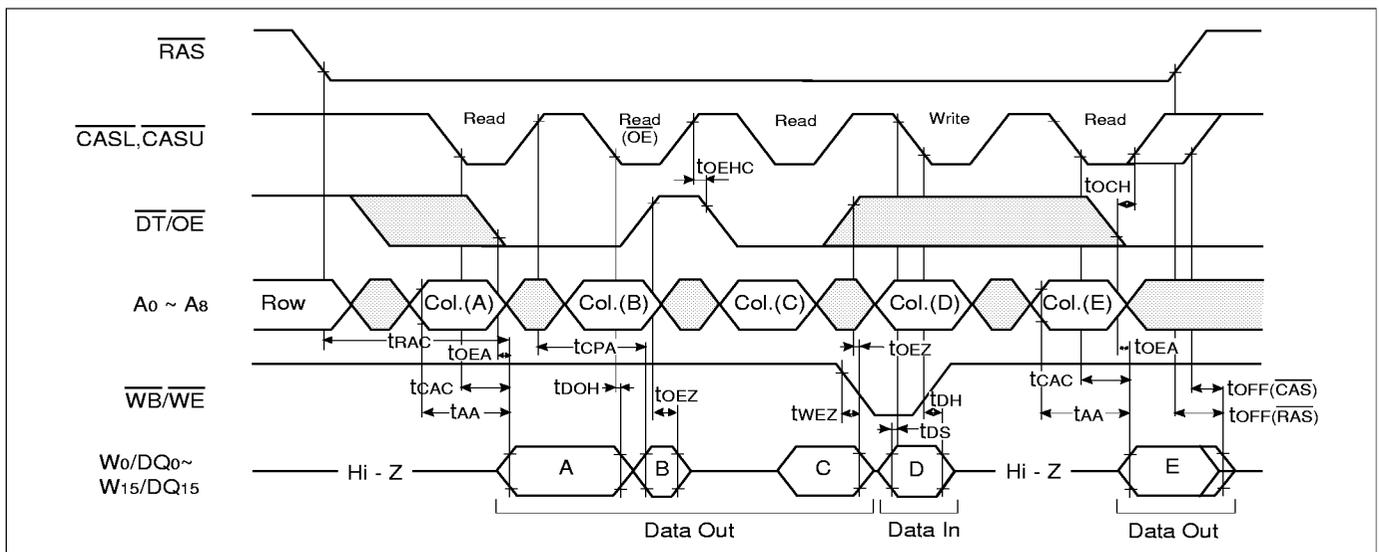

Figure 1. Extended Data Output Example

SAMSUNG ELECTRONICS

DEVICE OPERATIONS(Continued)

2 CAS Byte/Word Read/ Write Operation
The KM4216C258 has 2 CAS control pin, CASL and CASU, and offers asynchronous Read/Write operation with lower byte (W0/DQ0 ~ W7/DQ7) and upper byte (W8/DQ8 ~ W15/DQ15). This is called 2CAS Byte/Word Read/Write operation. This operation can be performed in any RAM Read in RAM Write, Block Write, Load Mask Register, and Load Color Register.

New Masked Write Per Bit
The New Masked Write per Bit cycle is achieved by maintaining CAS high and WB/WE and DSF low at the falling edge of RAS. The mask data on the W0/DQ0 ~ W15/DQ15 pins are latched into the write mask register at the falling edge of RAS.   When the mask data is low, writing is inhibited into the RAM and the mask data is high, data is written into the RAM. The mask data is valid for only one cycle. Mask Data must be provided in every write cycle that a masking operation is desired.
The Early Write cycle is achieved by WB/WE low before CAS falling and the Late Write cycle is achieved by WB/WE low after CAS falling. During the Early or Late Write cycle, input data through W0/DQ0 ~ W15/DQ15 must keep the set-up and hold time at the falling edge of CAS or WB/WE .
If WB/WE is high at the falling edge of RAS, no masking operation is performed (see Figure 2,3).

And if CASL is high during WB/WE low, write operation of lower byte does not perform and if CASU is high, also write operation of upper byte does not execute.

Load Mask Register (LMR)
The Load Mask Register operation loads the data present on the Wi/DQi pins into the Mask Data Register at the falling edge of CAS or WB/WE. The LMR cycle is performed if DSF high, WB/WE high at the RAS falling edge and DSF low at the CAS falling edge. If an LMR is done, the KM4216C258 are set to Old masked write mode.

Old Masked Write Per Bit
This mode is enabled through the Load Mask Register (LMR) cycle. If an LMR is done, all Masked Write are Old masked Write Per Bit and the I/O mask data will be provided by the Mask Data Register (see Figure 4).
The mask data is applied in the same manner as in New Masked Write Per Bit mode. Mask Data Register s content is changed by the another LMR, To reset the device back to the New Masked Write Mode, CBRR(CBR Refresh with option reset) cycle must be performed. After power-up, the KM4216C258 initializes in the New Masked Write Mode.
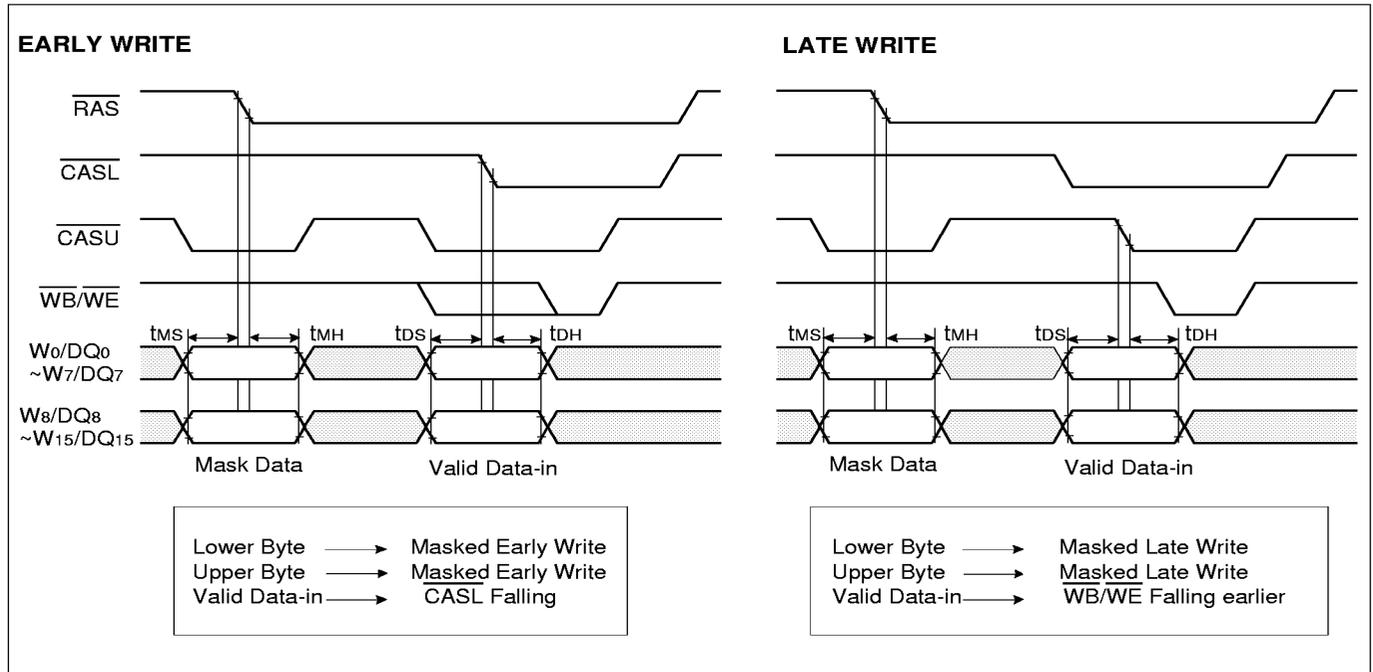

Figure 2. Byte Write and New Masked Write Cycle Example1. (Early Write & Late Write)
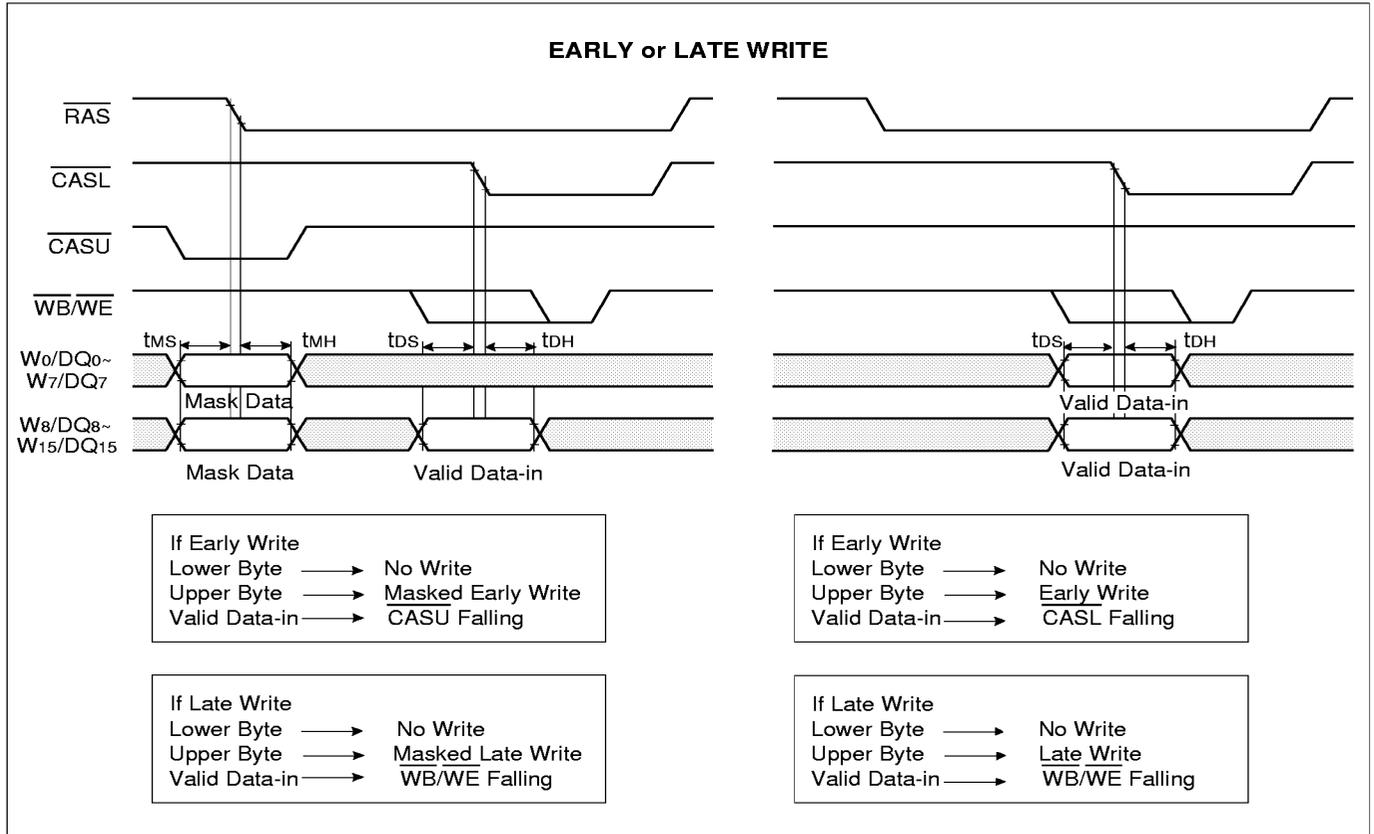
DEVICE OPERATIONS(Continued)

EARLY or LATE WRITE

Figure 3. Byte Write and New Masked Write Cycle Example2.

Fast Page Mode

The KM4216C258 has Fast Page Mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. In this cycle, read, write, read-modify-write, and block write cycles can be mixed in any order. In one $\overline{RAS}$ cycle, 512 word memory cells of the same row address can be accessed. While $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Load Color Register (LCR)

A Load Color Register cycle is performed by keeping DSF high on the both the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Color data is loaded on the falling edge of $\overline{CAS}$ (early write) or $\overline{WE}$ (late write) via the W0/DQ0 ~ W7/DQ7 (lower byte), W8/DQ8 ~ W15/DQ15 (upper byte) pins. This data is used in Block Write cycles and remains unchanged until the next Load Color Register cycle.

DEVICE OPERATIONS(Continued)
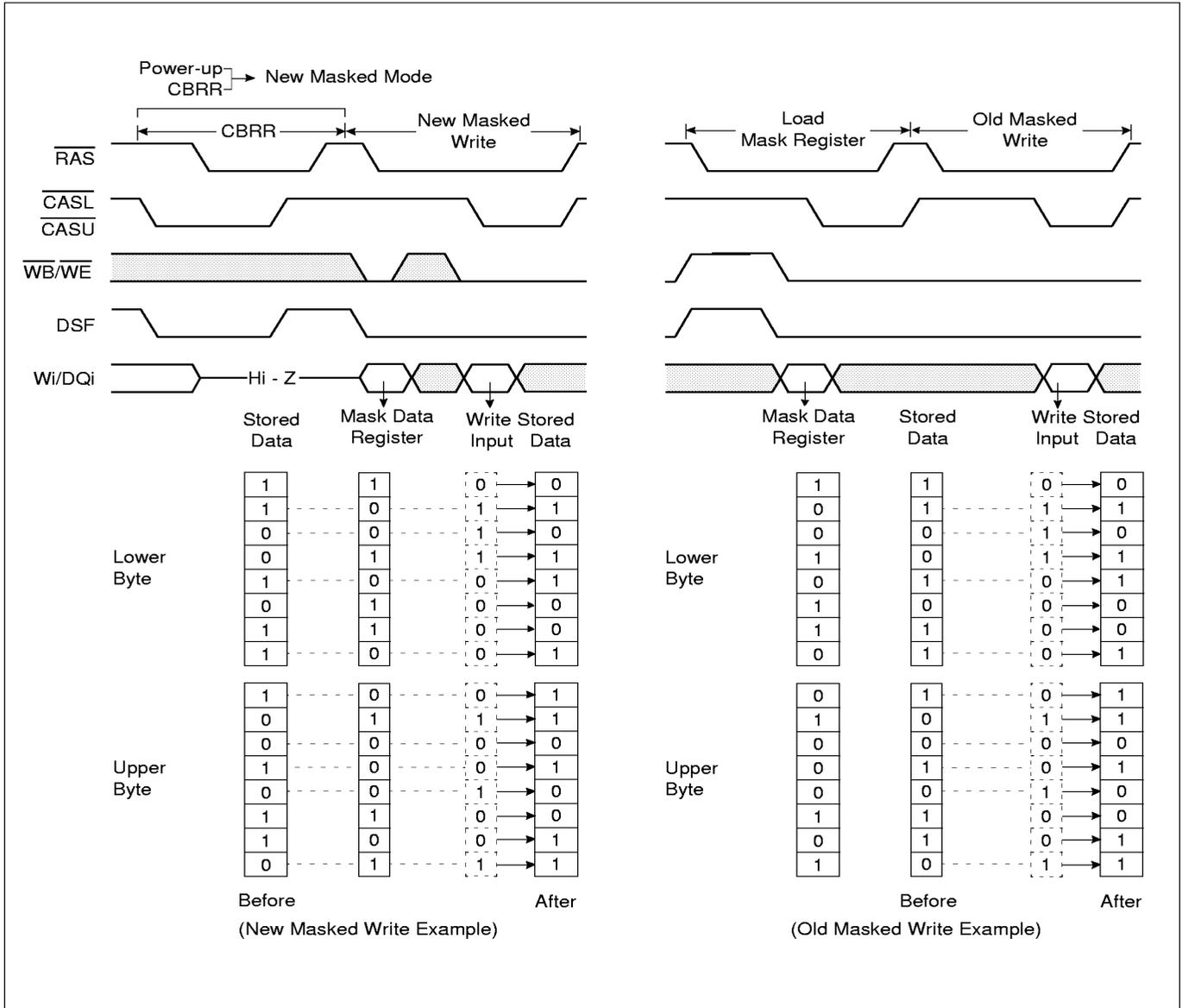
Figure 4. New Masked Write Cycle and Old Masked Write Cycle Example

DEVICE OPERATIONS(Continued)

Block Write

In a Block Write cycle 8 adjacent column locations can be written simultaneously with the same data, resulting in fast screen fills of the same color.

First, the internal 16 bit Color Register must be loaded with the data to be written by performing a Load Color Register(LCR) cycle.

When a Block write cycle is performed, each bit of the Color Register is written into 8 adjacent locations of the same row of each corresponding bit plane(16). This results in a total of 128bits being written in a single Block Write cycle compared to 16-bits in a normal Write cycle.

The Block Write cycle is performed if DSF is low at the falling edge of the $\overline{RAS}$ and high at the falling edge of $\overline{CAS}$.

Column Mask   I/O Mask

1 Row of 512

	$\overline{RAS}$ ↘
W0/DQ0 ~ 7	Lower Block I/O Mask
W8/DQ8 ~ 15	Upper Block I/O Mask

	$\overline{CAS}$ ↘
A0 ~ A2	Don't Care
W0/DQ0 ~ 7	Lower Block Column Select
W8/DQ8 ~ 15	Upper Block Column Select

A2 ~ A0	Lower	Upper	Column Mask	
0 0 0	W0/DQ0	W8/DQ8	DQi = 1	Column Enable
0 0 1	W1/DQ1	W9/DQ9		
0 1 0	W2/DQ2	W10/DQ10		
0 1 1	W3/DQ3	W11/DQ11		
1 0 0	W4/DQ4	W12/DQ12	DQi = 0	Column Disable
1 0 1	W5/DQ5	W13/DQ13		
1 1 0	W6/DQ6	W14/DQ14		
1 1 1	W7/DQ7	W15/DQ15		

Figure 5. Block Write Scheme

DEVICE OPERATIONS(Continued)

Address Lines : The row address is latched on the falling edge of $\overline{RAS}$. Since 8 columns are being written at a time, the minimum increment required for the column address is eight. Therefore, when the column address is latched at the falling edge of $\overline{CAS}$, the 3 LSBs, $A_0 \sim A_2$ are ignored and only bits($A_3 \sim A_8$) are used to define the location of the first bit out of the eight to be written.

Data Lines : On the falling edge of $\overline{CAS}$, the data on the $W_0/DQ_0 \sim W_{15}/DQ_{15}$ pins provide column mask data. That is, for each of the eight bits in all 16-bit planes, writing of Color Register contents can be inhibited. For example, If $W_0/DQ_0 = 1$ and $W_1/DQ_1 = 0$, then the Color Register contents will be written into the first bit out of the 8, but the second remains unchanged.

Fig. 5 shows the correspondence of each data line to the column mask bits.

A masked Block Write cycle identical to a New/Old Masked Write-per-bit cycle except that each of the 16-bit planes being masked is operating on 8 column locations instead of one.

To perform a Masked Block Write cycle, both DSF and $\overline{WB/WE}$ must be low at the falling edge of $\overline{RAS}$. DSF must be high at the falling edge of $\overline{CAS}$. In new mask mode, Mask data is latched into the device via the $W_0/DQ_0 \sim W_{15}/DQ_{15}$ pins at the falling edge of $\overline{RAS}$ and needs to be re-entered for every new $\overline{RAS}$ cycle. And $\overline{WB/WE}$ must be low, DSF must be high on the falling edge of $\overline{CAS}$. In Old Mask Mode, I/O mask data will be provided by the Mask Data Register.
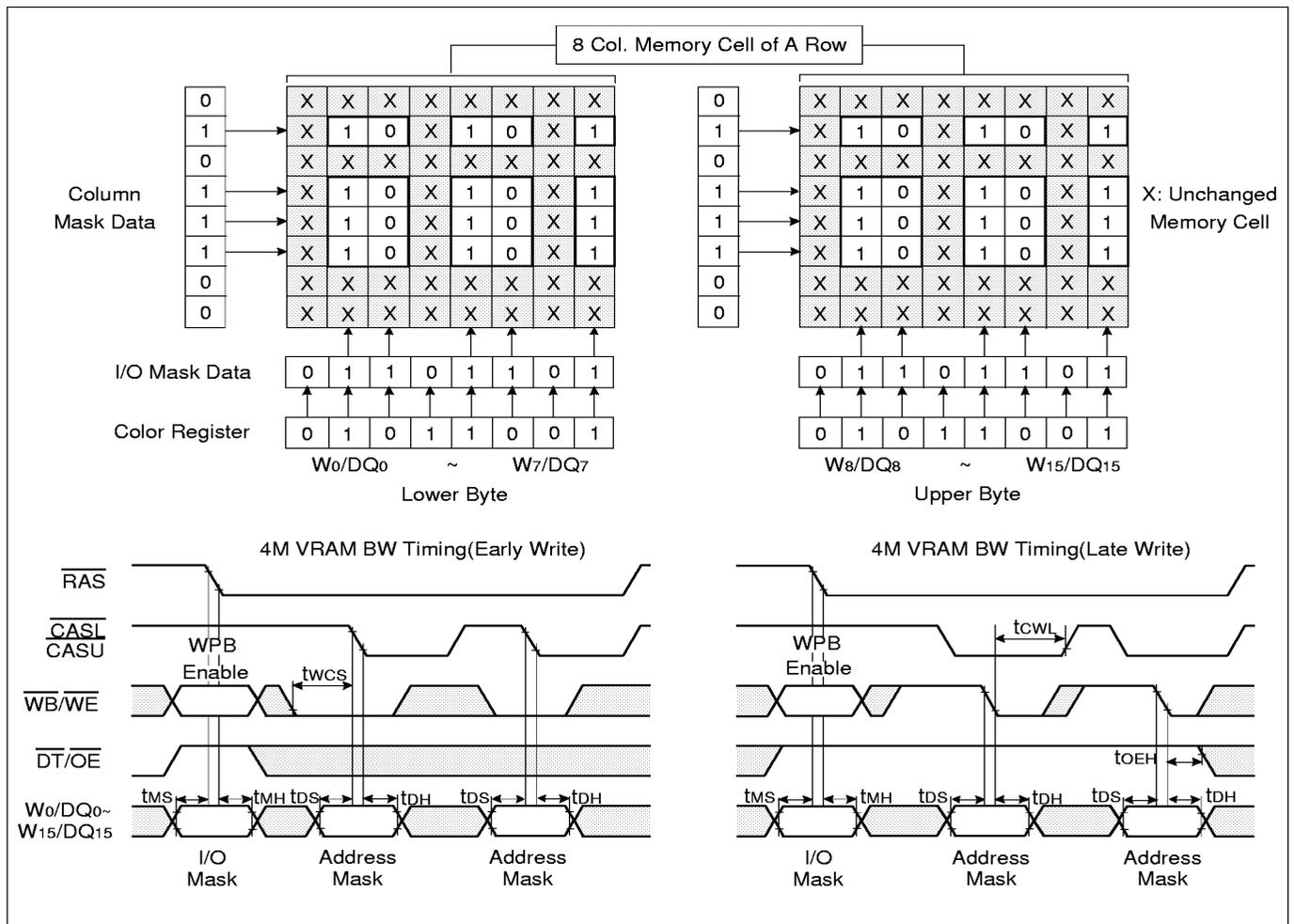
Figure 6. Block Write Example and Timing

DEVICE OPERATIONS(Continued)

Data Output

The KM4216C258 has three state output buffer controlled by $\overline{DT/OE}$ and $\overline{CAS/RAS}$. If $\overline{DT/OE}$ is high when $\overline{CAS}$ and $\overline{RAS}$ low, the output state is high impedance (High-z). In any cycle, the output goes low impedance state after tCLZ of the first $\overline{CAS}$ falling edge. Invalid data may be present at the output during the time after tCLZ and the valid data appears at the output. The timing parameter tRAC, tCAC and tAA specify when the valid data will be present at the output.

Refresh

The data in the KM4216C258 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM port refreshes the 8192 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh

This is the most common method for performing refresh. it is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address, (A0 ~ A8).

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh

The KM4216C258 has $\overline{CAS}$-before-$\overline{RAS}$ on chip refresh capability that eliminates the need for external refresh address. If $\overline{CAS}$ is held low for the specified set up time(tCSR) before $\overline{RAS}$ goes low, the on chip refresh circuitry is enabled.
An internal refresh operation occurs automatically. The refresh address is supplied by the on chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

The KM4216C258 has 3 type $\overline{CAS}$-before-$\overline{RAS}$ refresh operations CBRR, CBRN, CBRS
CBRR (CBR Refresh with option reset) is set if DSF low at the $\overline{RAS}$ falling edge. This mode initiates to change from old masked write to new masked write cycle, and reset stop register to default values.
CBRN (CBR refresh without reset) is set if DSF high when $\overline{WB/WE}$ is high at the falling edge of $\overline{RAS}$ and simply does only refresh operation.
CBRS (CBR Refresh with stop register set) cycle is set if DSF high when $\overline{WB/WE}$ is low and this mode is to set stop register s value.

Hidden Refresh :

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM4216C258 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle.
The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods :

It is also possible to refresh the KM4216C258 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

DEVICE OPERATIONS(Continued)

Table.1 Truth Table for Transfer Operation

* : Don t care

RAS Falling Edge					Function	Transfer Direction	Transfer Data Bit
CAS	DT/OE	WB/WE	DSF	SE			
H	L	H	L	*	Read Transfer	RAM → SAM	512 x 16
H	L	H	H	*	Split Read Transfer	RAM → SAM	256 x 16

Transfer Operation

Transfer operation is initiated when $\overline{DT/OE}$ is low at the falling edge of $\overline{RAS}$. The state of DSF when $\overline{RAS}$ goes low is used to select between normal transfer and split transfer cycle. Each of the transfer cycle is described in the truth table for transfer operation (Table 1).

Read Transfer (RT)

The Read Transfer operation is set if $\overline{DT/OE}$ is low, $\overline{WB/WE}$ is high and DSF low at the falling edge of $\overline{RAS}$. The row address bits in the read transfer cycle indicate which sixteen 512bit DRAM row portions are transferred to the sixteen SAM data register portions. The column address bits indicate the start address of the SAM Registers when SAM data read operation is performed. If MSB of column address is low during Read transfer operation, the QSF state will be set low level and this indicates the start address of SAM register is present at lower half of SAM port. (If A8 is high, QSF will be high and means the start address is in upper half) Read Transfer may be accomplished in two ways. If the transfer is to be synchronized with the SC. $\overline{DT/OE}$ is taken high after $\overline{CAS}$ goes low. This is usually called "Real Time Read Transfer". Note that the rising edge of $\overline{DT/OE}$ must be synchronized with the rising edge of SC(tTSL/tTSD) to retain the continuity of serial read data output. If the transfer does not have to be synchronized with SC, $\overline{DT/OE}$ may go high before $\overline{CAS}$ goes low and the actual data transfer will be timed internally.

Split Read Transfer (SRT)

In a graphic system, if data has to be transferred from DRAM to SAM while in the middle of a display line, the only way to do this seamlessly is performed by a Real Time Read Transfer cycle. However, this cycle has many critical timing restriction (between SC, $\overline{DT/OE}$, $\overline{RAS}$ and $\overline{CAS}$) because the transfer has to occur at the first rising edge of $\overline{DT/OE}$ The split read transfer(SRT) cycle eliminates the need for this critical transfer timing, thereby simplifying system design. This is accomplished by dividing the SAM port into 2 halves of 256 bits each. A Split Read Transfer loads only the lower or upper half. While data is being serially read from one half of the SAM Register, new RAM data can be transferred to the other half. Since transfer timing is controlled internally, there is no timing restriction between $\overline{DT/OE}$ and $\overline{RAS}$, $\overline{CAS}$, SC.

A normal Read Transfer cycle must be executed before performing a Split Read Transfer to set the state of QSF. A Split Read Transfer cycle is initiated by keeping DSF and $\overline{WB/WE}$ high and $\overline{DT/OE}$ low at the falling edge of $\overline{RAS}$.

Address : The row address is latched on the falling edge of $\overline{RAS}$. The column address defined by (A0 ~ A7) defines the starting address of the SAM port from which data will begin shifting out. Column address pin A8 is a "Don t Care."

The QSF pin indicates which SAM half is shifting out serial data (0 = Lower, 1 = Upper). A Split Read Transfer will load data into the other half. The state of the QSF output changes when the SAM address counter reaches a split SAM boundary (e.g. 255th or 511th bit).

Examples of SRT application are shown in Fig. 7 through Fig.10.

The normal usage of Split Read Transfer cycle is described in Fig.7. When Read Transfer is executed, data from X1 row address is fully transferred to the SAM port and serial Read is started from 0 (Tap address).

If SRT is performed while data is being serially read from lower half SAM, data from X2 row address is transferred to upper half SAM. The Tap address of SRT is loaded after the boundary location of lower half SAM (255th SC) is accessed and the QSF state is changed into high level at the rising edge of 255th SC. Note that in this case "256+Y0" Tap address instead of "Y0" is loaded.

The another example of SRT cycle is described in Fig.8. When Serial Read is performed after executing RT and SRT in succession, the data accessed by first SC is the starting address given by RT Tap address. Serial data access from the starting address given by SRT cycle is performed after the data of RT to lower boundary (255th SC) is completed. Fig. 9 and 10 are the example of abnormal SRT cycle.

DEVICE OPERATIONS(Continued)

If SRT1 and SRT2 are performed in succession before access-ing the boundary like Fig. 9, the data transferred by SRT2 overwrites the data transferred by SRT1, so that data followed by SRT2 will be remain in the upper half SAM. The Serial Read after lower boundary 255th SC is started from the starting address given by SRT2 cycle. The Fig. 10 indicates that SRT cycle is not performed until Serial Read is completed to the boundary location 511.

In this case, the internal serial counter is designed to designate "0" address after boundary 511, therefore accessed data from 0 address corresponds to the old data transferred by RT. Note that there is not allowed period of SRT cycle. Since a SRT cycle must be ended before tSTH and started after tSTS, a split transfer is not allowed during tSTH + tSTS (see Fig. 11)

A Split Read Transfer does not change the direction of the SAM I/O port.
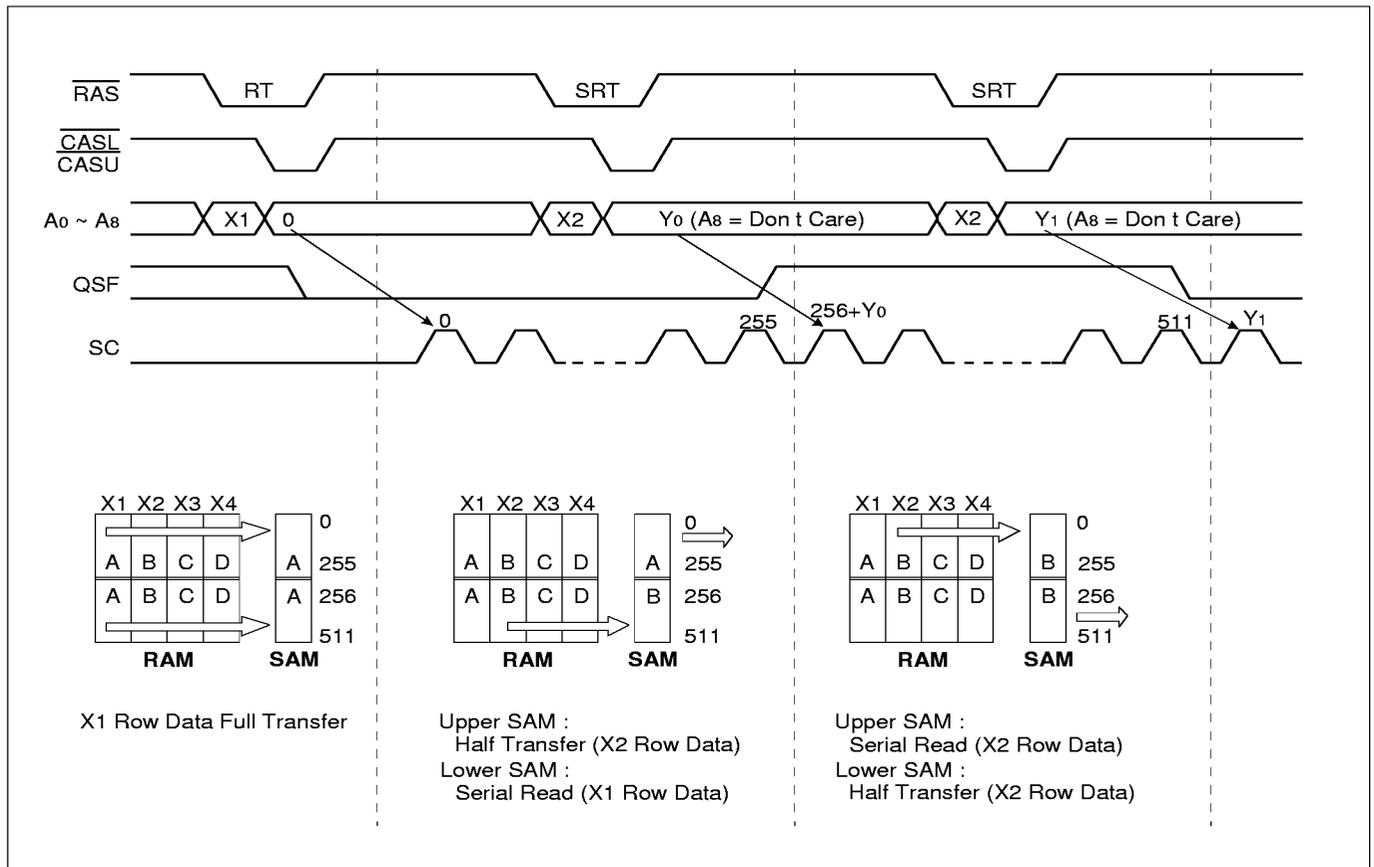
Figure 7. Split Read Transfer Normal Usage

DEVICE OPERATIONS(Continued)
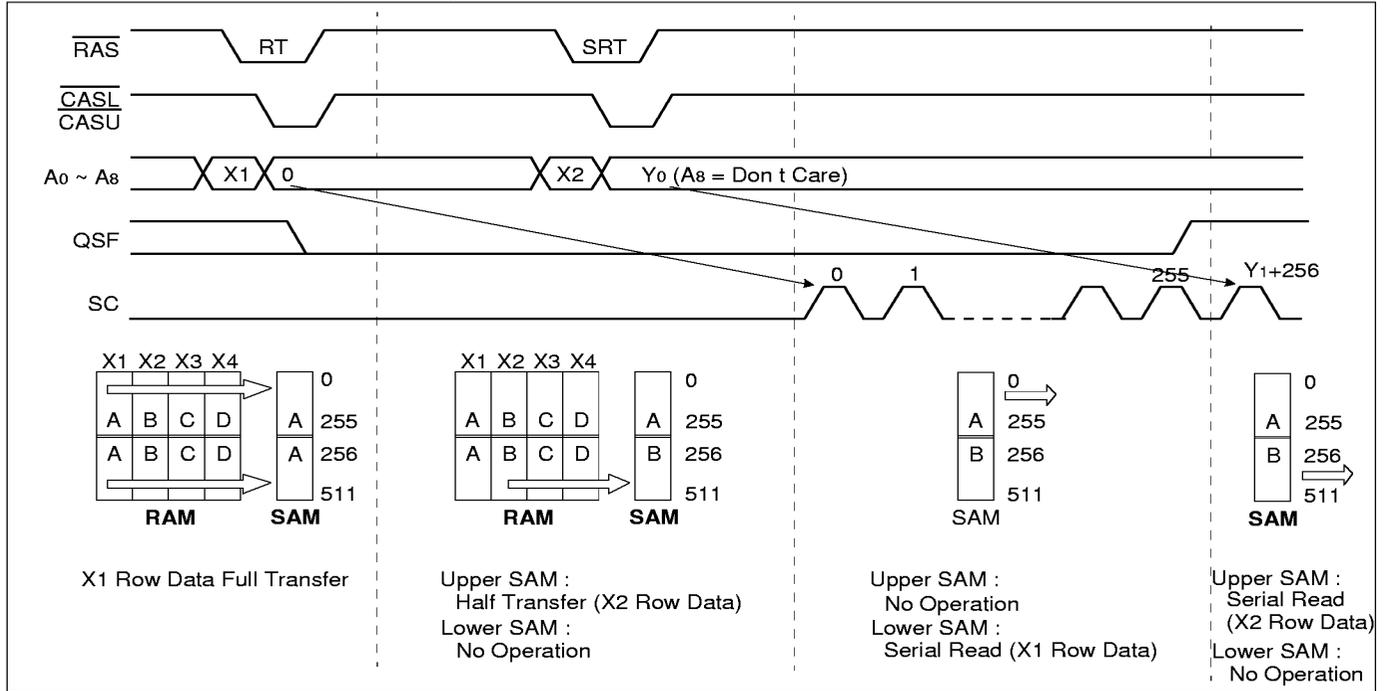
Figure 8. Split Read Transfer Normal Usage
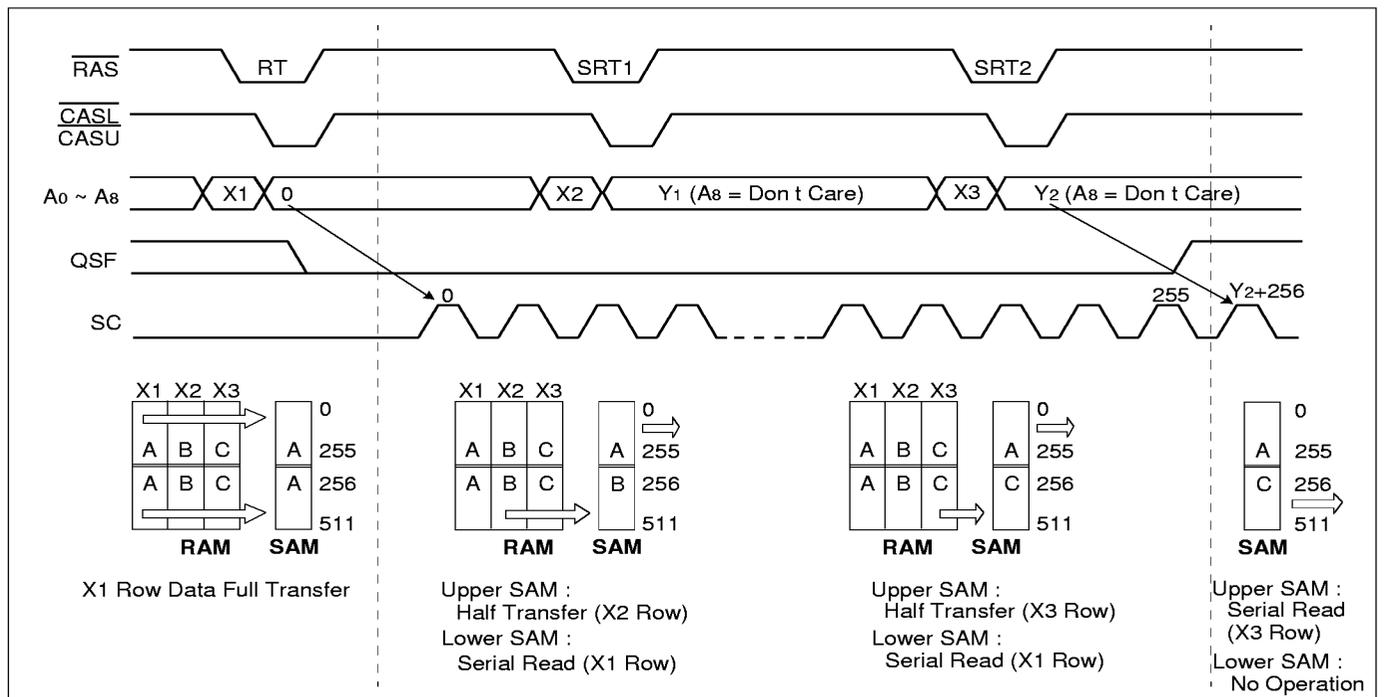
Figure 9. Split Read Transfer Abnormal Usage (Case 1)

DEVICE OPERATIONS(Continued)
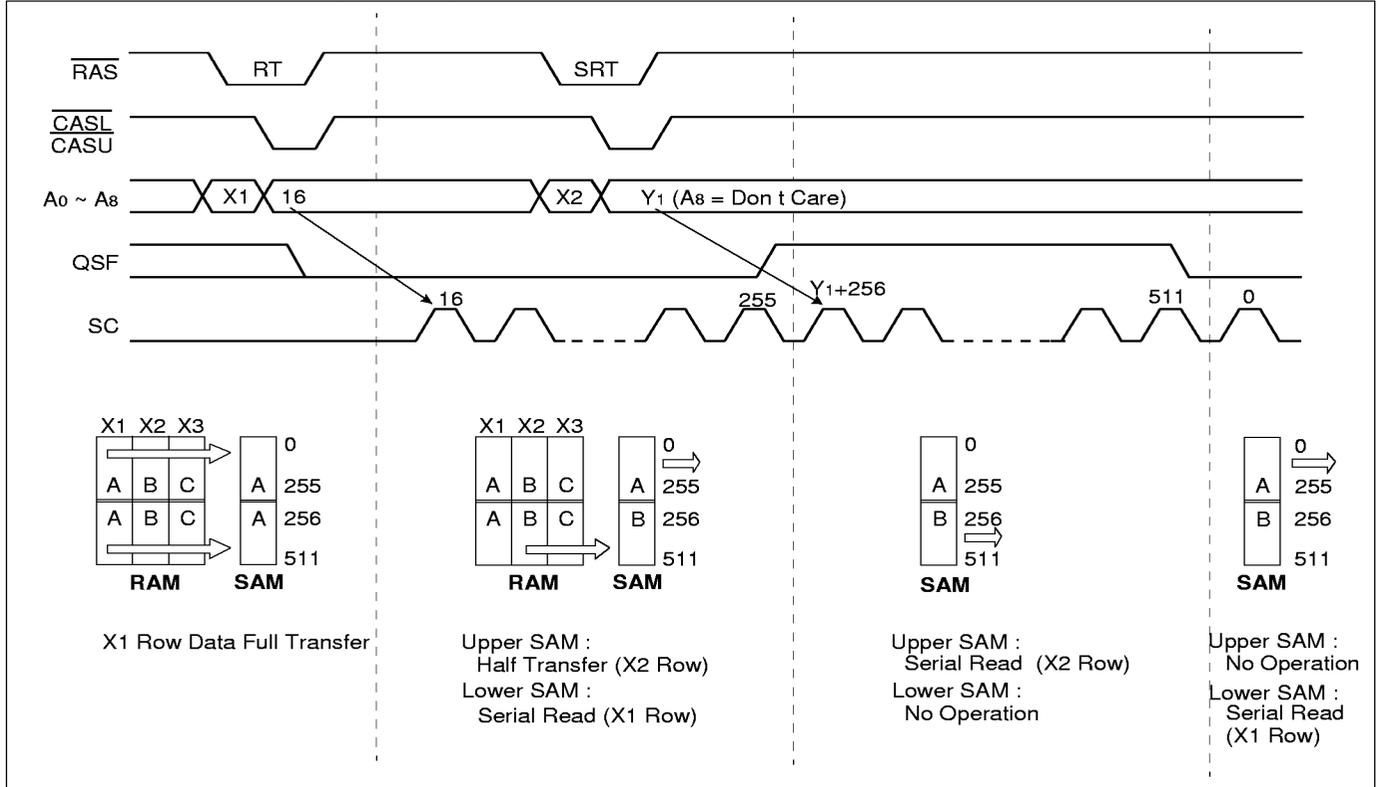
Figure 10. Split Read Transfer Abnormal Usage (Case 2)
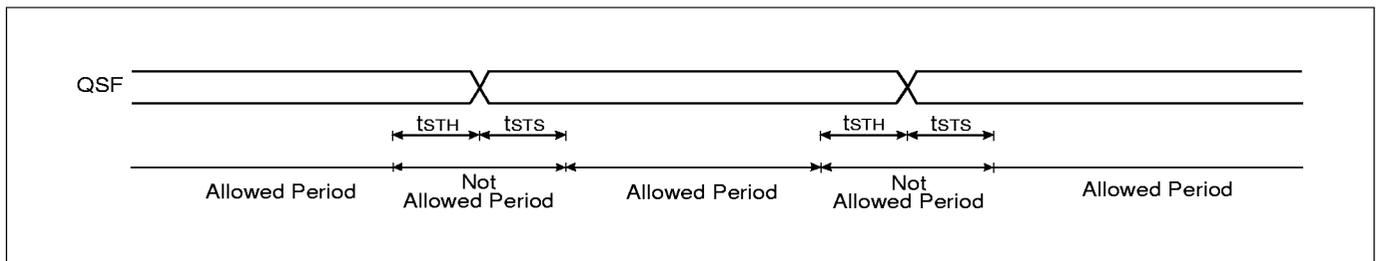
Figure 11. Split Transfer Cycle Limitation Period

DEVICE OPERATIONS(Continued)

Programmable Split SAM

In split SAM mode, SAM is divided into the lower half and the upper half, After the last address of each half SAM (255 or 511) is accessed, the access will be changed one half of the SAM to the other half (at the loaded Tap address). This last address is called stop point.

The KM4216C258 offers user-programmable Stop Points. The Stop Points and size of the resulting partitions are shown in Table 2. The Stop Point is set by performing CBRS cycle. The CBRS cycle s condition is $\overline{WB/WE}$ low, DSF high at the falling edge of $\overline{RAS}$ in CBR cycle and the Stop Point is determined by row address entering at this time.

The Stop Point will not become valid until a SRT cycle is done. The Stop Point does not effect to SAM in normal RT, RRT cycle. In Figure 12. programmable split SAM operation is shown. if a SRT cycle was done before the partition boundary (383), the access will jump to the TAP address (70) of the next half. Otherwise, the access will continue in the same half until a SRT occurs at the SAM half boundary (255, 511). Note that the Stop Point may be changed at any time by performing another CBRS, and New Stop Point will not be valid until a SRT is performed.

To reset Stop Point, CBRR cycle must be performed. CBRR is a CBR cycle with DSF low at the falling edge of $\overline{RAS}$
The CBRR will take effect immediately ; it does not require a SRT to become active valid.

Table. 2 Stop Point Setting Address

Stop Register = Store The Address of Serial Access Use on the Split Transfer Cycle Stop Pointer Set ⟶ CBRS Cycle							
Number Stop Points /Half	Partition	Stop Point Setting Address					
		A8	A7	A6	A5	A4	A3~A0
1	(1x256)x2	X	1	1	1	1	X
2	(2x128)x2	X	0	1	1	1	X
4	(4x64)x2	X	0	0	1	1	X
8	(8x32)x2	X	0	0	0	1	X
16	(16x16)x2	X	0	0	0	0	X

*Other Case = Inhibit, X =don t care.
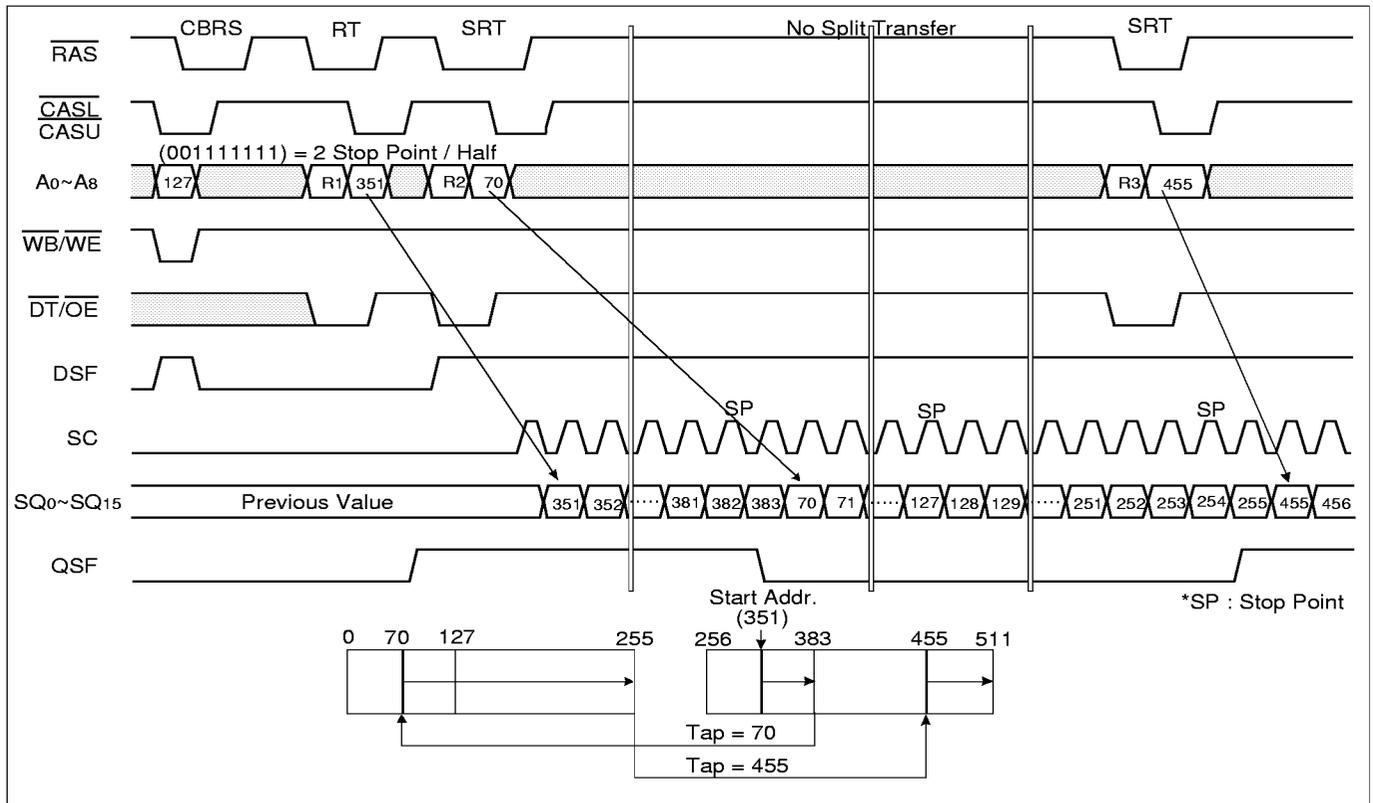
Figure 12. Programmable Split SAM Operation

TIMING DIAGRAMS

READ CYCLE

FAST PAGE MODE READ CYCLE (Extended Data Out)

Don't care

SAMSUNG
ELECTRONICS
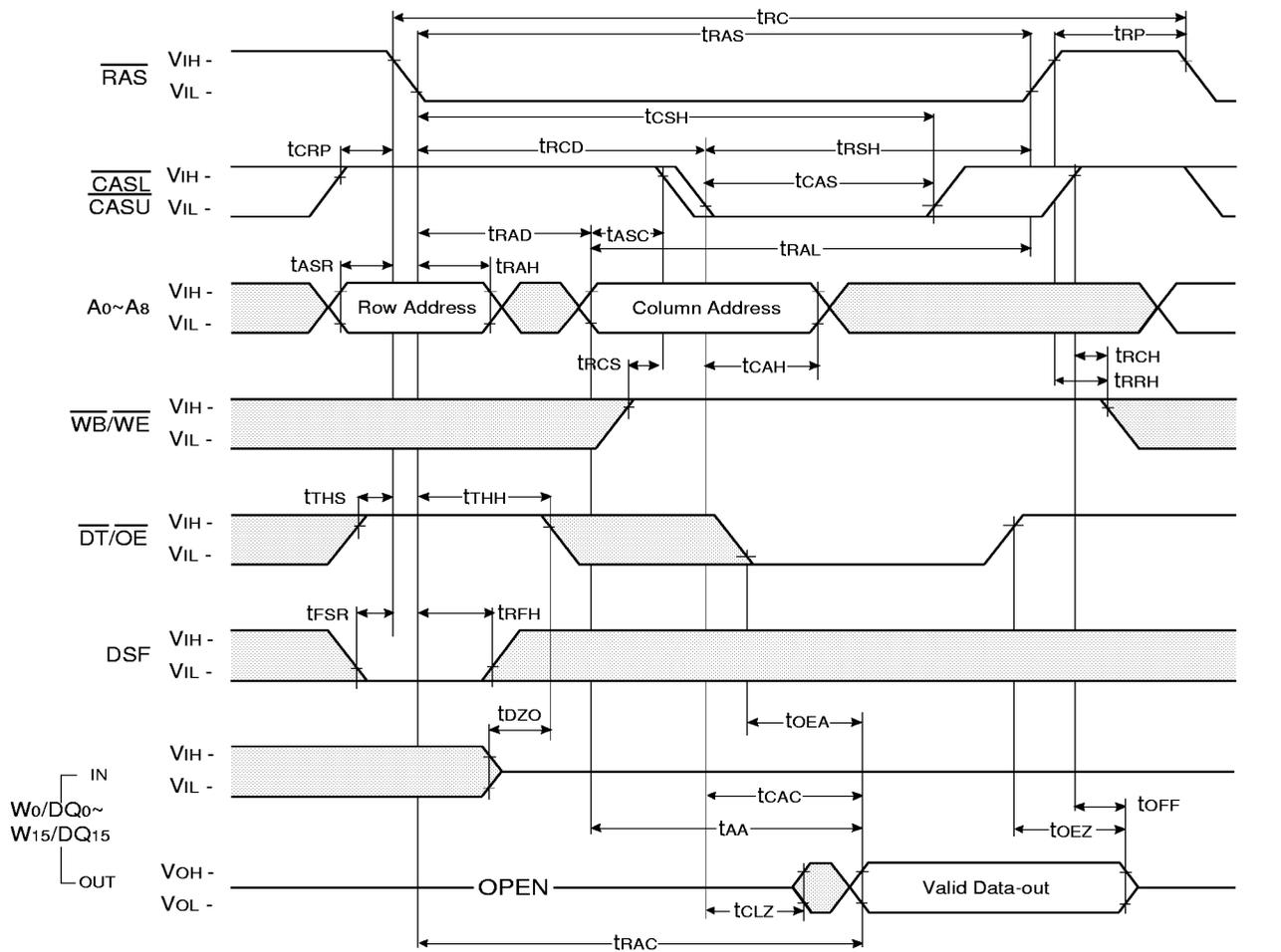
TURTH TABLE FOR WRITE CYCLE (1)

FUNCTION	$\overline{RAS}$ ⬎			$\overline{CAS}$ ⬎	$\overline{CAS}$ ⬎ or $\overline{WB}/\overline{WE}$ ⬎
	*1 $\overline{WB}/\overline{WE}$	*2 DSF	*3 Wi/DQi(4) (New Mask)	*4 DSF	*5 Wi/DQi
Normal Write	1	0	X	0	Write Data
Masked Write	0	0	Write Mask	0	Masked Write Data
Block Write (No I/O Mask)(4)	1	0	X	1	Column Mask
Masked Block Write(4)	0	0	Write Mask	1	Column Mask
Load Mask Data Register(2)	1	1	X	0	Write Mask Data
Load Color Register	1	1	X	1	Color Data

Note :

1) Reference truth table to determine the input signal states of *1, *2, *3, *4, and *5 for the write cycle timing diagram, on the following page.
2) Old Mask data load
3) Function table for Old Mask and New Mask

IF		*1 $\overline{WB}/\overline{WE}$	*3 Wi/DQi	Note
LMR Cycle Executed	YES	0	X	Write using mask register data (Old Mask Data)
		1	X	Non Masked Write
	NO	0	Mask	Write using New Mask Data Wi/DQi=0 Write Disable Wi/DQi=1 Write Enable
		1	X	Non Masked Write

X : Don t care

4) Function Table for Block Write Column Mask

| Column Address A_2 A_1 A_0			*5 Lower Byte	Upper Byte	IF Wi/DQi=0	Wi/DQi=1
0	0	0	W_0/DQ_0	W_8/DQ_8		
0	0	1	W_1/DQ_1	W_9/DQ_9		
0	1	0	W_2/DQ_2	W_{10}/DQ_{10}		Color Register Data
0	1	1	W_3/DQ_3	W_{11}/DQ_{11}	No Change the	is Written to the
1	0	0	W_4/DQ_4	W_{12}/DQ_{12}	Internal Data	Corresponding Column
1	0	1	W_5/DQ_5	W_{13}/DQ_{13}		Address Location
1	1	0	W_6/DQ_6	W_{14}/DQ_{14}		
1	1	1	W_7/DQ_7	W_{15}/DQ_{15}		

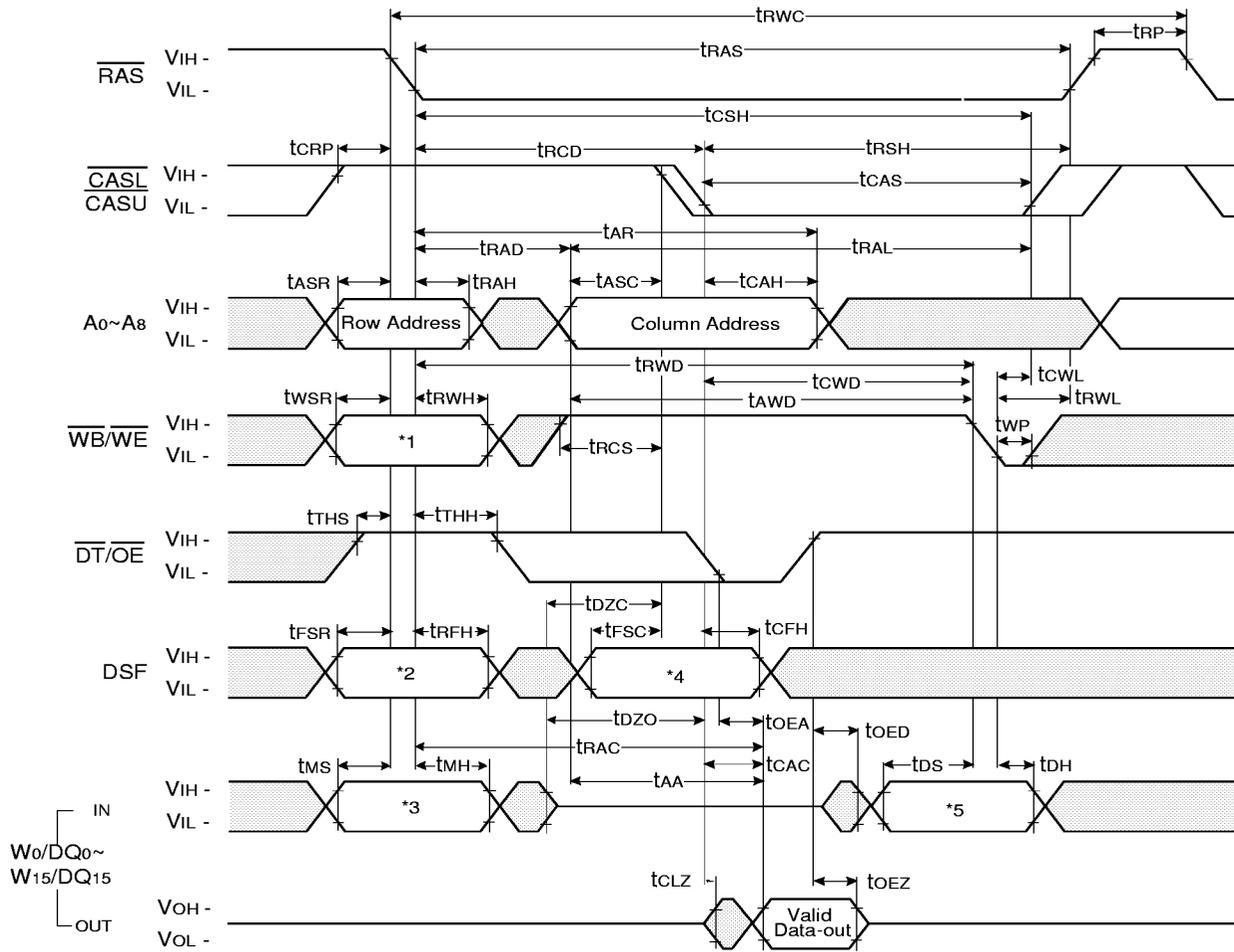## EARLY WRITE CYCLE

Note : In Block Write cycle, only Column Address A3 ~ A8 are used.

Don t care

LATE WRITE CYCLE
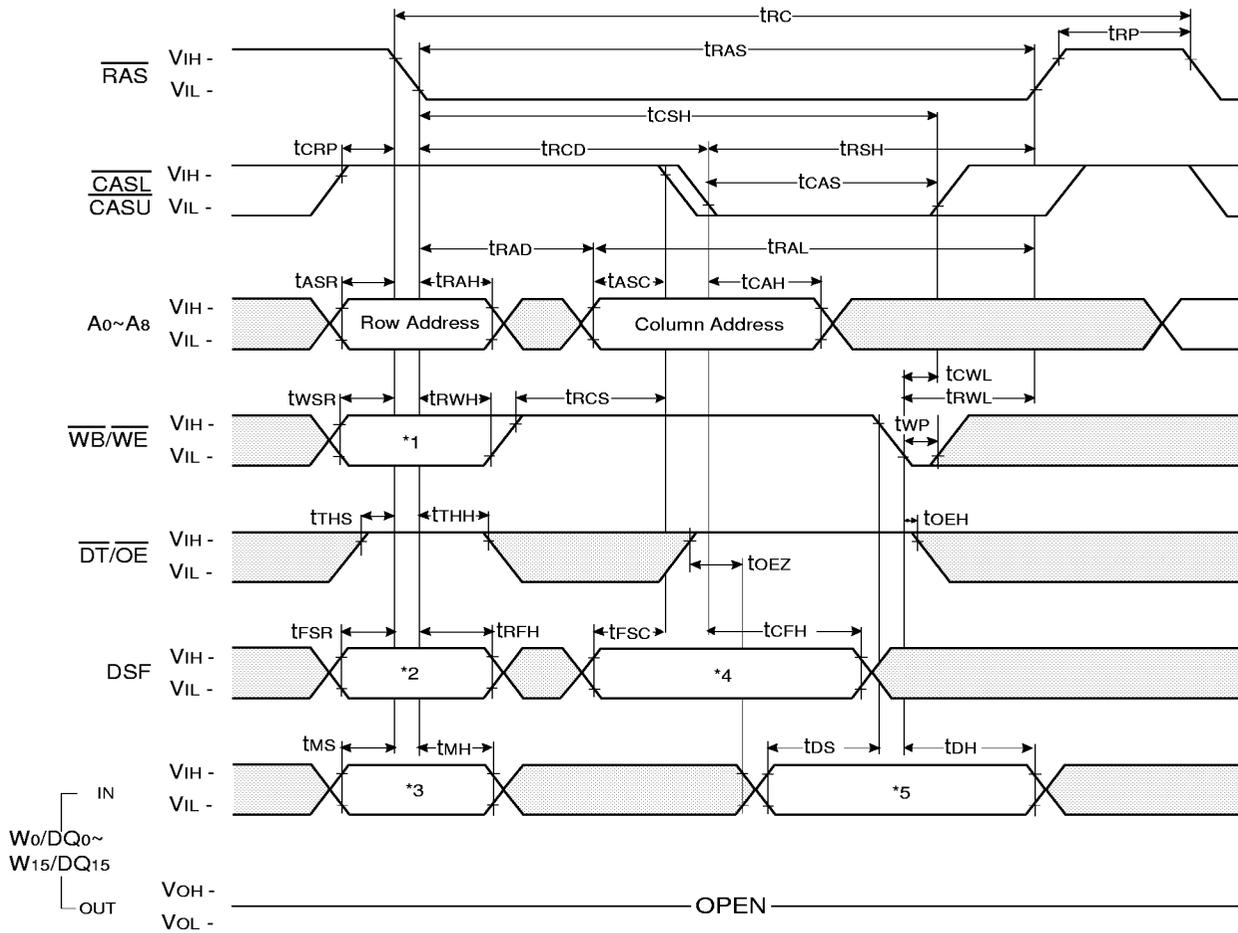
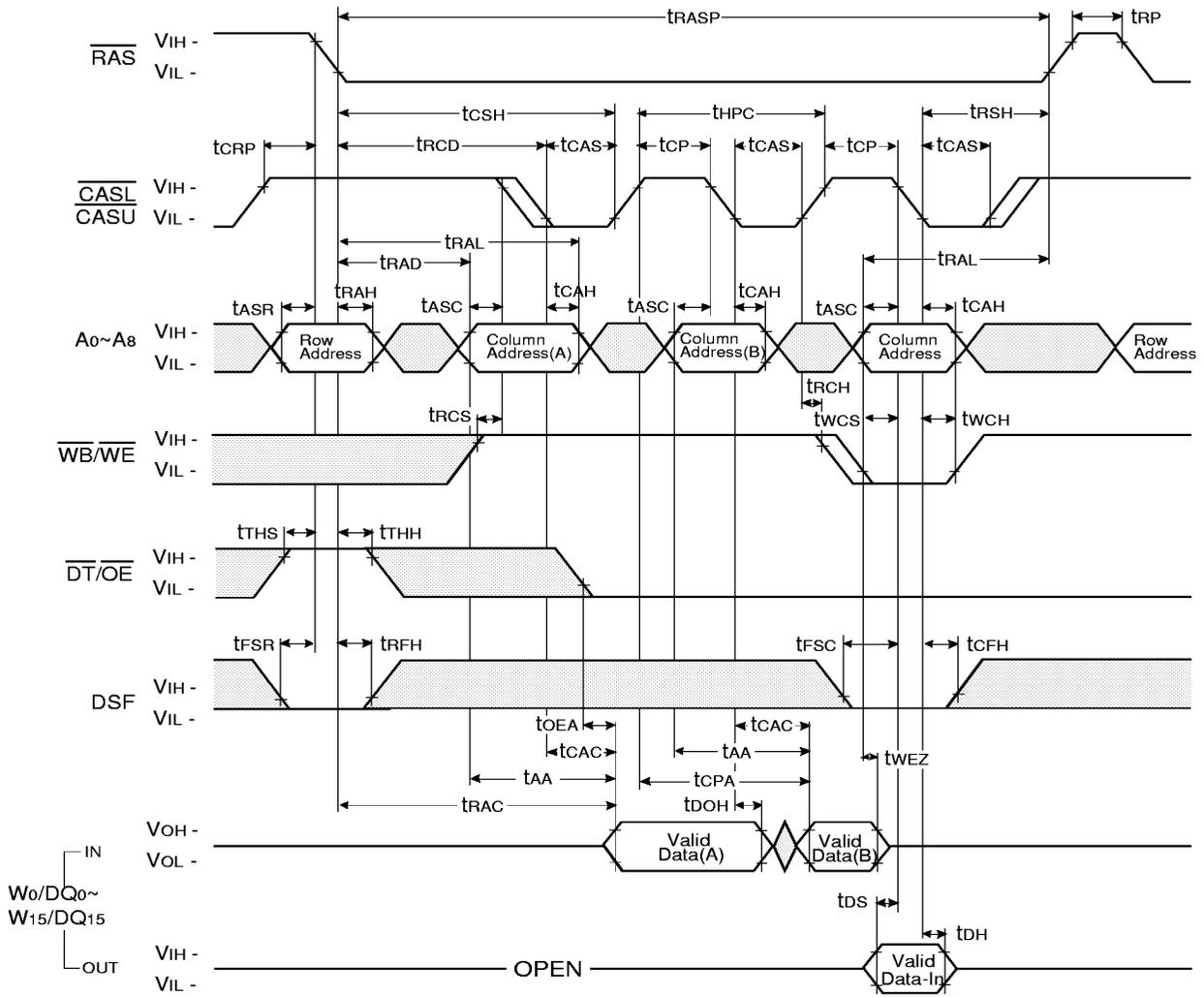Note : In Block Write cycle, only Column Address A3 ~ A8 are used.

Don t care

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READ-WRITE/READ-MODIFY-WRITE CYCLE

Note : In Block Write cycle, only Column Address A3 ~ A8 are used.

▨ Don t care

FAST PAGE MODE READ/WRITE CYCLE (Extended Data Out)

Note : In Block Write cycle, only Column Address A3 ~ A8 are used.

Don t care

FAST PAGE MODE EARLY WRITE CYCLE

Note : In Block Write cycle, only Column Address $A_3 \sim A_8$ are used.

 Don t care

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FAST PAGE MODE READ-MODIFY-WRITE CYCLE

Note : In Block Write cycle, only Column Address A3 ~ A8 are used.

▨ Don t care

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$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

Wo/DQo~   VOH -
W15/DQ15 VOL -   ———— OPEN ————
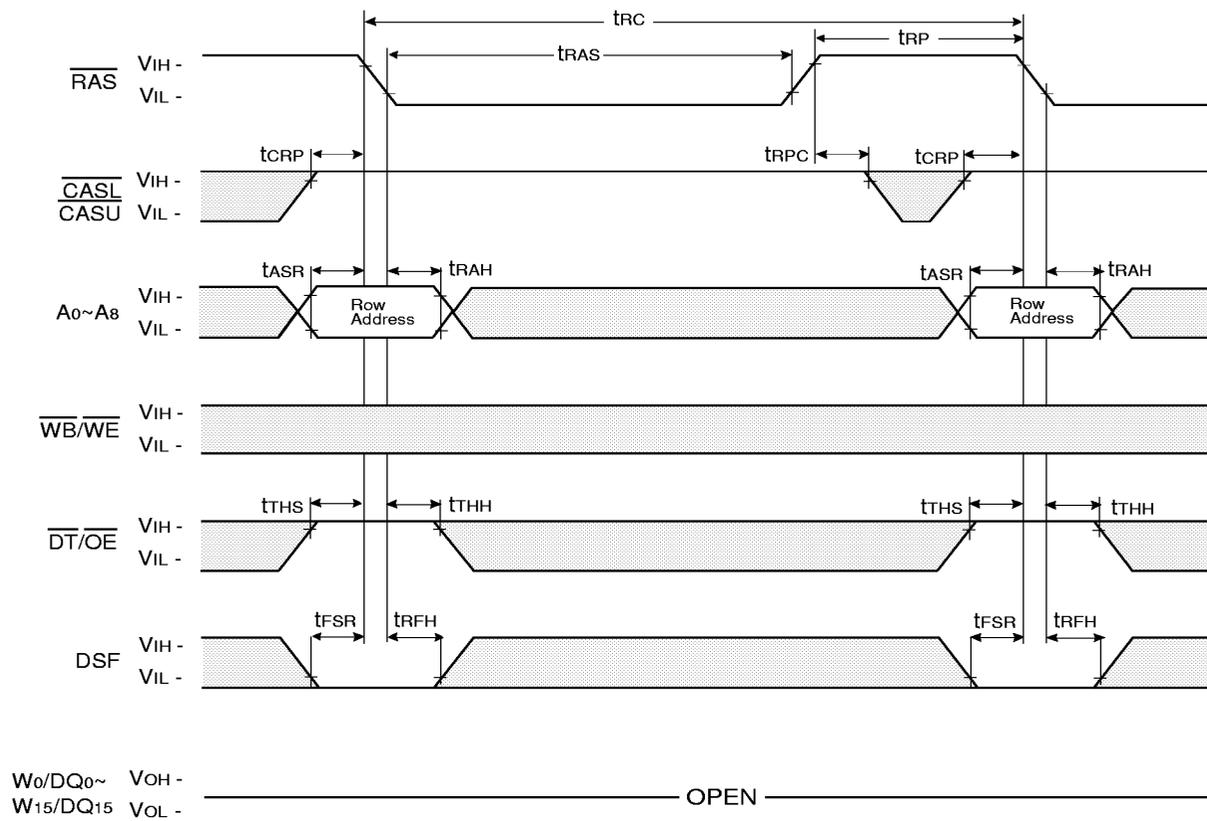
[Don't care]

HIDDEN REFRESH CYCLE
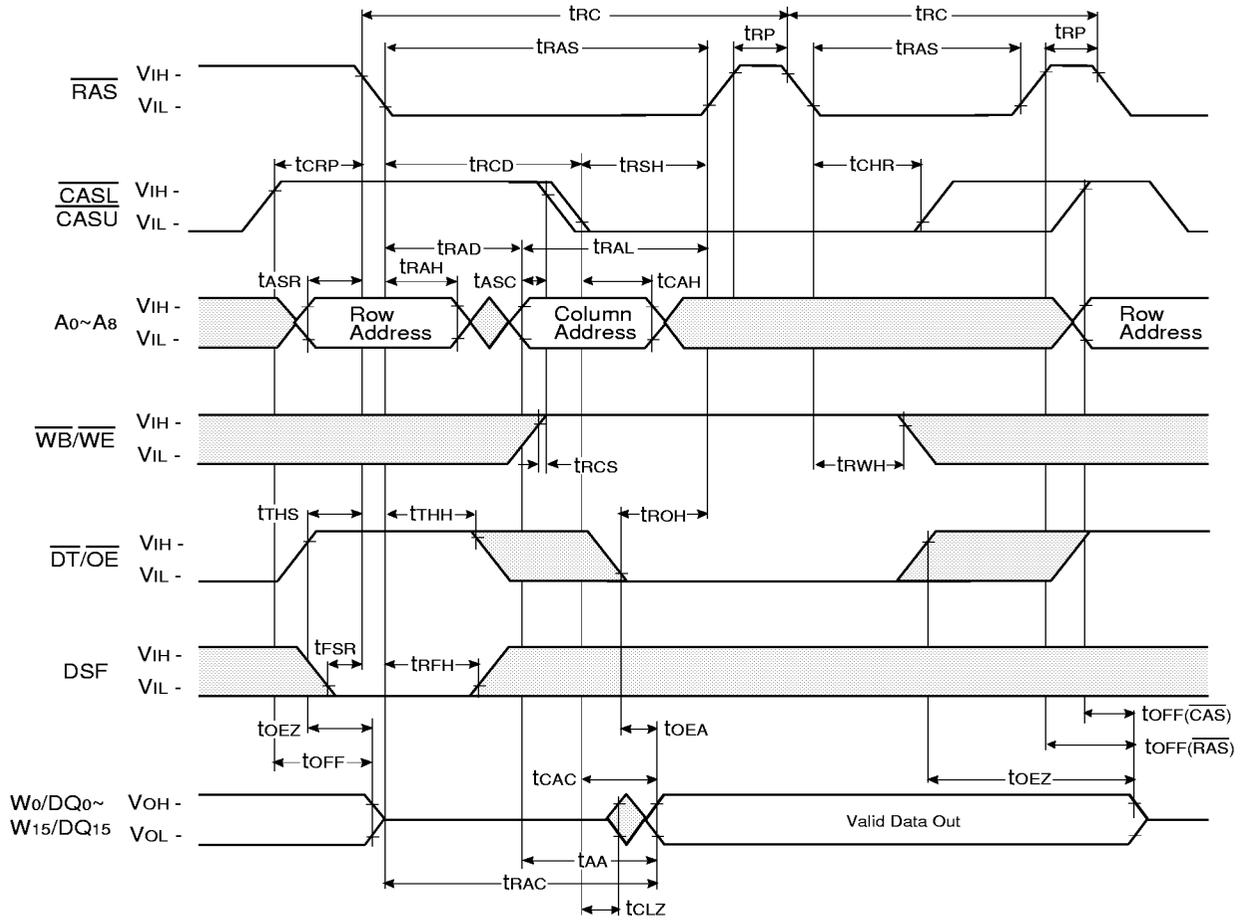
Don t care

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
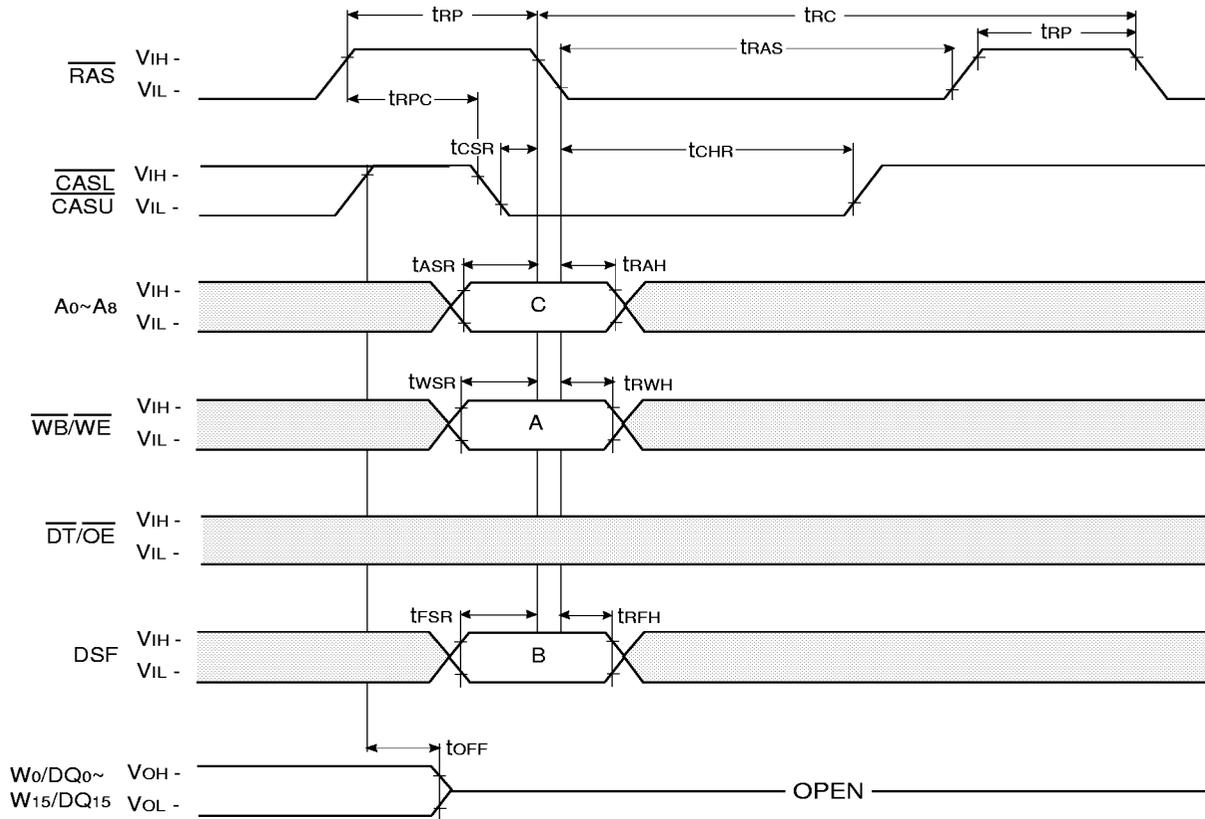
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle Function Table

FUNCTION	CODE	LOGIC STATES		
		A	B	C
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle (Reset All Options)	CBRR	X	0	X
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle (Stop Register Set)	CBRS	0	1	Stop Address
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle (No Reset)	CBRN	1	1	X

☐ Don t care

CAS-BEFORE-RAS SELF REFRESH CYCLE
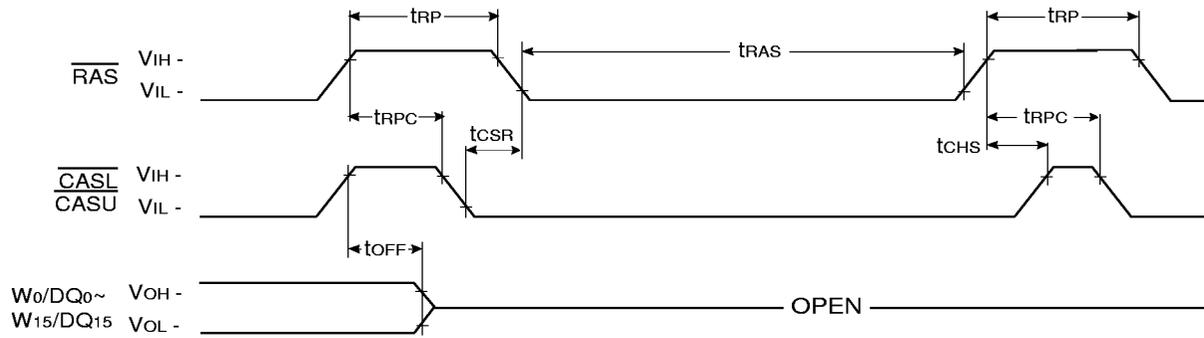
* CBR Self Refresh Cycle is Applicable With CBRR, CBRS, or CBRN Cycle

Don t care

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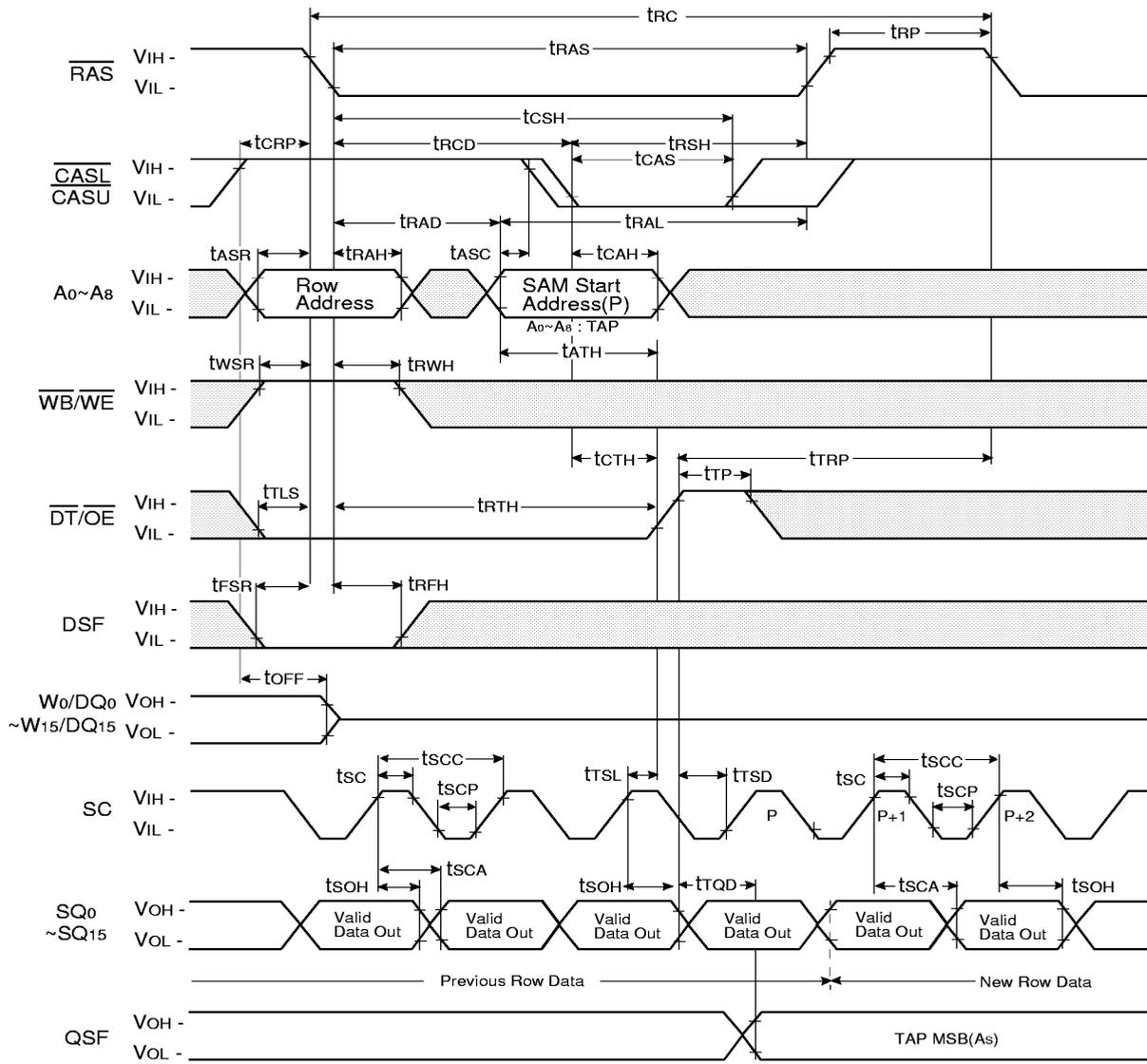## CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE
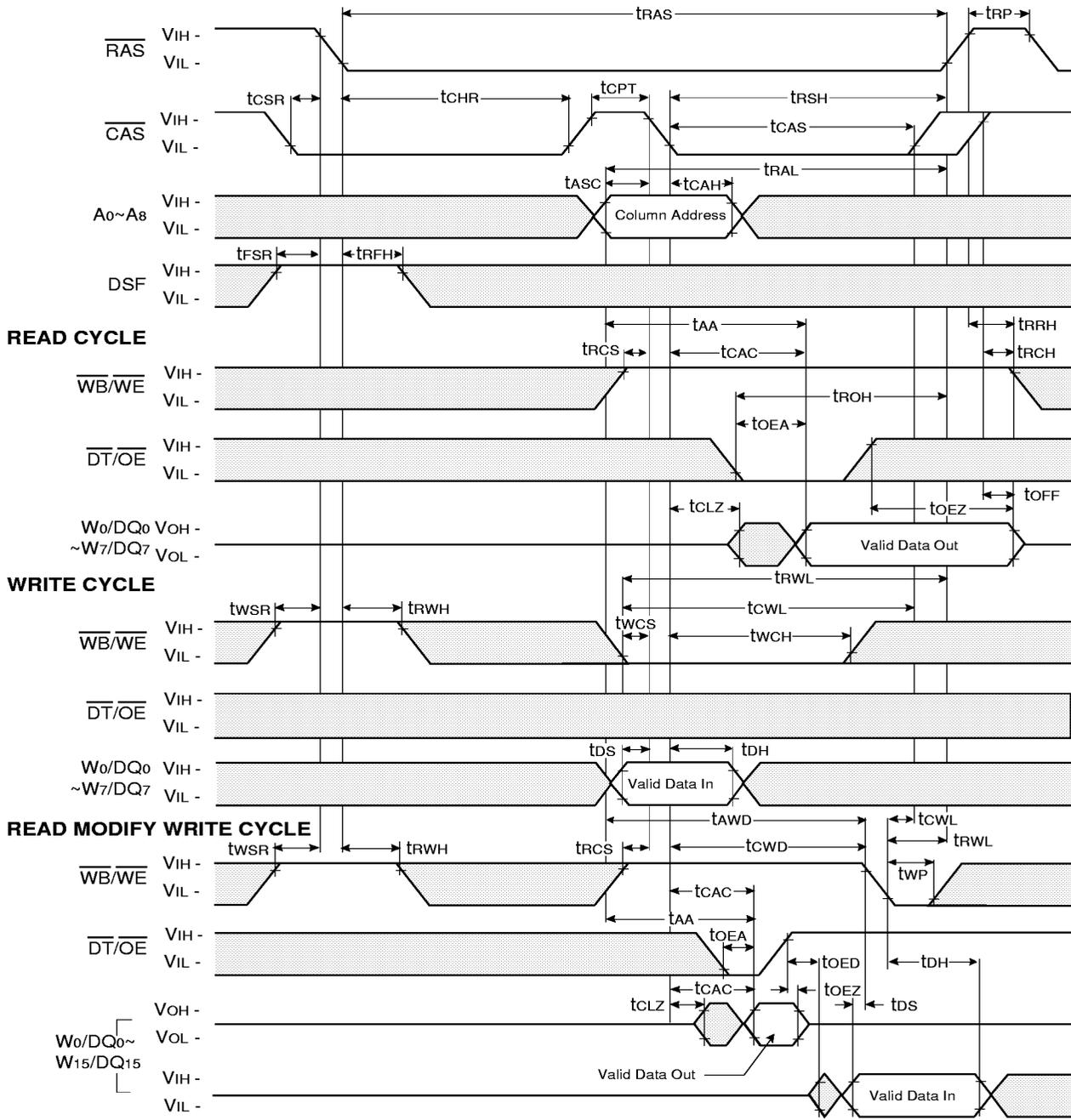
READ TRANSFER CYCLE
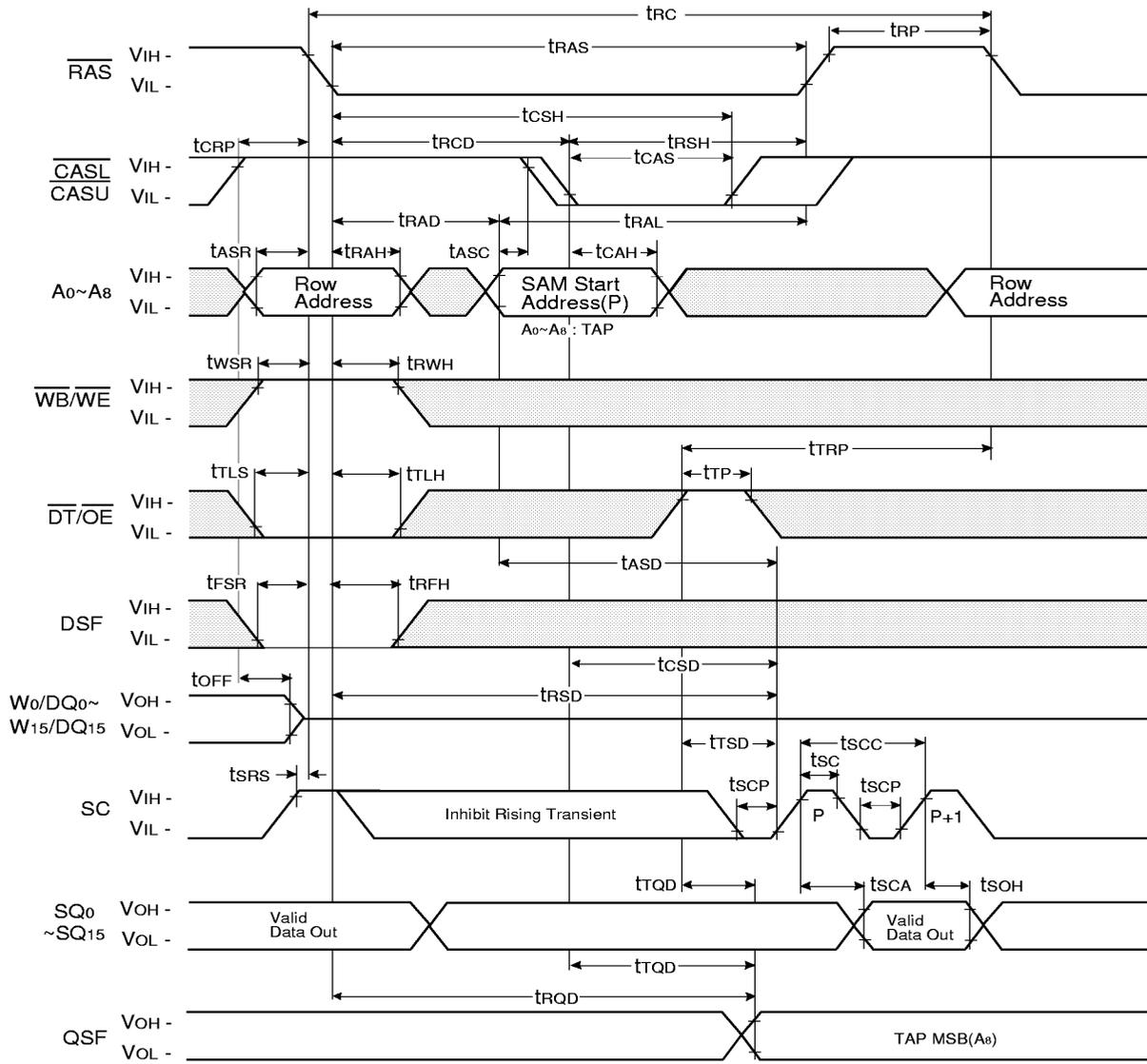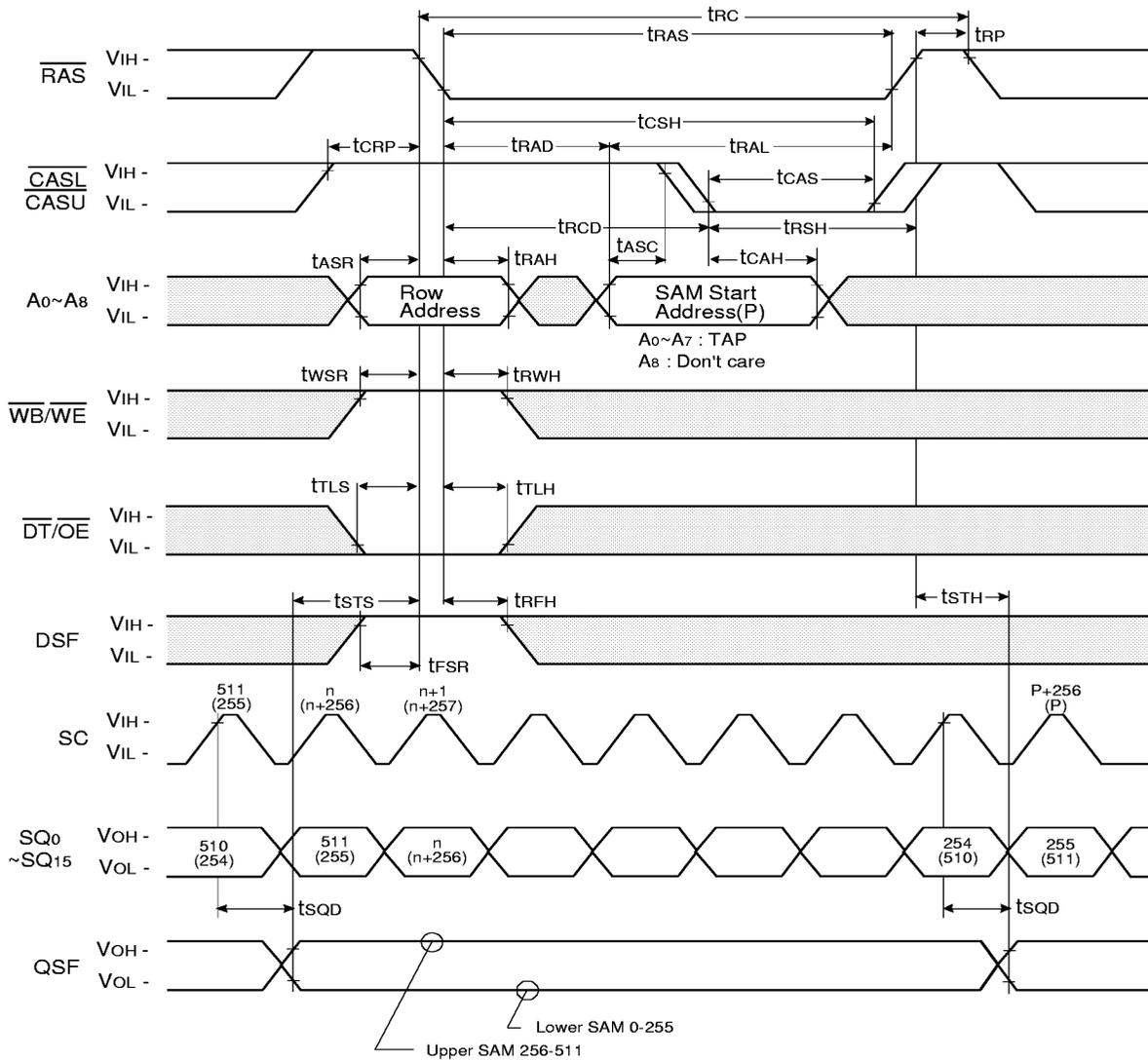

Note : $\overline{SE}$ = V$_{IL}$

☐ Don t care

REAL TIME READ TRANSFER CYCLE
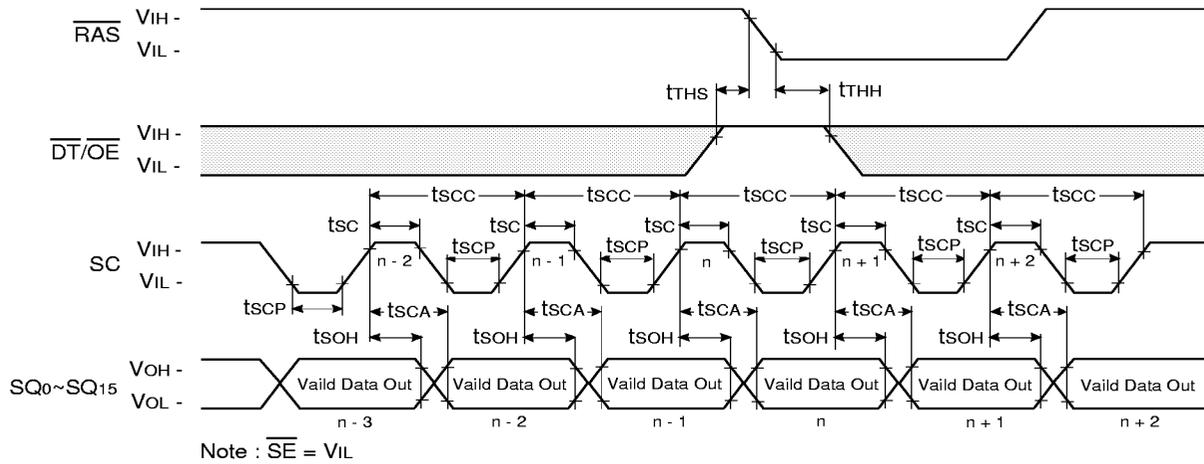

Note : $\overline{SE}$ = V$_{IL}$
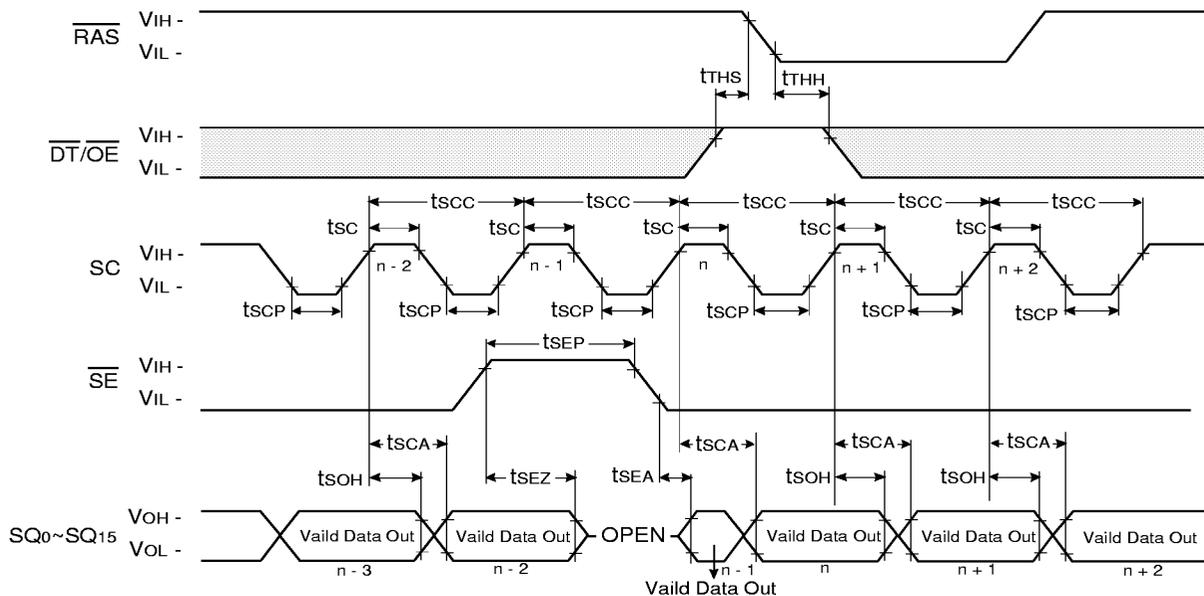
Don t care

SPLIT READ TRANSFER CYCLE

Note : $\overline{SE}$ = V_{IL}

Don t care

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SERIAL READ CYCLE ($\overline{SE}$=V$_{IL}$)

Note : $\overline{SE}$ = V$_{IL}$

SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)

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PACKAGE DIMENSIONS

64 Pin Plastic Small Out Line Package   (Units : Millimeters)