

- ◆ CMOS
- ◆ Highly Accurate : $\pm 2\%$
- ◆ Low Power Consumption : $0.7\mu A$ ($V_{IN} = 1.5V$)
- ◆ Ultra small SSOT-24 (SC-82) Package

General Description

The XC61C series are highly precise, low power consumption voltage detectors, manufactured using CMOS and laser trimming technologies. Detect voltage is extremely accurate with minimal temperature drift.

Both CMOS and N channel open drain output configurations are available.

Applications

- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors

Features

Highly accurate : $\pm 2\%$

Low power consumption : TYP $0.7\mu A$ [$V_{IN}=1.5V$]

Detect voltage range : 1.6V to 6.0V in 0.1V increments

Operating voltage range : 0.7V to 10.0V

Detect voltage temperature characteristics : TYP $\pm 100ppm/^{\circ}C$

Output configuration : N-channel open drain or CMOS

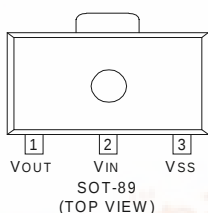
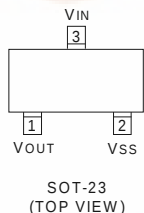
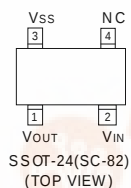
Ultra small package : SSOT-24 (150mW) super mini-mold

: SOT-23 (150mW) mini-mold

: SOT-89 (500mW) mini-power mold

Note : There are no products available with a set-up voltage accuracy of $\pm 1\%$.

Pin Configuration

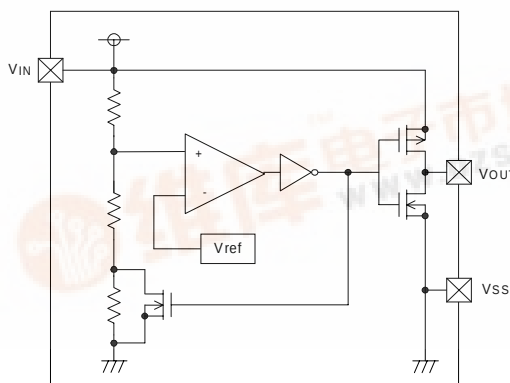


Pin Assignment

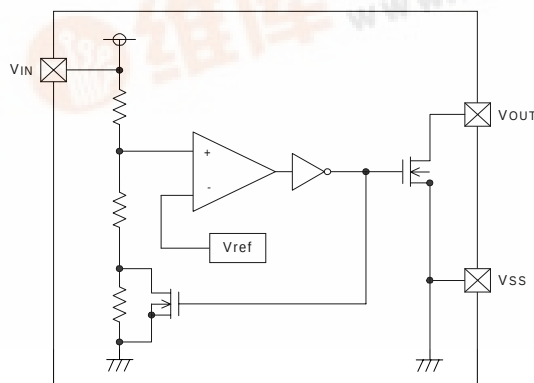
PIN NUMBER			PIN NAME	FUNCTION
SSOT-24	SOT-23	SOT-89		
2	3	2	VIN	Supply Voltage Input
4	2	3	VSS	Ground
1	1	1	VOUT	Output
3	-	-	NC	No Connection

Block Diagram

(1) CMOS Output



(2) Nch Open Drain Output



■ Absolute Maximum Ratings

Ta = 25°C

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage	V _{IN}	12	V
Output Current	I _{OUT}	50	mA
Output Voltage	CMOS	V _{SS} -0.3 to V _{IN} +0.3	V
	Nch open drain		
Power Dissipation	SSOT-24	150	mW
	SOT-23	150	
	SOT-89	500	
Operating Ambient Temperature	T _{opr}	-40 to +85	°C
Storage Temperature	T _{stg}	-40 to +125	°C

■ Electrical Characteristics

V_{DF} (T) = 1.6 to 6.0V ± 2%

Ta = 25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	CIRCUIT
Detect Voltage	V _{DF}		V _{DF} x 0.98	V _{DF}	V _{DF} x 1.02	V	1
Hysteresis Range	V _{HYS}		V _{DF} x 0.02	V _{DF} x 0.05	V _{DF} x 0.08	V	1
Supply Current	I _{SS}	V _{IN} = 1.5V		0.7	2.3	μA	2
		= 2.0V		0.8	2.7		
		= 3.0V		0.9	3.0		
		= 4.0V		1.0	3.2		
		= 5.0V		1.1	3.6		
Operating Voltage	V _{IN}	V _{DF} (T) = 1.6V to 6.0V	0.7		10.0	V	1
Output Current	I _{OUT}	Nch V _{DS} = 0.5V V _{IN} = 1.0V	1.0	2.2		mA	3
		= 2.0V = 3.0V = 4.0V = 5.0V	3.0 5.0 6.0 7.0	7.7 10.1 11.5 13.0			
		Pch V _{DS} = 2.1V V _{IN} = 8.0V (with CMOS output)		-10.0	-2.0		4
Temperature Characteristics	$\frac{\Delta V_{DF}}{\Delta T_{opr} \cdot V_{DF}}$	-40°C ≤ T _{opr} ≤ 85°C		± 100		ppm/°C	-
Delay Time (V _{DR} → V _{OUT} inversion)	t _{DLY}				0.2	ms	5

Note :

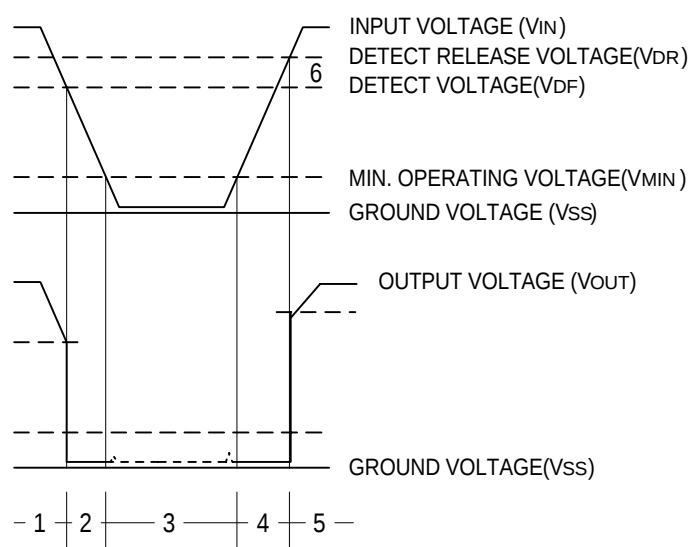
V_{DF} (T) : Established Detect Voltage Value

Release Voltage : V_{DR} = V_{DF} + V_{HYS}

■ Functional Description (CMOS output)

1. When input voltage (V_{IN}) rises above detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to V_{IN} .
(A condition of high impedance exists with Nch open drain output configurations.)
2. When input voltage (V_{IN}) falls below detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to the ground voltage (V_{SS}) level.
3. When input voltage (V_{IN}) falls to a level below that of the minimum operating voltage (V_{MIN}), output will become unstable. In this condition, V_{IN} will equal the pulled-up output (should output be pulled-up.)
4. When input voltage (V_{IN}) rises above the ground voltage (V_{SS}) level, output will be unstable at levels below the minimum operating voltage (V_{MIN}). Between the V_{MIN} and detect release voltage (V_{DR}) levels, the ground voltage (V_{SS}) level will be maintained.
5. When input voltage (V_{IN}) rises above detect release voltage (V_{DR}), output voltage (V_{OUT}) will be equal to V_{IN} . (A condition of high impedance exists with Nch open drain output configurations.)
6. The difference between V_{DR} and V_{DF} represents the hysteresis range.

■ Timing Chart

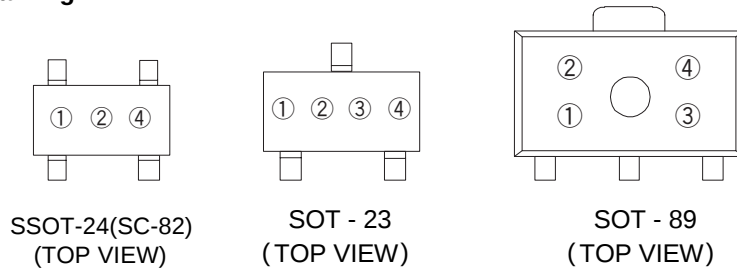


■ Ordering Information

XC61C xx xx xx xx xx
a b c d e f

DESIGNATOR	DESCRIPTION	DESIGNATOR	DESCRIPTION
a	Output Configuration : C = CMOS N = Nch open drain	e	Package Type N = SSOT-24 (SC-82) M = SOT-23 P = SOT-89 T = TO-92
b	Detect Voltage : 25 = 2.5V 38 = 3.8V	f	Device Orientation : R = Embossed Tape (Right) L = Embossed Tape (Left) H = Paper Type (TO-92) B = Bag (TO-92)
c	Output Delay : 0 = No delay		
d	Detect Accuracy : 2 = within $\pm 2.0\%$		

■ Marking



① Represents the integer of the Output Voltage and Detect Voltage

DESIGNATOR	CONFIGURATION	VOLTAGE (V)
A	CMOS	0.②
B	CMOS	1.②
C	CMOS	2.②
D	CMOS	3.②
E	CMOS	4.②
F	CMOS	5.②
H	CMOS	6.②

DESIGNATOR	CONFIGURATION	VOLTAGE (V)
K	Nch	0.②
L	Nch	1.②
M	Nch	2.②
N	Nch	3.②
P	Nch	4.②
R	Nch	5.②
S	Nch	6.②

② Represents the decimal point of the Detect Voltage

DESIGNATOR	VOLTAGE	DESIGNATOR	VOLTAGE
0	①.0	5	①.5
1	①.1	6	①.6
2	①.2	7	①.7
3	①.3	8	①.8
4	①.4	9	①.9

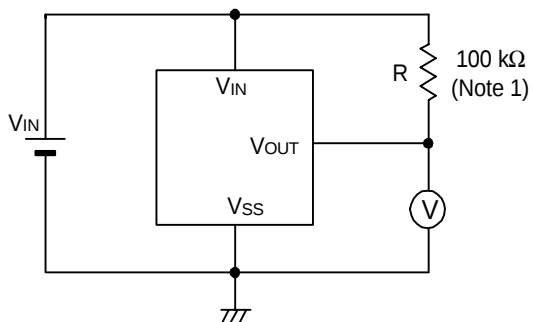
③ Based on Internal Standards
(SSOT-24 excepted)

DESIGNATOR
3

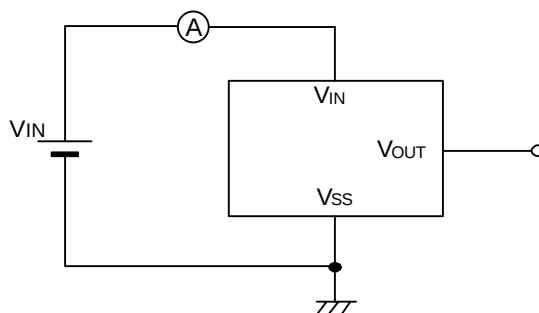
④ Represents the assembly lot no.
Based on internal standards

Measuring Circuits

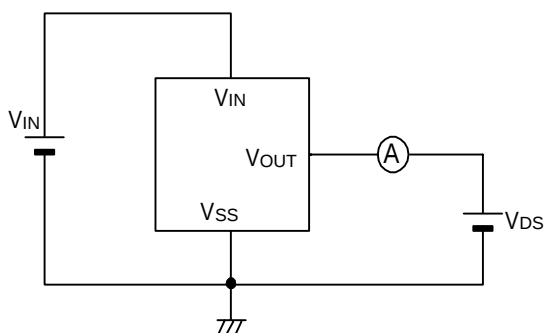
Circuit 1



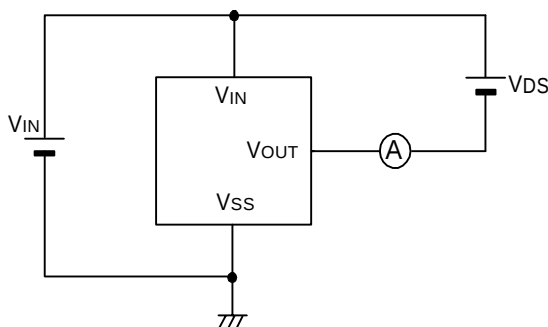
Circuit 2



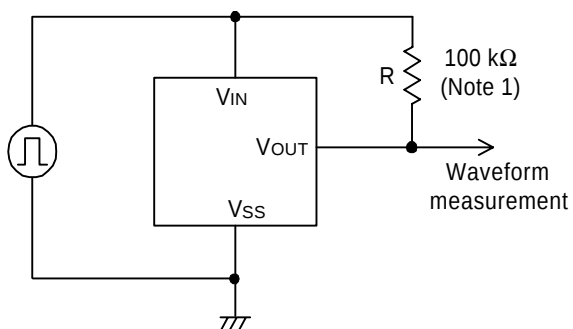
Circuit 3



Circuit 4



Circuit 5



Note 1 : Not necessary with CMOS output products.

■ Notes on Use

1. When a resistor is connected between the V_{IN} pin and the input with CMOS output configurations, oscillation may occur as a result of voltage drops at R_{IN} if load current (I_{OUT}) exists.
(refer to N.B. 1 - (1) below)
2. When a resistor is connected between the V_{IN} pin and the input with CMOS output configurations, irrespective of Nch output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current (I_{OUT}) does not exist.
(refer to N.B. 1 - (2) below)
3. With a resistor connected between the V_{IN} pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the V_{IN} pin.
4. In order to stabilise the IC's operations, please ensure that V_{IN} pin's input frequency's rise and fall times are more than several $\mu\text{sec} / V$.

■ N.B.

1. Oscillation

(1) Output current oscillation with the CMOS output configuration

When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current (I_{OUT}) will flow at R_L . Because a voltage drop ($R_{IN} \times I_{OUT}$) is produced at the R_{IN} resistor, located between the input (IN) and the V_{IN} pin, the load current will flow via the IC's V_{IN} pin. The voltage drop will also lead to a fall in the voltage level at the V_{IN} pin. When the V_{IN} pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at R_{IN} will disappear, the voltage level at the V_{IN} pin will rise and release operations will begin over again.

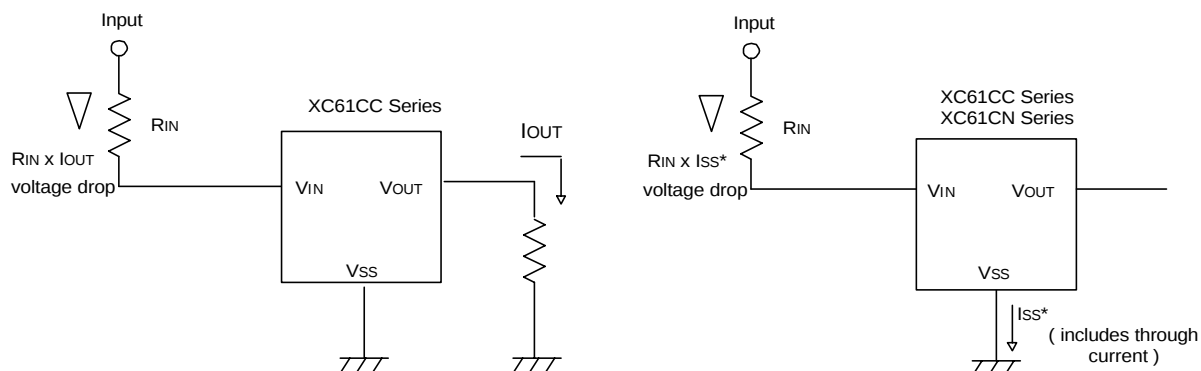
Oscillation may occur with this " release - detect - release " repetition.

Further, this condition will also appear via means of a similar mechanism during detect operations.

(2) Oscillation as a result of through current

Since the XC61C series are CMOS ICs, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor (R_{IN}) during release voltage operations. (refer to diagram 2)

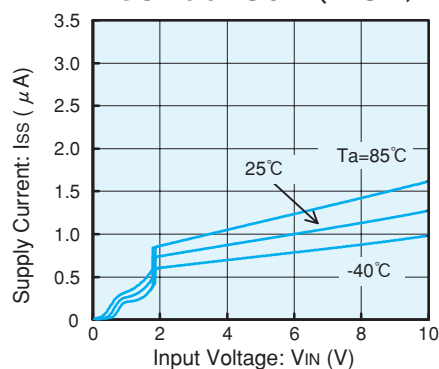
Since hysteresis exists during detect operations, oscillation is unlikely to occur.



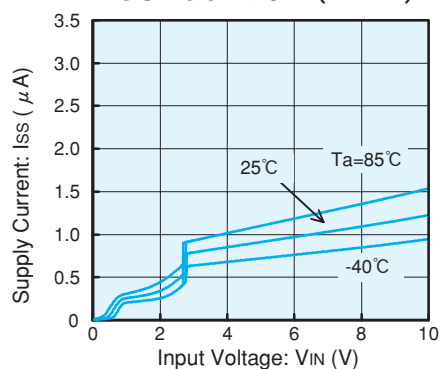
■ Electrical Characteristics

(1) SUPPLY CURRENT vs. INPUT VOLTAGE

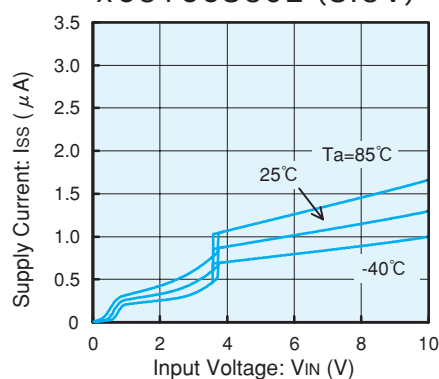
XC61CC1802 (1.8 V)



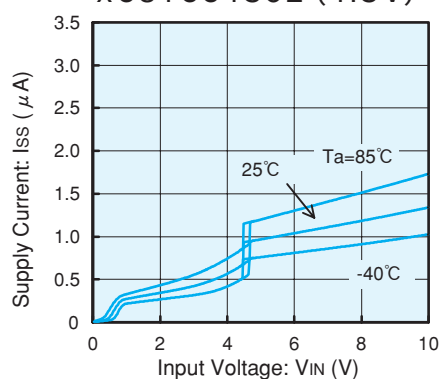
XC61CC2702 (2.7 V)



XC61CC3602 (3.6 V)

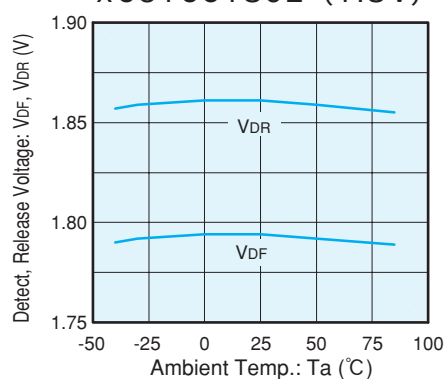


XC61CC4502 (4.5 V)

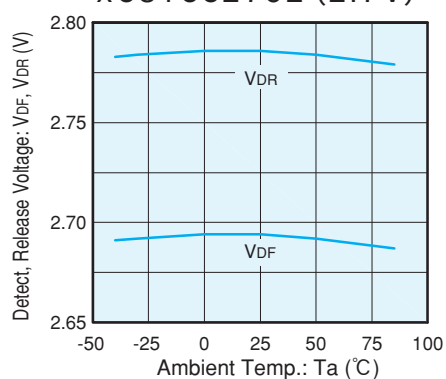


(2) DETECT, RELEASE VOLTAGE vs. AMBIENT TEMP.

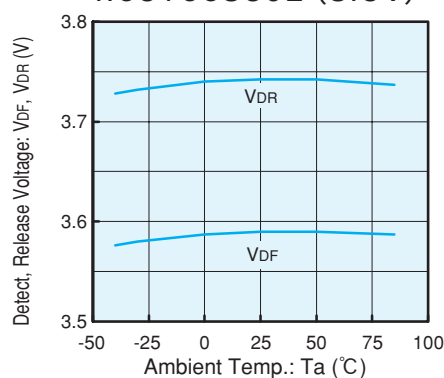
XC61CC1802 (1.8 V)



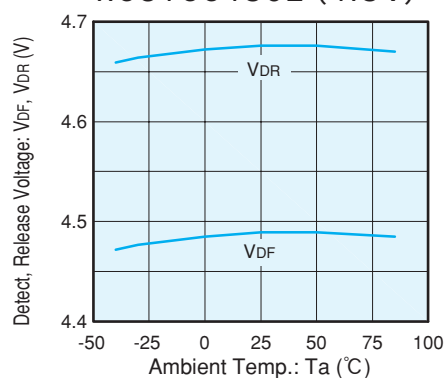
XC61CC2702 (2.7 V)



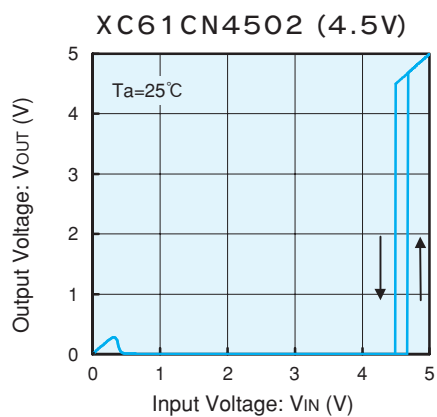
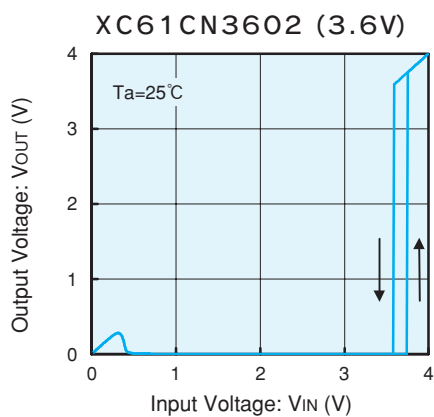
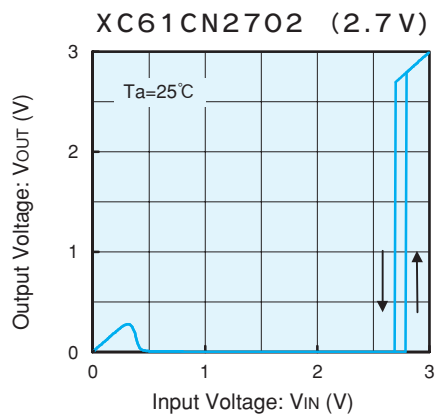
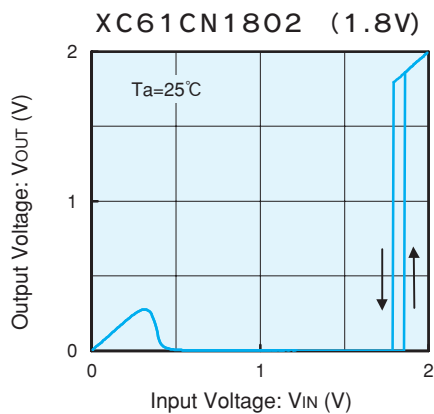
XC61CC3602 (3.6 V)



XC61CC4502 (4.5 V)

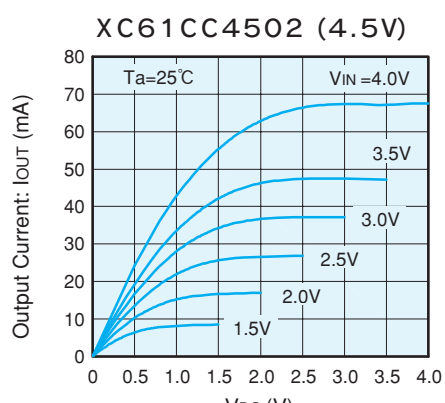
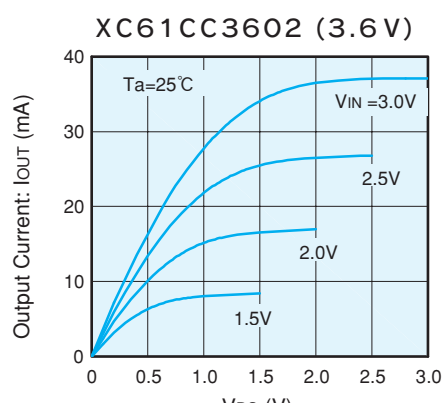
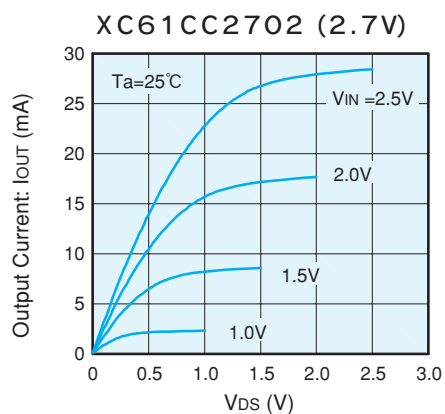
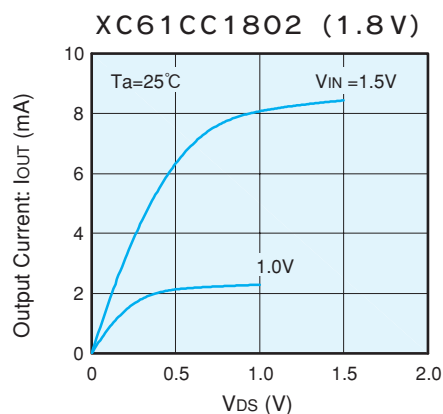


(3) OUTPUT VOLTAGE vs. INPUT VOLTAGE



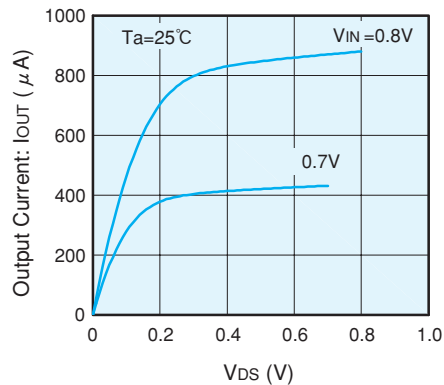
Note : The N-channel open drain pull up resistance value is 100k Ω .

(4) Nch DRIVER OUTPUT CURRENT vs. VDS

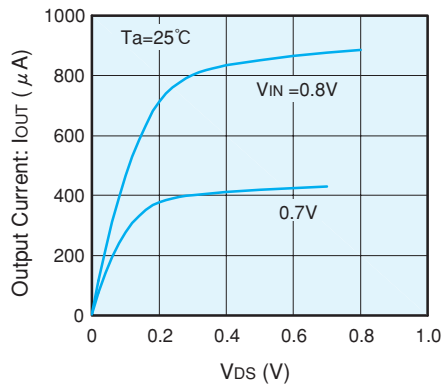


(4) Nch DRIVER OUTPUT CURRENT vs. V_{DS} (contd.)

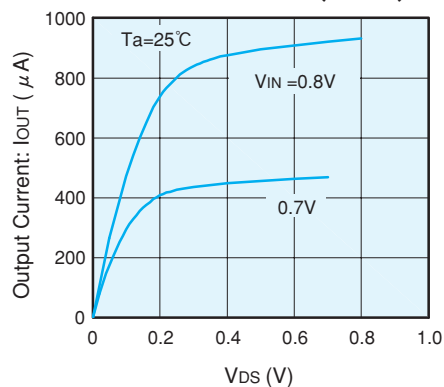
XC61CC1802 (1.8V)



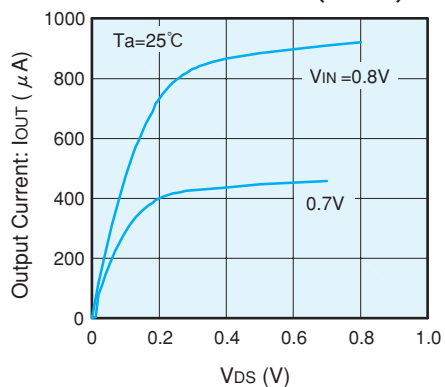
XC61CC2702 (2.7V)



XC61CC3602 (3.6V)

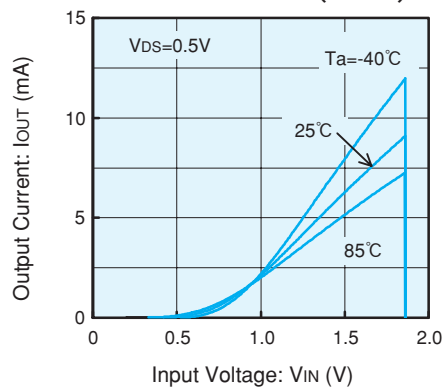


XC61CC4502 (4.5V)

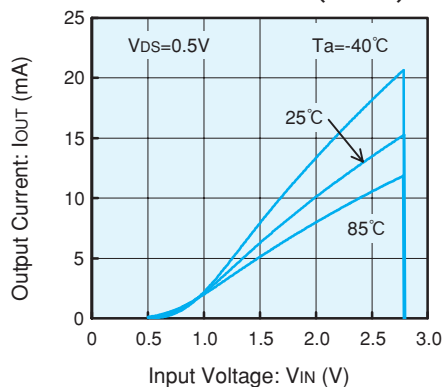


(5) Nch DRIVER OUTPUT CURRENT vs. INPUT VOLTAGE

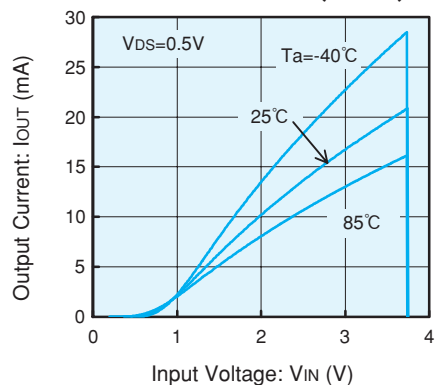
XC61CC1802 (1.8V)



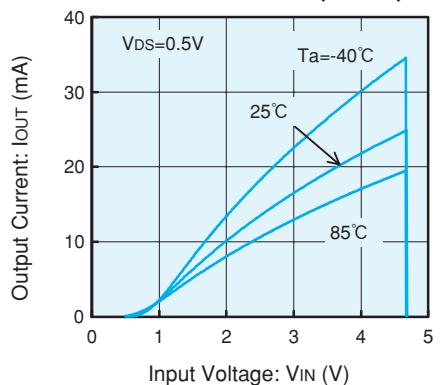
XC61CC2702 (2.7V)



XC61CC3602 (3.6V)



XC61CC4502 (4.5V)



(6) Pch DRIVER OUTPUT CURRENT vs. INPUT VOLTAGE

