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Winbond Electronics Corp.

10-MEMORY TONE/PULSE DIALER WITH HANDFREE AND HOLD FUNCTIONS

GENERAL DESCRIPTION

The W91340N series are tone/pluse switchable telephone dialers with ten memories, hold function, and a handfree dialing control circuit. Fabricated using CMOS technology, the W91340N series offer good performance in low-voltage and low-power applications.

FEATURES

- DTMF/pulse switchable dialer
- 32-digit redial memory
- Ten by 16-digit two-touch direct repertory memory
- Cascaded dialing allowed, with unlimited dialing length
- Pulse-to-tone (*/T) keypad for long distance call operation
- Uses 5 × 4 keyboard
- Easy operation with redial, flash, pause, and */T keypads
- Pause, P→T (pulse-to-tone) can be stored as a digit in memory
- Dialing rate (10 ppS or 20 ppS) is selectable by bonding option
- On-hook debounce time: 150 msec.
- Minimum tone output duration: 93 msec. (W91344AN: 87 mS)
- Minimum intertone pause: 93 msec. (W91344AN: 87 mS)
- Flash break time (73, 100, 300, 600 msec) selectable by keypad; pause time is 1.0 sec.
- Make/break ratio (40:60 or 33.3:66.7) selectable by MODE pin
- On-chip power-on reset
- Uses 3.579545 MHz crystal or ceramic resonator
- Packaged in 18 or 20-pin plastic DIP
- The different dialers in the W91340N series are shown in the following table:

TYPE NO.	REPLACEMENT TYPE NO.	PULSE (ppS)	FLASH (mS)	M/B	HANDFREE DIALING	PACKAGE (PINS)
W91340N	W91340	10	600/300/73/100	Pin	-	18
	W91341					
W91342N	W91342	20	600/300/73/100	Pin	-	18
W91340AN	W91340A	10	600/300/73/100	Pin	Yes	20
	W91341A					
W91342AN	W91342A	20	600/300/73/100	Pin	Yes	20
W91344AN	New type	10	600/300/73/100	Pin	Yes	20

Note: The W91344AN is designed specifically for use in France. The pause time is not added in pulse-to-tone mode.

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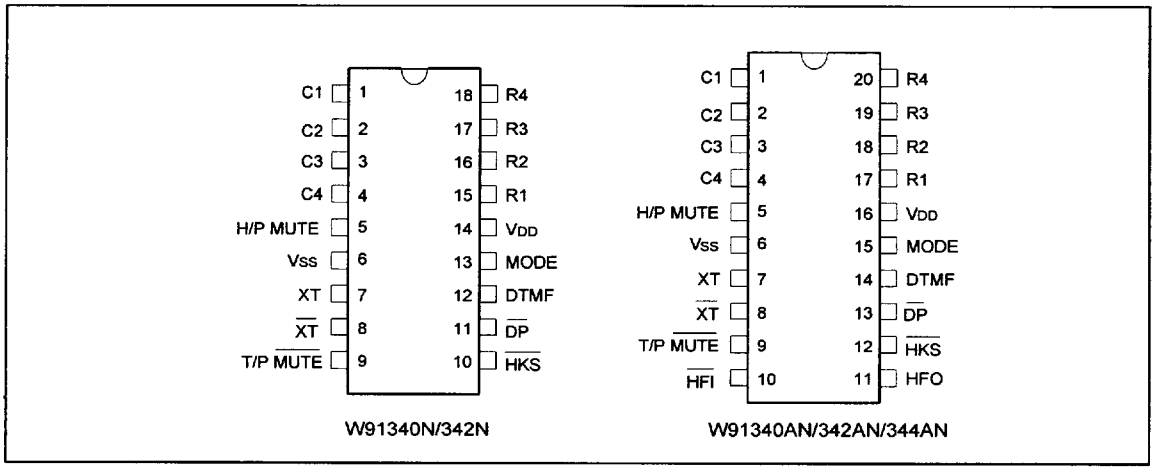
PIN CONFIGURATIONS



PIN DESCRIPTION

SYMBOL	18-PIN	20-PIN	I/O	FUNCTION
Column-Row Inputs	1–4 & 15–18	1–4 & 17–20	I	The keyboard inputs may be used with either a standard 5 × 4 keyboard or an inexpensive single contact (Form A) keyboard. Electronic input from a μC can also be used. A valid key is defined as a single row being connected to a single column.
XT, $\overline{XT}$	7, 8	7, 8	I, O	A built-in inverter provides oscillation with an inexpensive 3.579545 MHz crystal or ceramic resonator.
T/P $\overline{MUTE}$	9	9	O	The T/P $\overline{MUTE}$ is a conventional CMOS N-channel open drain output. The output transistor is switched on during dialing sequence and flash break time. Otherwise, it is switched off.
MODE	13	15	I	Pulling mode pin to VSS places the dialer in tone mode. Pulling mode pin to VDD places the dialer in pulse mode with M/B ratio of 40:60 (10 ppS, except for W91342N/W91342AN = 20 ppS.) Floating mode pin places the dialer in pulse mode with M/B ratio of 33.3:66.7 (10 ppS, except for W91342N/W91342AN = 20 ppS.)
$\overline{HKS}$	10	12	I	Hook switch input. $\overline{HKS}$ = VDD: On-hook state. Chip in sleeping mode, no operation. $\overline{HKS}$ = VSS: Off-hook state. Chip is enabled for normal operation. $\overline{HKS}$ pin is pulled to VDD by an internal resistor.

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Pin Description, continued

<table>
<tr><th>SYMBOL</th><th>18-PIN</th><th>20-PIN</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>$\overline{DP}$</td><td>11</td><td>13</td><td>O</td><td>N-channel open drain dialing pulse output.
Flash key will cause $\overline{DP}$ to be active in either tone mode or pulse mode.
The timing diagram for pulse mode is shown in Figure 1(a, b, c).</td></tr>
<tr><td>VDD, VSS</td><td>14, 6</td><td>16, 6</td><td>I</td><td>Power input pins.</td></tr>
<tr><td>DTMF</td><td>12</td><td>14</td><td>O</td><td>In pulse mode, this pin remains in low state at all times. In the tone mode, it will output a dual or single tone. Detailed timing diagram for tone mode is shown in Figure 2(a, b, c).
<table>
<tr><th colspan="4">Output Frequency</th></tr>
<tr><th></th><th>Specified</th><th>Actual</th><th>Error %</th></tr>
<tr><td>R1</td><td>697</td><td>699</td><td>+0.28</td></tr>
<tr><td>R2</td><td>770</td><td>766</td><td>-0.52</td></tr>
<tr><td>R3</td><td>852</td><td>848</td><td>-0.47</td></tr>
<tr><td>R4</td><td>941</td><td>948</td><td>+0.74</td></tr>
<tr><td>C1</td><td>1209</td><td>1216</td><td>+0.57</td></tr>
<tr><td>C2</td><td>1336</td><td>1332</td><td>-0.30</td></tr>
<tr><td>C3</td><td>1477</td><td>1472</td><td>-0.34</td></tr>
</table></td></tr>
<tr><td>$\overline{HFI}$, HFO</td><td>-</td><td>10, 11</td><td>I, O</td><td>Handfree control pins. The handfree control state is toggled on by a low pulse on the $\overline{HFI}$ input pin. The status of the handfree control state is described in the following table:
<table>
<tr><th colspan="2">CURRENT STATE</th><th colspan="3">NEXT STATE</th></tr>
<tr><th>Hook SW.</th><th>HFO</th><th>Input</th><th>HFO</th><th>Dialing</th></tr>
<tr><td>–</td><td>Low</td><td>$\overline{HFI}$ ↓</td><td>High</td><td>Yes</td></tr>
<tr><td>On Hook</td><td>High</td><td>$\overline{HFI}$ ↓</td><td>Low</td><td>No</td></tr>
<tr><td>Off Hook</td><td>High</td><td>$\overline{HFI}$ ↓</td><td>Low</td><td>Yes</td></tr>
<tr><td>On Hook</td><td>–</td><td>Off Hook</td><td>Low</td><td>Yes</td></tr>
<tr><td>Off Hook</td><td>Low</td><td>On Hook</td><td>Low</td><td>No</td></tr>
<tr><td>Off Hook</td><td>High</td><td>On Hook</td><td>High</td><td>Yes</td></tr>
</table>
$\overline{HFI}$ pin is pulled to VDD by an internal resistor.
Detailed timing diagram is shown in Figure 3.</td></tr>
<tr><td>H/P MUTE</td><td>5</td><td>5</td><td>O</td><td>The H/P MUTE is a conventional inverter output. During pulse dialing, flash break or hold period, this output is active high; otherwise, it remains in low state.</td></tr>
</table>

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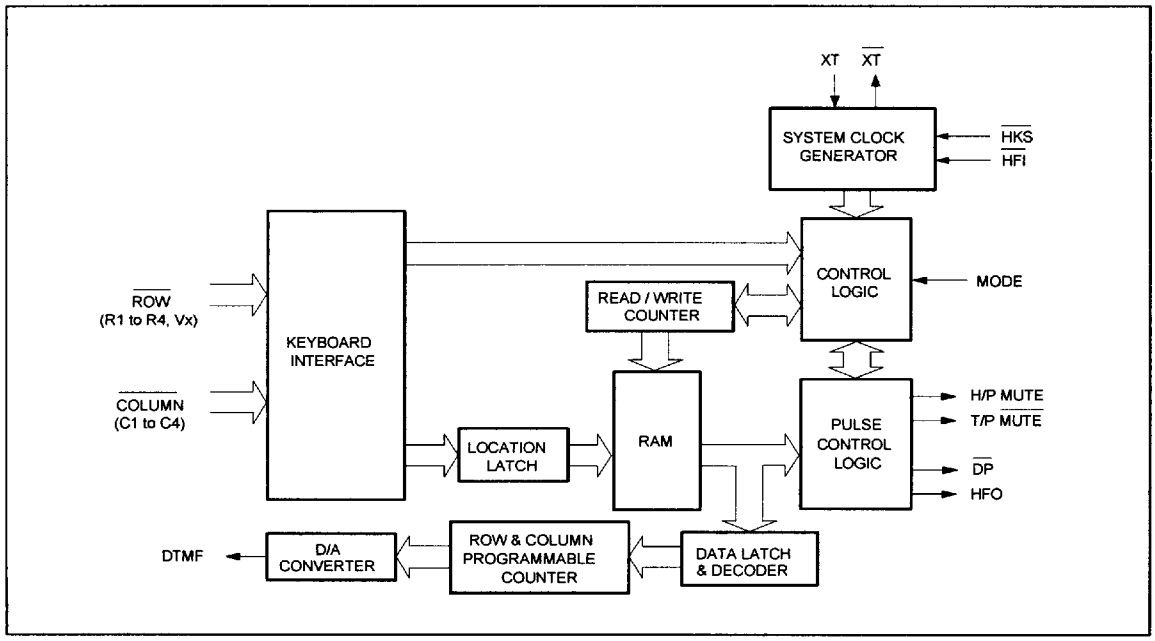
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Keyboard Operation

C1	C2	C3	C4	
1	2	3	S	R1
4	5	6	F4	R2
7	8	9	A	R3
*/T	0	#	R/P	R4
F1	F2	F3	H	Vx

- S: Store function key
- H: Hold function key
- A: Indirect repertory memory dialing function key
- R/P: Redial and pause function key
- */T: * in tone mode and P→T in pulse mode
- F1, ..., F4: Flash keys, F1 = 600 mS, F2 = 300 mS, F3 = 73 mS, F4 = 100 mS

Notes:
D1, ..., Dn, D1', ..., Dn': 0, ..., 9, */T, #
Ln: 0, ..., 9 ; Fn: F1, ..., F4

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Normal Dialing

[OFF HOOK] , (or [ON HOOK] & [HFI •• _]), [D1] , [D2] , ..., [Dn]

1. D1, D2, ..., Dn will be dialed out.
2. Dialing length is unlimited, but redial is inhibited if length exceeds 32 digits in normal dialing.

Redialing

[OFF HOOK] , (or [ON HOOK] & [HFI •• _]), [D1] , [D2] , ..., [Dn] Busy, Come

[ON HOOK] , [OFF HOOK] , (or [ON HOOK] & [HFI •• _]), [R/P]

1. The redial memory content will be dialed out.
2. The [R/P] key can execute the redial function only as the first key-in after off-hook; otherwise, it executes pause function.

Number Store

[OFF HOOK] , (or [ON HOOK] & [HFI •• _]), [D1] , [D2] , ..., [Dn] , [S] , [S] , [Ln]

1. If the sequence of the dialed digits D1, D2, ..., Dn has not finished, [S] will be ignored.
2. D1, D2, ..., Dn will be dialed out and stored in memory location.

[OFF HOOK] , (or [ON HOOK] & [HFI •• _]), [S] , [D1] , [D2] , ..., [Dn] , [S] , [Ln]

3. D1, D2, ..., Dn will be stored in memory location but will not be dialed out.
4. [R/P] and [*/T] keys can be stored as a digit in memory.

   In store mode, [R/P] is the pause function key.
5. The store mode is released after the store function is executed or when the state of the hook switch is changed.

Repertory Dialing

[OFF HOOK] , (or [ON HOOK] & [HFI •• _]), [A] , [Ln]

Access Pause

[OFF HOOK] , (or [ON HOOK] & [HFI •• _]), [D1] , [D2] , [R/P] , [D3] , ..., [Dn]

1. The pause function can be stored as a digit in memory.

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2. The pause function is executed in normal dialing, redial dialing, or memory dialing.
3. The detailed timing diagram for the pause function is shown in Figure 4.

Pulse-to-tone (*/T)

[OFF HOOK] , (or [ON HOOK] & [HFI •-•_]), [D1] , [D2] , ..., [Dn] , [*/T] , [D1']

, [D2'] , ..., [Dn']

1. If the mode switch is set to pulse mode, then the output signal will be as follows:

All versions except W91344AN:

D1, D2, ..., Dn, Pause (3.6 sec.), D1', D2', ..., Dn'
(Pulse) (Tone)

W91344AN:

D1, D2, ..., Dn, *, D1', D2', ..., Dn'
(Pulse) (Tone) (Tone)

2. If the mode switch is set to tone mode, then the output signal will be as follows:

D1, D2, ..., Dn, *, D1', D2', ..., Dn'
(Tone) (Tone)

3. The dialer remains in tone mode when the digits have been dialed out and can be reset to pulse mode only by going on-hook.
4. The pulse-to-tone function timing diagram is shown in Figure 5(a, b).

Flash

[OFF HOOK] , (or [ON HOOK] & [HFI •-•_]), [Fn]

1. Fn = F1, ..., F4
2. The dialer will execute a flash break time of 600 mS (F1), 300 mS (F2), 73 mS (F3), or 100 mS (F4).

   In each case the flash pause time is 1.0 sec. before the next digit is dialed out.
3. Flash key cannot be stored as a digit in memory, and it has first priority among keyboard functions.
4. The system will return to the initial state after the flash pause time is finished.
5. The flash function timing diagram is shown in Figure 6.

Cascaded Dialing

1. [Normal Dialing] + [Repertory Dialing] + [Normal Dialing]
2. [Repertory Dialing] + [Normal Dialing] + [Repertory Dialing]
3. [Redialing] + [Normal Dialing] + [Repertory Dialing]

   Redialing is valid as first key-in only.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}–V_{SS}	-0.3 to +7.0	V
Input/Output Voltage	V_{IL}	V_{SS} -0.3	V
	V_{IH}	V_{DD} +0.3	V
	V_{OL}	V_{SS} -0.3	V
	V_{OH}	V_{DD} +0.3	V
Power Dissipation	P_D	120	mW
Operation Temperature	T_{OPR}	-20 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

(V_{DD}–V_{SS} = 2.5V, $F_{OSC.}$ = 3.579545 MHz, T_A = 25° C, all outputs unloaded)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V_{DD}	-	2.0	-	5.5	V
Operating Current	I_{OP}	Tone, Unloaded	-	0.4	0.6	mA
		Pulse, Unloaded	-	0.2	0.4	
Standby Current	I_{SB}	$\overline{HKS}$ = V_{SS}, No load & No key entry	-	-	15	µA
Memory Retention Current	I_{MR}	$\overline{HKS}$ = V_{DD}, V_{DD} = 1.0V	-	-	0.2	µA
DTMF Output Voltage	V_{TO}	Row group, R_L = 5 KΩ	130	150	170	mVrms
Pre-emphasis	-	Col/Row, V_{DD} = 2.0 to 5.5V	1	2	3	dB
DTMF Distortion	THD	R_L = 5 KΩ, V_{DD} = 2.0 to 5.5V	-	-30	-23	dB
DTMF Output DC Level	V_{TDC}	R_L = 5 KΩ, V_{DD} = 2.0 to 5.5V	1.0	-	3.0	V
DTMF Output Sink Current	I_{TL}	V_{TO} = 0.5V	0.2	-	-	mA
$\overline{DP}$ Output Sink Current	I_{PL}	V_{PO} = 0.5V	0.5	-	-	mA
T/P $\overline{MUTE}$ Output Sink Current	I_{ML}	V_{MO} = 0.5V	0.5	-	-	mA

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DC Characteristics, continued

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
H/P Mute Output Drive/Sink Current	I_{HPH}	V_{HPH} = 2.0V	0.5	-	-	mA
	I_{HPL}	V_{HPL} = 0.5V	0.5	-	-	mA
HFO Drive/Sink Current	I_{HFH}	V_{HFH} = 2.0V	0.5	-	-	mA
	I_{HFL}	V_{HFL} = 0.5V	0.5	-	-	mA
Keypad Input Drive Current	I_{KD}	V_I = 0.0V	30	-	-	µA
Keypad Input Sink Current	I_{KS}	V_I = 2.5V	200	400	-	µA
$\overline{HKS}$ I/P Pull-high Resistor	R_{HK}	-	-	300	-	KΩ
Keypad Resistance	R_K	-	-	-	5.0	KΩ

AC CHARACTERISTICS

(V_{DD}–V_{SS} = 2.5V, $F_{OSC.}$ = 3.579545 MHz, T_A = 25° C, all outputs unloaded)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Key-in Debounce	T_{KID}	-	-	20	-	mS
Key Release Debounce	T_{KRD}	-	-	20	-	mS
On-hook Debounce	T_{OHD}	-	-	150	-	mS
Pre-digit Pause[1]	T_{PDP1}	Mode = V_{DD}	-	40	-	mS
	10 ppS	Mode = Floating	-	33.3	-	
Pre-digit Pause[2]	T_{PDP2}	Mode = V_{DD}	-	20	-	mS
	20 ppS	Mode = Floating	-	16.7	-	
Interdigit Pause (Auto Dialing)	T_{IDP}	10 ppS	-	800	-	mS
		20 ppS	-	500	-	
Make/Break Ratio	M/B	Mode = V_{DD}	-	40:60	-	%
		Mode = Floating	-	33.3:66.7	-	
Tone Output Duration	T_{TD}	Auto dialing	-	93	-	mS
		W91344AN Only	-	87	-	
Intertone Pause	T_{ITP}	Auto dialing	-	93	-	mS
		W91344AN Only	-	87	-	
Flash Break Time	T_{FB}	F1	-	600	-	mS
		F2	-	300	-	
		F3		73		
		F4	-	100	-	
Flash Pause Time	T_{FP}	F1, F2, F3, F4	-	1.0	-	S
Pause Time	T_P	R/P	-	3.6	-	S

Notes:

1. Crystal parameters suggested for proper operation are Rs<100Ω Lm = 96 mH, Cm = 0.02 pF, Cn = 5 pF, Cl = 18 pF, Fosc.= 3.579545 MHz± 0.02%.
2. Crystal oscillator accuracy directly affects these times.

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TIMING WAVEFORMS

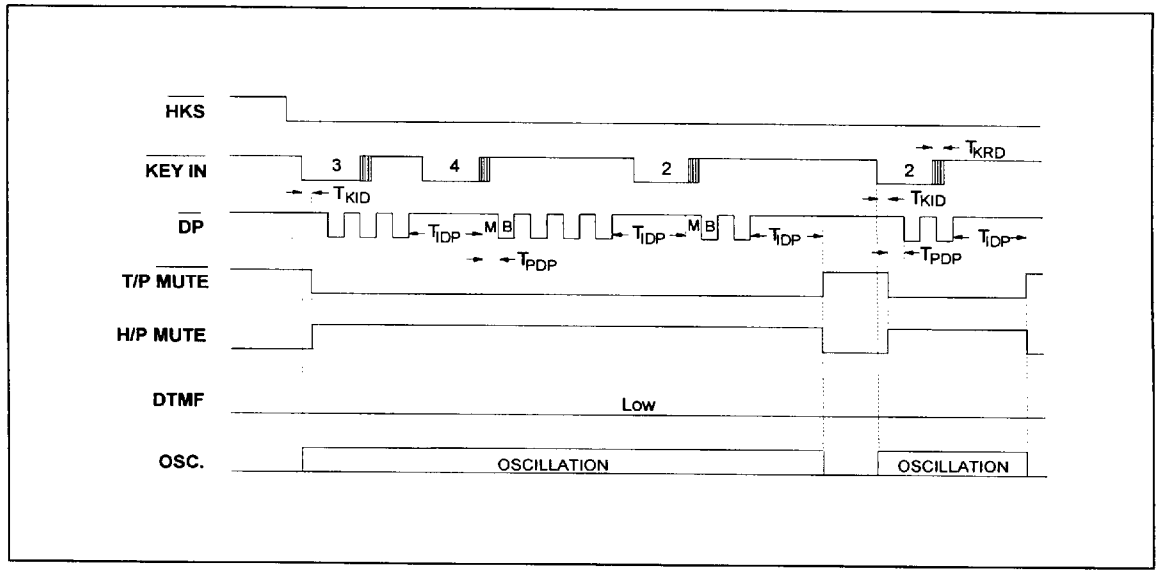

Figure 1(a). Normal Dialing Timing Diagram

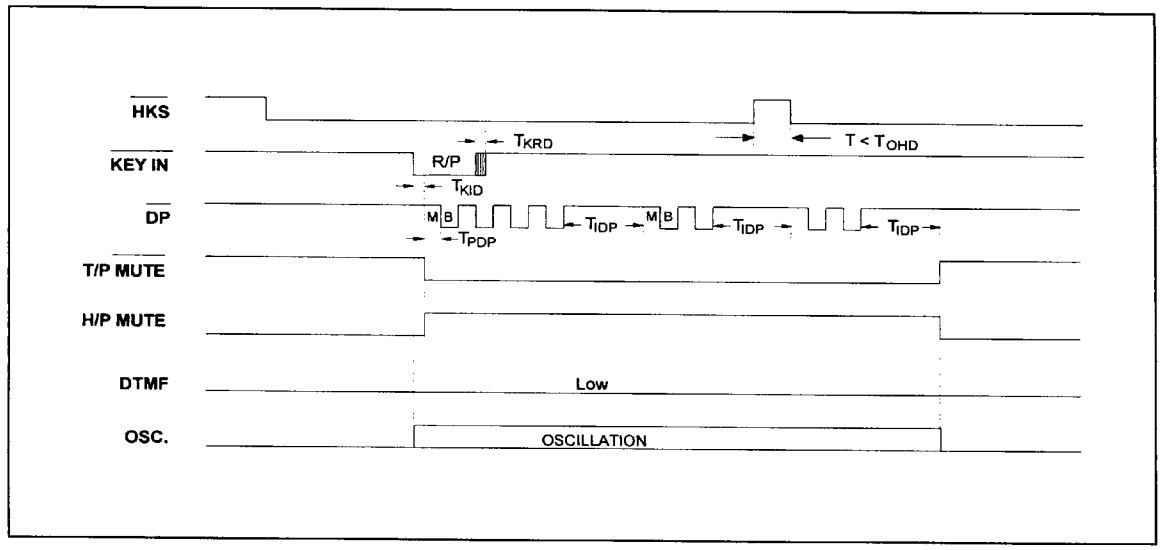

Figure 1(b) Pulse Mode Auto Dialing Timing Diagram

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