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MOS FIELD EFFECT POWER TRANSISTOR

2SK1954, 2SK1954-Z

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

The 2SK1954 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 0.65 \Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 2 \text{ A}$)
- Low C_{iss} $C_{iss} = 300 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DS}	180	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current (DC)	$I_D(\text{DC})$	± 4.0	A
Drain Current (pulse)	$I_D(\text{pulse})^*$	± 16	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T1}	20	W
Total Power Dissipation ($T_a = 25^\circ\text{C}$)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to $+150$	$^\circ\text{C}$
Single Avalanche Current	I_{AS}^{**}	4.0	A
Single Avalanche Energy	E_{AS}^{**}	44.3	mJ

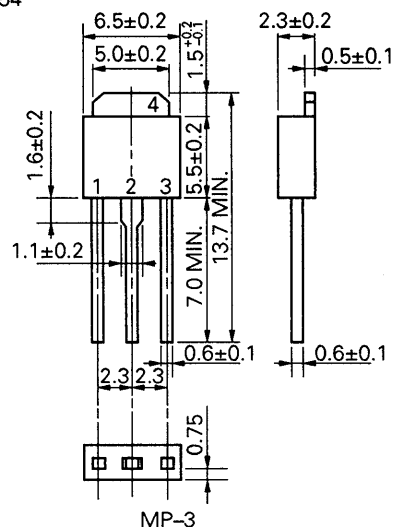
* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

** Starting $T_{ch} = 25^\circ\text{C}$, $R_\theta = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0$

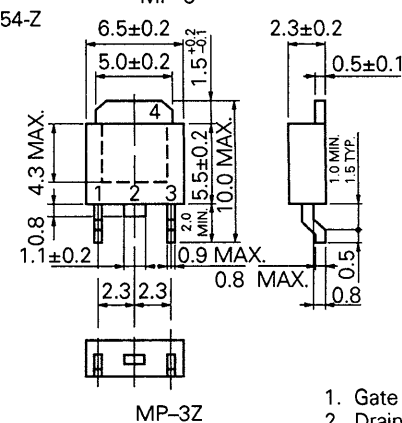
PACKAGE DIMENSIONS

(in millimeters)

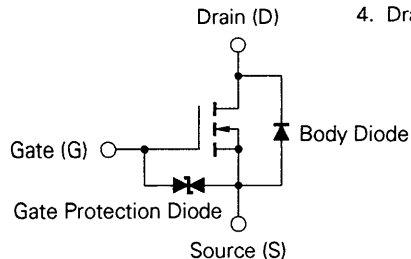
2SK1954



2SK1954-Z



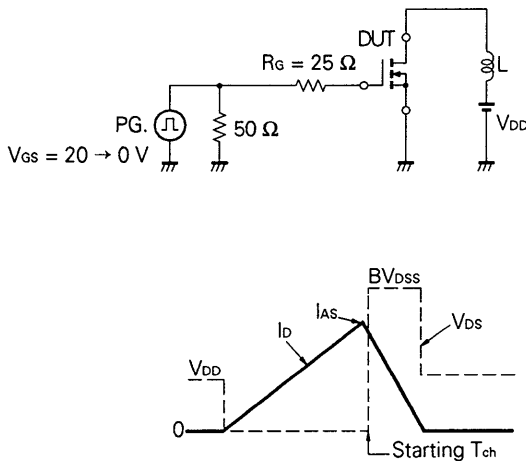
1. Gate
2. Drain
3. Source
4. Drain (Fin)



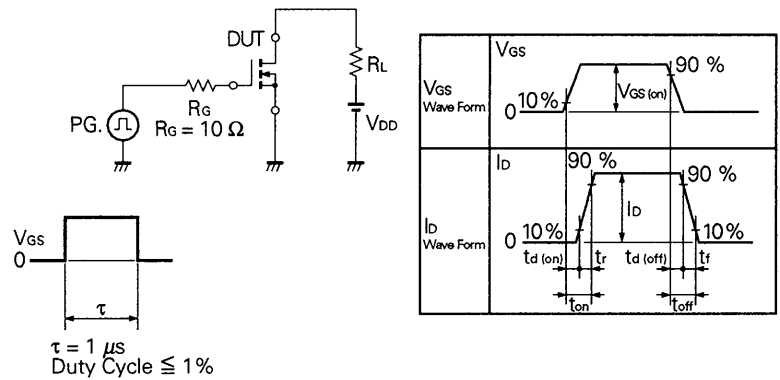
ELECTRICAL CHARACTERISTICS ($T_a = 25\text{ }^{\circ}\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		0.52	0.65	Ω	$V_{GS} = 10\text{ V}$, $I_D = 2.0\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.0		4.0	V	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	0.5			S	$V_{DS} = 10\text{ V}$, $I_D = 2.0\text{ A}$
Drain Leakage Current	I_{DSS}			100	μA	$V_{DS} = 180\text{ V}$, $V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0$
Input Capacitance	C_{iss}		300		pF	$V_{DS} = 10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$
Output Capacitance	C_{oss}		170		pF	
Reverse Transfer Capacitance	C_{rss}		50		pF	
Turn-On Delay Time	$t_{d(on)}$		9		ns	$V_{GS} = 10\text{ V}$ $V_{DD} = 100\text{ V}$ $I_D = 2.0\text{ A}$, $R_G = 10\text{ }\Omega$ $R_L = 50\text{ }\Omega$
Rise Time	t_r		10		ns	
Turn-Off Delay Time	$t_{d(off)}$		28		ns	
Fall Time	t_f		12		ns	
Total Gate Charge	Q_G		10		nC	$V_{GS} = 10\text{ V}$ $I_D = 4.0\text{ A}$ $V_{DD} = 140\text{ V}$
Gate to Source Charge	Q_{GS}		2.3		nC	
Gate to Drain Charge	Q_{GD}		4.7		nC	
Diode Forward Voltage	$V_{F(S-D)}$		0.9		V	$I_F = 4.0\text{ A}$, $V_{GS} = 0$
Reverse Recovery Time	t_{rr}		180		ns	$I_F = 4.0\text{ A}$ $di/dt = 50\text{ A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}		0.5		μC	

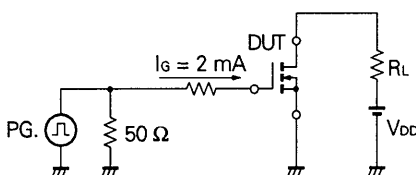
Test Circuit 1: Avalanche Capability



Test Circuit 2: Switching Time

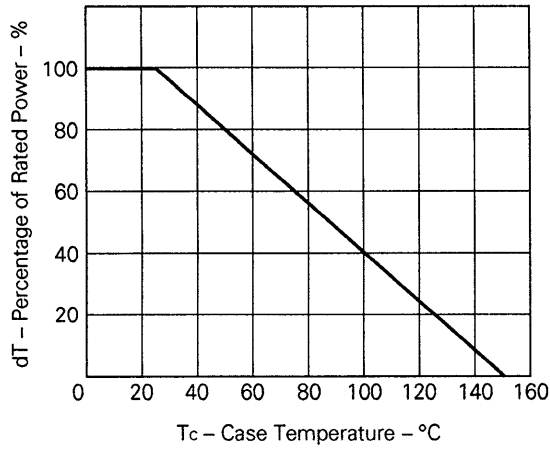


Test Circuit 3: Gate Charge

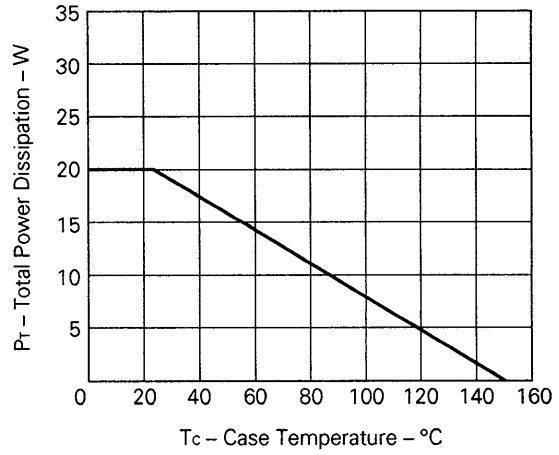


TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

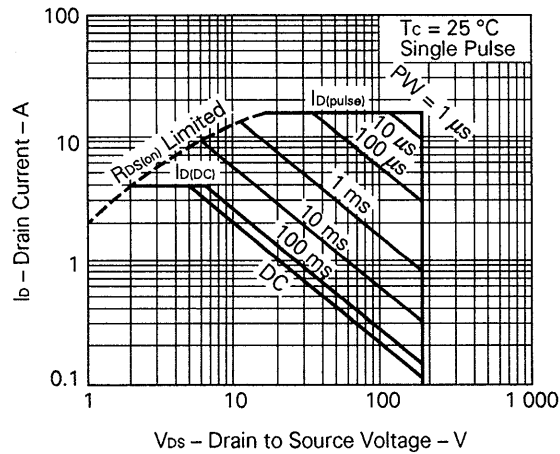
DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA



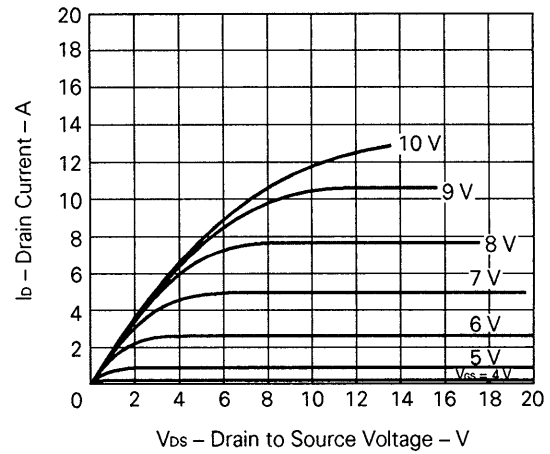
TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE



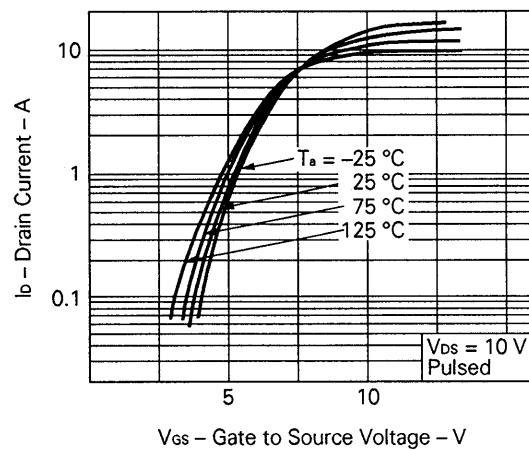
FORWARD BIAS SAFE OPERATING AREA

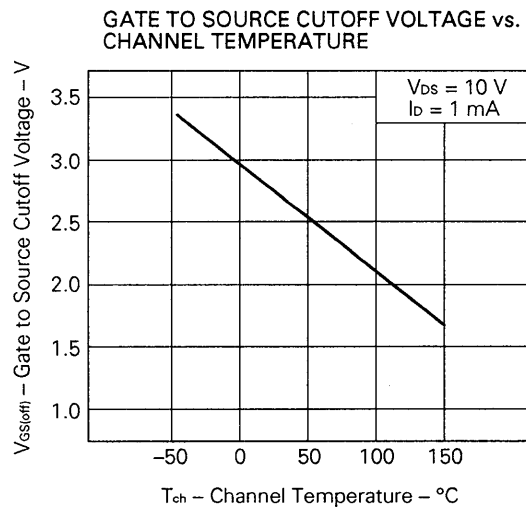
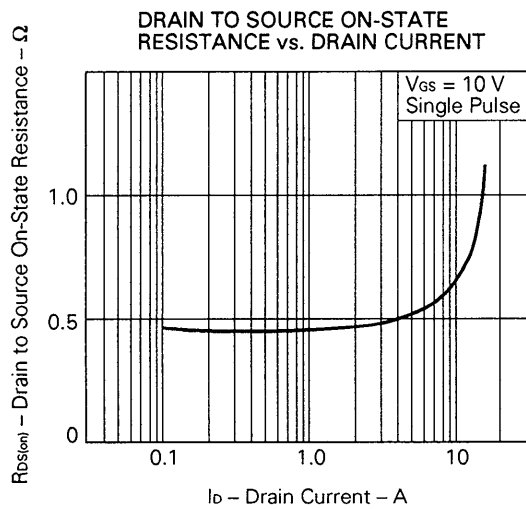
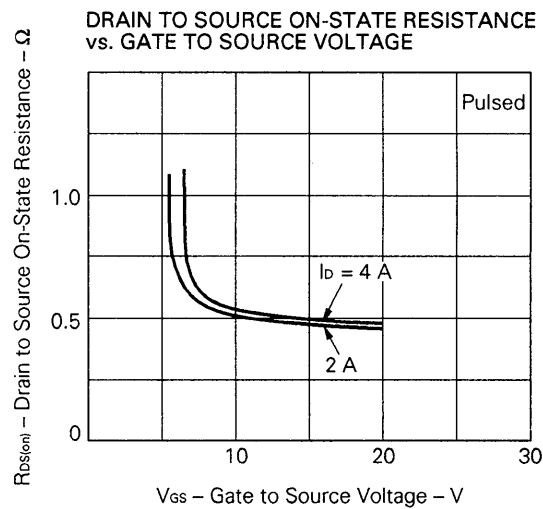
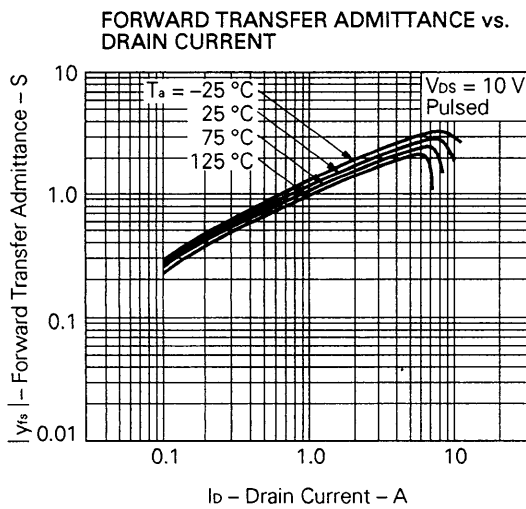
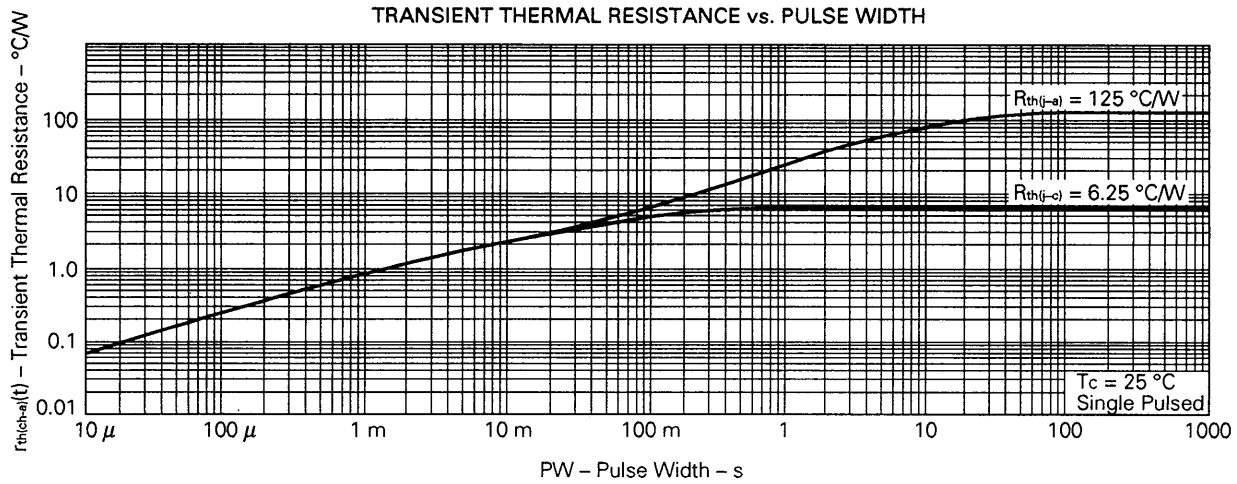


DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

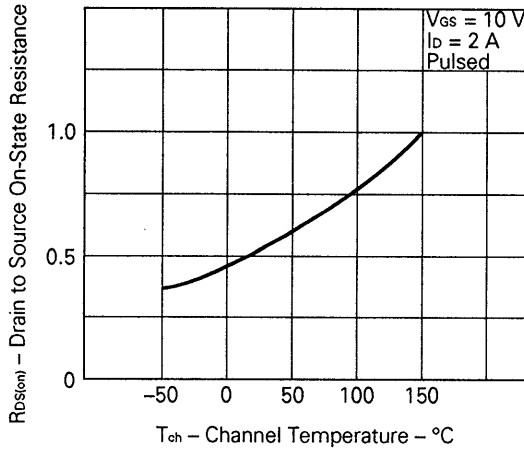


TRANSFER CHARACTERISTICS

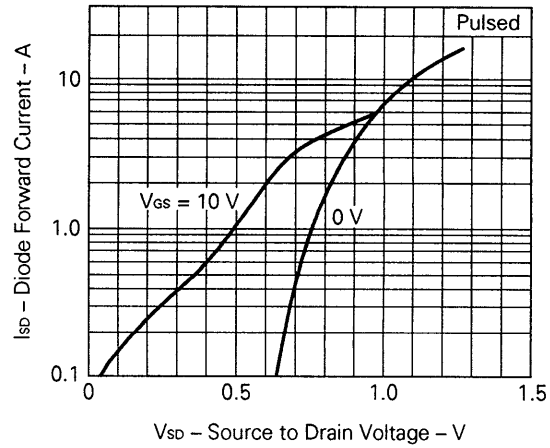




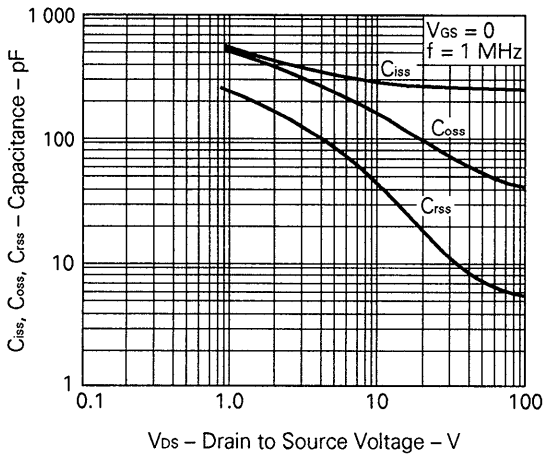
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



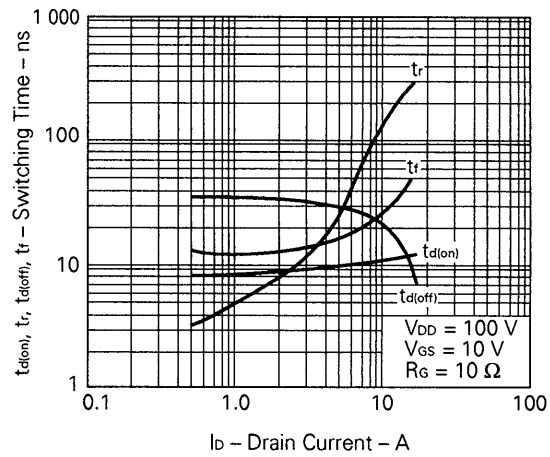
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



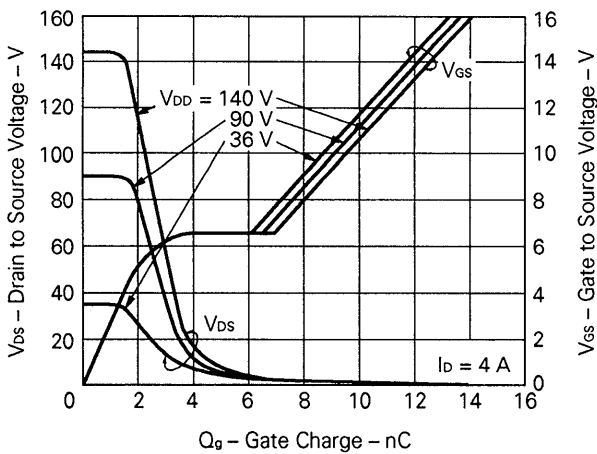
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



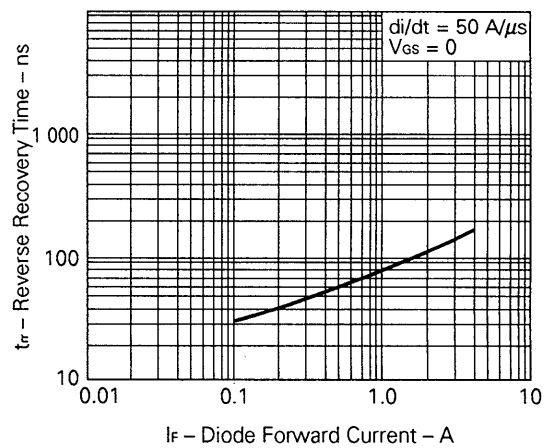
SWITCHING CHARACTERISTICS



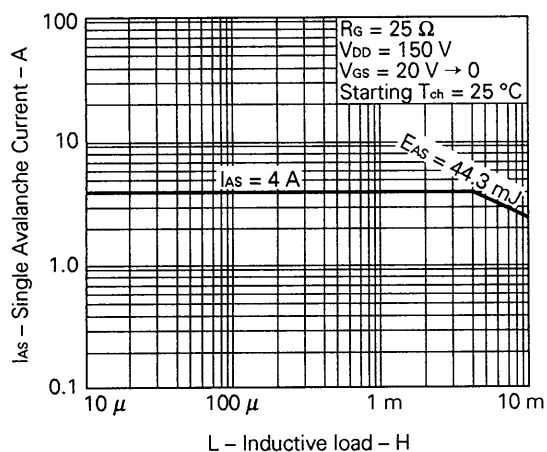
DYNAMIC INPUT CHARACTERISTICS



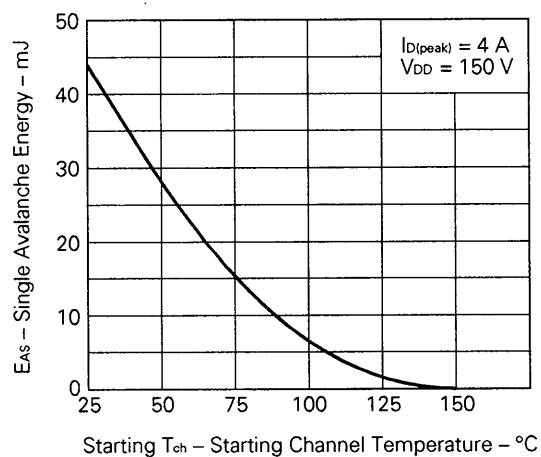
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs.
STARTING CHANNEL TEMPERATURE



Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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