MM1103 1024-bit fully decoded dynamic random access read/write memory

general description

The MM1103 fully decoded dynamic 1024 word x 1 bit per word read/write random access memory is a monolithic MOS integrated circuit using silicon gate low threshold technology. This device provides a non-destructive read out memory cell with chip enable for easy selection when many outputs are "OR"ed. Low power is achieved by the use of dynamic logic and power dissipation occurs primarily during precharge. The MM1103 is used for main memory applications where large bit storage, high performance and low cost are important.

- Refresh cycle — 2 ms
- Fully decoded
- Easy memory expansion — Chip enable input
- Device protection — All I/O lines have protection against static charge
- "OR"ing output capability
- Low power dissipation — 250 mW
- Small package size — 18 pin DIP

features

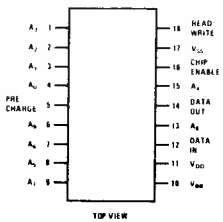
- Fast access time — 300 ns max
- Fast cycle time — 480 ns read cycle, 580 ns write cycle

applications

- Mainframe memory
- Large buffer memory

connection diagram

Dual-In-Line Package



TOP VIEW

absolute maximum ratings

All Input or Output Voltages With Respect to the Most Positive Supply Voltage V_{SS}	+0.3V to −25V
Supply Voltage V_{DD} and V_{BB} With Respect to V_{SS}	+0.3V to −25V
Power Dissipation at Room Temperature	500 mW
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−65°C to +160°C
Lead Temperature (Soldering, 10 sec)	300°C

dc operating characteristics 16 & 19.5

T_A within operating temperature range, V_{SS} = 16 ± 1V, (V_{BB} − V_{SS}) = 3V to 4V, V_{DD} = 0V unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	U
Input Load Current (All Input Pins) (I_{LI})	V_{IN} = 0V			1	
Output Leakage Current (I_{LO})	V_{OUT} = 0V			1	
V_{BB} Supply Current (I_{BB})				100	
Average Supply Current ($I_{DD\,AV}$)	Cycle Time = 580 ns precharge width = 240 ns, T_A = 25°C			20	
Standby Supply Current	Precharge = V_{SS}, Chip Enable = V_{SS}, T_A = 25°C			100	
Input LOW Voltage (V_{IL})		V_{SS} − 17		V_{SS} − 15	
Input HIGH Voltage (V_{IH})		V_{SS} − 1		V_{SS} + 1	
Output HIGH Current (I_{OH})	T_A = 25°C R_L = 100Ω	600		4000	
Output HIGH Voltage (V_{OH})	T_A = 25°C R_L = 100Ω	60		400	

ac operating characteristics T_A = 0°C to 70°C, V_{SS} = 16 ± 5%, (V_{BB} − V_{SS}) = 3.0V to 4.0V, V_{DD} = 0V

READ, WRITE, AND READ/WRITE CYCLE

PARAMETER	CONDITIONS	MIN	TYP	MAX	U
Time Between Refresh (t_{REF})				2	
Address to Cenable Set Up Time (t_{AC}) Note 1		115			
Cenable to Address Hold Time (t_{CA})		20			
Precharge to Cenable Delay (t_{PC}) Note 1		125			
Precharge & Cenable Overlap, LOW (t_{OV1})		25		75	
Cenable to Precharge Delay (t_{CP})		85			
Precharge & Cenable Overlap, HIGH (t_{OVH})				140	

READ CYCLE

PARAMETER	CONDITIONS	MIN	TYP	MAX	U
Read Cycle (t_{RC}) Note 1	$t_{ACmin} + t_{OV1min} + t_{POmax} + 2t_T$; t_T = 20 ns, C_{LOAD} = 100 pF, R_{LOAD} = 100Ω, V_{REF} = 40 mV	480			
Precharge to End of Cenable (t_{POV})		165		500	
End of Precharge to Output Delay (t_{PO})				120	
Address to Output Access (t_{ACC1}) Note 1		300			
Precharge to Output Access (t_{ACC2}) Note 1	$t_{PCmin} + t_{OV1min} + t_{POmax} + 2t_T$	310			

WRITE OR READ/WRITE CYCLE

PARAMETER	CONDITIONS	MIN	TYP	MAX	U
Write Cycle (t_{WC}) Note 1	t_T = 20 ns	580			
Read/Write Cycle (t_{RWC}) Note 1	t_T = 20 ns	580			
Precharge to Read/Write Delay (t_{PW})		165		500	
Read/Write Pulse Width (t_{WP})		80			
Read/Write Set Up Time (t_W)		80			
Data Set Up Time (t_{DW})		105			
Data Hold Time (t_{DH})		10			
End of Precharge to Output Delay (t_{PO})	C_{LOAD} = 100 pF, R_{LOAD} = 100Ω, V_{REF} = 40 mV			120	
Time to Next Precharge (t_P)		0			

Note 1. These times will degrade by 40 ns (worst case) if the maximum values for V_{IL} (for precharge, cenable and read/write inputs) go to V_{SS} − 14.2V @ 0°C and V_{SS} − 14.5V @ 70°C

ac operating characteristics (con't)

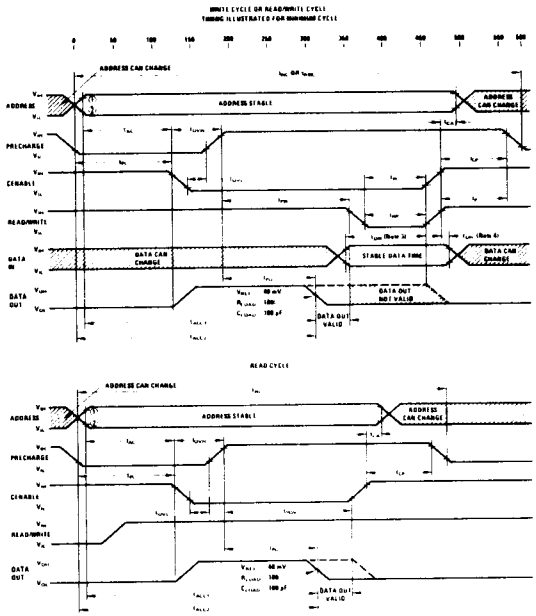
*CAPACITANCE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Address Capacitance (C_{ADD})	V_{IN} = V_{CC}		5	7	pF
Precharge Capacitance (C_{PRE})	V_{IN} = V_{CC}		15	18	pF
Cenable Capacitance (C_{CE})	V_{IN} = V_{CC}		15	25	pF
Read/Write Capacitance ($C_{R/W}$)	V_{IN} = V_{CC}		11	15	pF
Data Input Capacitance (C_{IN1})	Cenable = 0V; V_{IN} = V_{CC}		4	5	pF
Data Input Capacitance (C_{IN2})	Cenable = V_{CC}; V_{IN} = V_{CC}		2	4	pF
Data Output Capacitance (C_{OUT})	V_{OUT} = 0V		2	3	pF

f = 1 MHz; All Unused Pins Are at AC GND

*This parameter is periodically sampled and is not 100% tested. They are measured at worst case operating conditions. Capacitance are for plastic packages only.

switching time waveforms



Note 1 V_{DD} + 2V t_t is defined as the transitions between these two points

Note 2 V_{SS} - 2V t_t is defined as the transitions between these two points

Note 3 t_{DH} is referenced to point 2 of the rising edge of cenable or read/write whichever occurs first

Note 4 t_{DH} is referenced to point 3 of the rising edge of cenable or read/write whichever occurs first

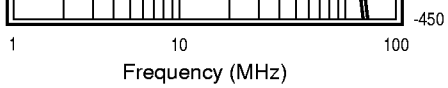


Figure 3: Channel Matching

The CLC417's channel-to-channel isolation is better than 70dB for input frequencies of 4MHz. Input referred crosstalk vs. frequency is illustrated in Figure 4.

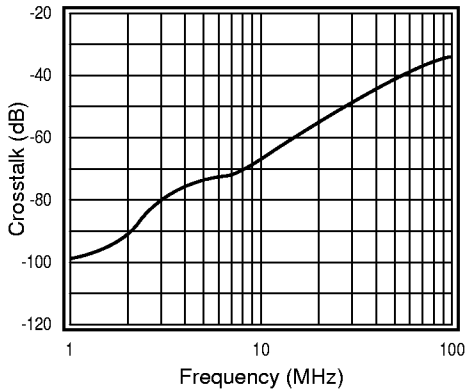


Figure 4: Input Referred Crosstalk vs. Frequency

Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC417 will improve stability. The ***R_s vs. Capacitive Load*** plot, in the ***Typical Performance*** section, gives the recommended series resistance value for optimum flatness at various capacitive loads.

Power Dissipation

The power dissipation of an amplifier can be described in two conditions:

- Quiescent Power Dissipation - P_Q (No Load Condition)
- Total Power Dissipation - P_T (with Load Condition)

The following steps can be taken to determine the power consumption for each CLC417 amplifier:

$$P = \frac{(175° - Tamb)}{\theta_{JA}}$$

where: T_{amb} = Ambient temperature (°C)
θ_{JA} = Thermal resistance, from ju
ambient, for a given packag

Layout Considerations

A proper printed circuit layout is essenti
high frequency performance. Natio
evaluation boards for the CLC417 (CLC
CLC730036 - SOIC) and suggests their
for high frequency layout and as an aid fo
and characterization.

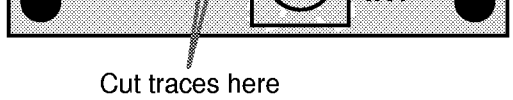
Supply bypassing is required for best per
bypass capacitors provide a low imp
current path at the supply pins. They al
frequency filtering on the power supply
layout factors play a major role in h
performance. The following are recomme
for high frequency layout:

1. Include 6.8μF tantalum and 0.1μF
capacitors on both supplies.
2. Place the 6.8μF capacitors within
of the power pins.
3. Place the 0.1μF capacitors less th
inches from the power pins.
4. Remove the ground plane near th
and output pins to reduce parasiti
capacitance.
5. Minimize all trace lengths to reduc
inductances.

Additional information is included in the e
literature.

Special Evaluation Board Considerati

To optimize off-isolation of the CLC417, c
on both the 730038 and 730036 evaluatio
cut minimizes capacitive feedthrough bet
and output. Figure 5 indicates th
recommended to improve off-isolation.



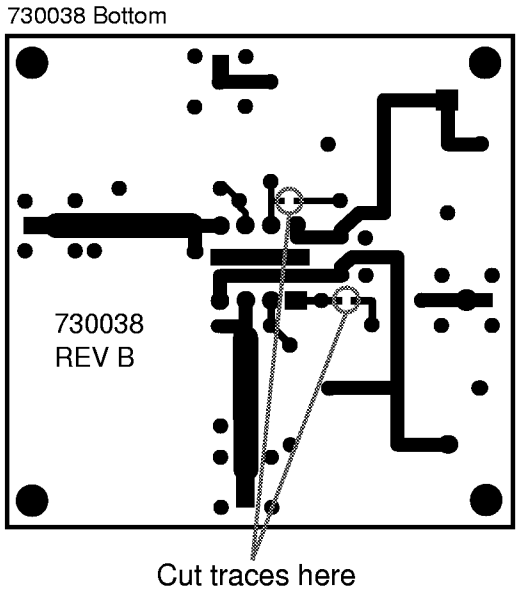


Figure 5: Optional Evaluation Board Alterations

SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for National's monolithic amplifiers that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The ***readme*** file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for National's Op Amps, contains schematics and a reproduction of the ***readme*** file.

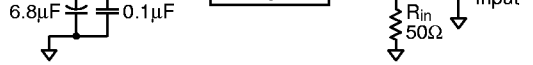


Figure 6: Typical Cable Driver

Single to Differential Line Driver

The topology in Figure 7 accomplishes a sing
differential conversion with no external co
With this configuration, the value of Vin is lir
common mode input range of the CLC417.

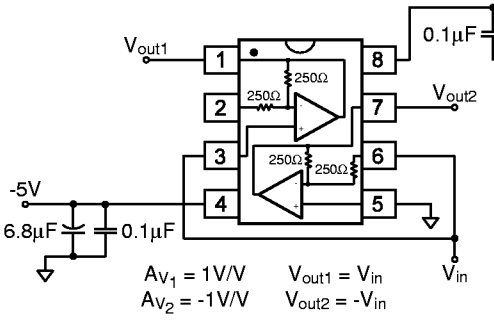


Figure 7: Single to Differential Line D