MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC68HC11E20

Technical Summary
8-Bit Microcontroller

The MC68HC11E20 high-performance microcontroller unit (MCU) is an enhanced member of the M68HC11 E series of microcontrollers. These devices combine a multiplexed bus with highly sophisticated on-chip peripheral functions and are characterized by high speed and low power consumption. Their fully static design allows these devices to operate at frequencies from 3 MHz to dc.

This document contains information concerning both the ROM-based (MC68HC11E20) and the EPROM-based (MC68HC711E20) versions of this MCU. ROM/EPROM refers to ROM for ROM-based devices and refers to EPROM for EPROM-based devices. Custom-ROM devices have a ROM array that is programmed at the factory to customer specifications. The diagrams for these devices are combined also and differences are noted where necessary.

Features

- M68HC11 CPU
- 20 Kbytes of On-Chip ROM or EPROM
- 512 Bytes of On-Chip Electrically-Erasable Programmable Read-Only Memory (EEPROM)
- 768 Bytes of On-Chip RAM, All Saved During Standby
- Power Saving STOP and WAIT Modes
- Multiplexed Address/Data Bus
- 16-Bit Timer System
    - Three Input Capture (IC) Channels
    - Four Output Compare (OC) Channels
    - One Additional Channel, Software Selectable as Fourth IC or Fifth OC
- 8-Bit Pulse Accumulator
- Real-Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog
- Block Protect on EEPROM for Added Security
- Asynchronous Nonreturn to Zero (NRZ) Serial Communications Interface (SCI)
- Synchronous Serial Peripheral Interface (SPI)
- Eight-Channel 8-Bit Analog-to-Digital (A/D) Converter
- Five Input/Output (I/O) Ports (38 Pins)
    - 16 Bidirectional Pins
    - 11 Input Only Pins
    - 11 Output Only Pins
- Available in 52-Pin Plastic Leaded Chip Carrier (PLCC), 52-Pin Windowed Ceramic Leaded Chip Carrier (CLCC), and 64-Pin Plastic Quad Flat Pack (QFP)

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Standard Device Ordering Information

Package	Description	CONFIG	Frequency	Temperature	MC Order Number
64-Pin QFP	OTPROM	$0F	2 MHz	− 40° to + 85° C	MC68HC711E20CFU2
				− 40° to + 105° C	MC68HC711E20VFU2
				− 40° to + 125° C	MC68HC711E20MFU2
			3 MHz	0° to + 70° C	MC68HC711E20FU3
				− 40° to + 85° C	MC68HC711E20CFU3
52-Pin PLCC	OTPROM	$0F	2 MHz	− 40° to + 85° C	MC68HC711E20CFN2
				− 40° to + 105° C	MC68HC711E20VFN2
				− 40° to + 125° C	MC68HC711E20MFN2
			3 MHz	0° to + 70° C	MC68HC711E20FN3
				− 40° to + 85° C	MC68HC711E20CFN3
52-Pin CLCC (Windowed)	EPROM	$0F	2 MHz	− 40° to + 85° C	MC68HC711E20CFS2
				− 40° to + 105° C	MC68HC711E20VFS2
				− 40° to + 125° C	MC68HC711E20MFS2
			3 MHz	0° to + 70° C	MC68HC711E20FS3
				− 40° to + 85° C	MC68HC711E20CFS3

Custom ROM Device Ordering Information

Package	Description	Frequency	Temperature	MC Order Number
64-Pin QFP	Custom ROM	2 MHz	− 40° to + 85° C	MC68HC11E20CFU2
			− 40° to + 105° C	MC68HC11E20VFU2
			− 40° to + 125° C	MC68HC11E20MFU2
		3 MHz	0° to + 70° C	MC68HC11E20FU3
			− 40° to + 85° C	MC68HC11E20CFU3
52-Pin PLCC	Custom ROM	2 MHz	− 40° to + 85° C	MC68HC11E20CFN2
			− 40° to + 105° C	MC68HC11E20VFN2
			− 40° to + 125° C	MC68HC11E20MFN2
		3 MHz	0° to + 70° C	MC68HC11E20FN3
			− 40° to + 85° C	MC68HC11E20CFN3

MC68HC(7)11E20

Top pins (64–49): PA1/IC2, PA2/IC1, PA3/OC5/IC4/OC1, NC, NC, PA4/OC4/OC1, PA5/OC3/OC1, PA6/OC2/OC1, PA7/PAI/OC1, V_DD, PD5/SS, PD4/SCK, PD3/MOSI, PD2/MISO, PD1/TxD, V_SS

Left pins (1–16):
1 PA0/IC3
2 NC
3 NC
4 NC
5 PB7/ADDR15
6 PB6/ADDR14
7 PB5/ADDR13
8 PB4/ADDR12
9 PB3/ADDR11
10 PB2/ADDR10
11 PB1/ADDR9
12 PB0/ADDR8
13 PE0/AN0
14 PE4/AN4
15 PE1/AN1
16 PE5/AN5

Right pins (48–33):
48 NC
47 PD0/RxD
46 IRQ
45 XIRQ/V_PPE*
44 NC
43 RESET
42 PC7/ADDR7/DATA7
41 PC6/ADDR6/DATA6
40 PC5/ADDR5/DATA5
39 PC4/ADDR4/DATA4
38 PC3/ADDR3/DATA3
37 PC2/ADDR2/DATA2
36 PC1/ADDR1/DATA1
35 NC
34 PC0/ADDR0/DATA0
33 XTAL

Bottom pins (17–32): PE2/AN2, PE6/AN6, PE3/AN3, PE7/AN7, V_RL, V_RH, V_SS, V_SS, MODB/V_STBY, NC, MODA/LIR, STRA/AS, E, STRB/R/W, EXTAL, NC

* V_PPE APPLIES ONLY TO DEVICES WITH EPROM.

E20 64-PIN QFP

Pin Assignments for 64-Pin Quad Flat Pack

Pin Assignments for 52-Pin PLCC/CLCC
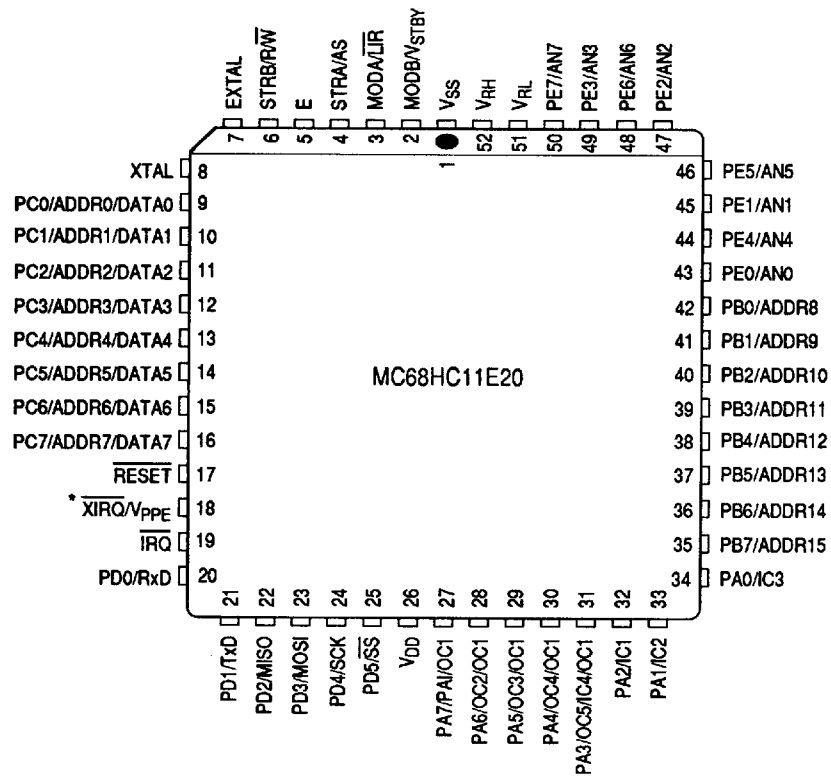
* V_PPE APPLIES ONLY TO DEVICES WITH EPROM.

E20 52-PIN PLCC

■ 6367248 0137126 T6T ■

MODA/ $\overline{LIR}$ MODB/ V_{STBY} XTAL EXTAL E $\overline{IRQ}$ $\overline{XIRQ}/V_{PPE}$* $\overline{RESET}$

MODE CONTROL

OSC
CLOCK LOGIC

INTERRUPT LOGIC

20 KBYTES ROM/EPROM

COP

TIMER SYSTEM

PERIODIC INTERRUPT

M68HC11 CPU

512 BYTES EEPROM

768 BYTES RAM

PULSE ACCUMULATOR

PAI
OC2
OC3
OC4
OC5/IC4/OC1
IC1
IC2
IC3

BUS EXPANSION ADDRESS   ADDRESS/DATA   R/W   AS

SERIAL PERIPHERAL INTERFACE SPI

SERIAL COMMUNICATION INTERFACE SCI

V_{DD}
V_{SS}

STROBE AND HANDSHAKE PARALLEL I/O   STRB STRA

$\overline{SS}$ SCK MOSI MISO   TxD RxD

V_{RH}
V_{RL}

A/D CONVERTER

CONTROL

CONTROL

PORT A   PORT B   PORT C   PORT D   PORT E

PA7/PAI
PA6/OC2
PA5/OC3
PA4/OC4
PA3/OC5/IC4/OC1
PA2/IC1
PA1/IC2
PA0/IC3

PB7/ADDR15
PB6/ADDR14
PB5/ADDR13
PB4/ADDR12
PB3/ADDR11
PB2/ADDR10
PB1/ADDR9
PB0/ADDR8

PC7/ADDR7/DATA7
PC6/ADDR6/DATA6
PC5/ADDR5/DATA5
PC4/ADDR4/DATA4
PC3/ADDR3/DATA3
PC2/ADDR2/DATA2
PC1/ADDR1/DATA1
PC0/ADDR0/DATA0

STRB/R/W
STRA/AS

PD5/$\overline{SS}$
PD4/SCK
PD3/MOSI
PD2/MISO

PD1/TxD
PD0/RxD

PE7/AN7
PE6/AN6
PE5/AN5
PE4/AN4
PE3/AN3
PE2/AN2
PE1/AN1
PE0/AN0

* V_{PPE} APPLIES ONLY TO DEVICES WITH EPROM.

E20 BLOCK

MC68HC11E20 Block Diagram

Operating Modes

The MC68HC11E20 has four modes of operation. These modes directly affect the address space and the memory map differs for each of them. Refer to the memory map diagram.

Single-Chip Mode

In single-chip operating mode, the MC68HC11E20 is a stand-alone microcontroller with no external address or data bus. Although the CPU can access the full 64-Kbyte address space, addressing is limited to on-chip resources. Portions of the 64-Kbyte space that are not occupied by the on-chip resources cannot be utilized. Refer to the memory map diagram.

Bootstrap Mode

Bootstrap mode is a special variation of the single-chip mode. Bootstrap mode allows special-purpose programs to be entered into internal RAM. When boot mode is selected at reset, a small bootstrap ROM becomes present in the memory map. Reset and interrupt vectors are located in this ROM at $BFC0–$BFFF. The bootstrap ROM contains a small program which initializes the SCI and allows the user to download a program of up to 768 bytes into on-chip RAM. After a four-character delay, or after receiving the character for address $02FF, control passes to the loaded program at $0000. Refer to the memory map diagram.

Special Test Mode

Special test mode is used primarily for factory testing. In this operating mode, ROM/EPROM is removed from the address space and vectors are located at $BFC0–$BFFF.

Expanded Operating Mode

In expanded operating mode, the MCU can access the full 64-Kbyte address space. The space includes the same on-chip memory addresses used for single-chip mode as well as addresses for external peripherals and memory devices. The expansion bus is made up of ports B and C, and control signals AS and R/W. The R/W (read/write) and AS (address strobe) allow the low-order address and the 8-bit data bus to be multiplexed on the same pins. During the first half of each bus cycle address information is present. During the second half of each bus cycle the pins become the bidirectional data bus. AS is an active-high latch enable signal for an external address latch. Address information is allowed through the transparent latch while AS is high and is latched when AS drives low. The address, R/W, and AS signals are active and valid for all bus cycles, including accesses to internal memory locations. The E-clock is used to enable external devices to drive data onto the internal data bus during the second half of a read bus cycle (E clock high). R/W controls the direction of data transfers. R/W drives low when data is being written to the internal data bus. R/W will remain low during consecutive data bus write cycles, such as when a double-byte store occurs. Notice that the write enable signal for an external memory is the NAND of the E clock and the inverted R/W signal. Refer to the example diagram of address and data demultiplexing.
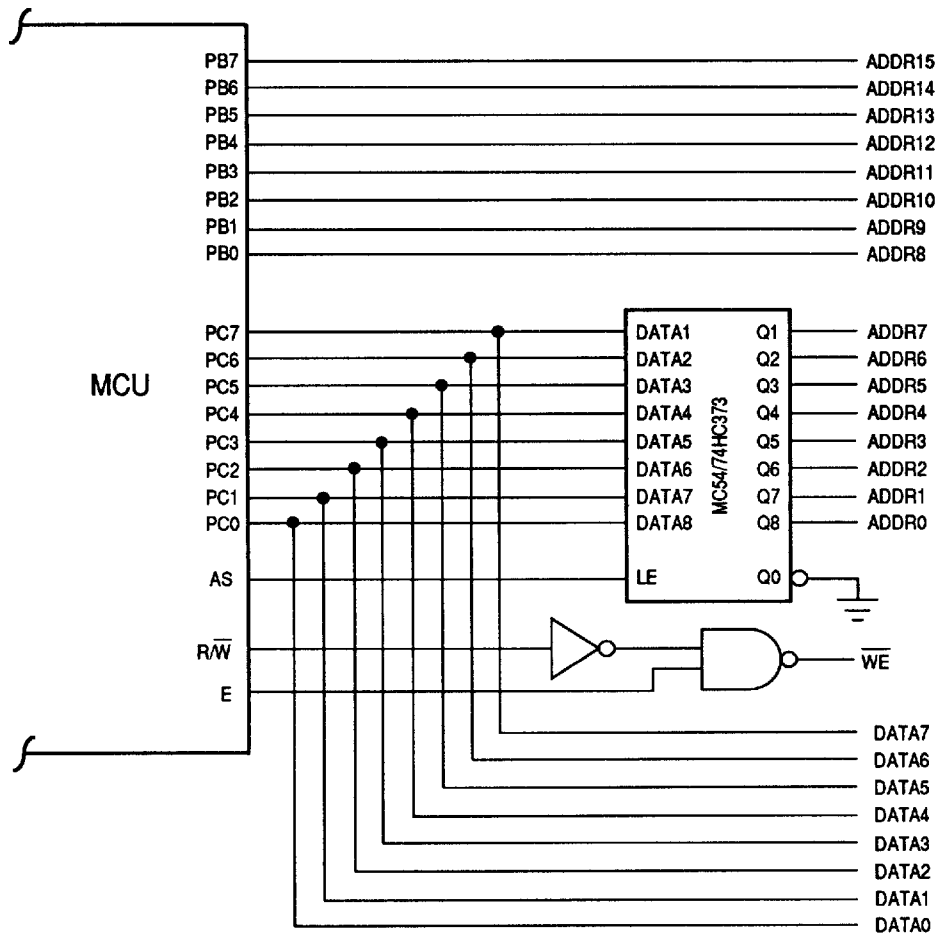
ADDR/DATA DEMUX

Address/Data Demultiplexing

Mode Selection

Operating modes are selected by a combination of logic levels applied to two input pins (MODA and MODB) during reset. The logic level present (at the rising edge of reset) on these inputs is reflected in bits in the HPRIO register. After reset, the operating mode may be changed according to the table contained in the following description of the HPRIO register.

The function of internal read visibility/not E is determined by the state of the IRVNE bit and the mode selected at reset. When enabled, internal read visibility (IRV) causes the data from internal reads to be driven out the data bus. The user must be cautioned that even though the R/W line suggests that the data bus is in a high-impedance state, data will be driven out each time an internal read occurs. The not E clock (NE) function of this bit determines whether the E clock is on or off. Refer to the description of IRVNE in HPRIO register.

MC68HC11E20
MC68HC11E20TS/D   ■ 6367248 0137129 779 ■   MOTOROLA
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HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous   **$103C**

Bit 7	6	5	4	3	2	1	Bit 0
RBOOT*	SMOD*	MDA*	IRVNE*	PSEL3	PSEL2	PSEL1	PSEL0

RESET:								
0	0	0	0	0	1	1	0	Single Chip
0	0	1	0	0	1	1	0	Expanded
1	1	0	0	0	1	1	0	Bootstrap
0	1	1	0	0	1	1	0	Special Test

*The reset values of RBOOT, SMOD, and MDA depend on the mode selected at power up.

RBOOT — Read Bootstrap ROM

Valid only when SMOD is set (bootstrap or special test mode). Can only be written in special modes.

0 = Bootloader ROM disabled and not in map

1 = Bootloader ROM enabled and in map at $BE00–$BFFF

SMOD and MDA — Special Mode Select and Mode Select A

The initial value of SMOD is the **inverse** of the logic level present on the MODB pin at the rising edge of reset. The initial value of MDA equals the logic level present on the MODA pin at the rising edge of reset. These two bits can be read at any time. They can be written anytime in special modes. MDA can only be written once in normal modes. SMOD cannot be set once it has been cleared.

Inputs		Mode	Latched at Reset	
MODB	MODA		SMOD	MDA
1	0	Single Chip	0	0
1	1	Expanded	0	1
0	0	Bootstrap	1	0
0	1	Special Test	1	1

IRVNE — Internal Read Visibility/Not E

IRVNE can be written once in any mode. In expanded modes, IRVNE determines whether IRV is on or off. In special test mode, IRVNE is reset to one. In all other modes, IRVNE is reset to zero.

0 = No internal read visibility on external bus

1 = Data from internal reads is driven out the external data bus.

In single-chip modes this bit determines whether the E clock drives out from the chip.

0 = E is driven out from the chip.

1 = E pin is driven low. Refer to the following table.

Mode	IRVNE Out of Reset	E Clock Out of Reset	IRV Out of Reset	IRVNE Affects Only	IRVNE Can Be Written
Single Chip	0	On	Off	E	Once
Expanded	0	On	Off	IRV	Once
Bootstrap	0	On	Off	E	Once
Special Test	1	On	On	IRV	Once

PSEL[3:0] — Priority Select Bits [3:0]

Refer to **Resets and Interrupts**.

On-Chip Memory

The MC68HC11E20 has 768 bytes RAM, 512 bytes EEPROM, and 20 Kbytes ROM. The MC68HC711E20 has EPROM replacing ROM. The following paragraphs describe the memory systems of these two MCUs.

Memory Map and Register Block

The INIT and CONFIG registers control the presence and location of the registers, RAM, EEPROM, and ROM/EPROM in the 64 Kbyte CPU address space. The 64-byte register block originates at $1000 after reset and can be placed at any 4K boundary ($x000) by writing an appropriate value to the INIT register. The INIT register can be written only in the first 64 cycles after reset. Refer to the memory map diagram.

$0000					0000	768 BYTES RAM
	EXT		EXT		02FF	(CAN BE REMAPPED TO ANY 4K PAGE BY THE INIT REGISTER)
$1000					1000	64-BYTE REGISTER BLOCK
	EXT		EXT		103F	(CAN BE REMAPPED TO ANY 4K PAGE BY THE INIT REGISTER)
$9000					9000	8 KBYTES ROM/EPROM
	EXT		EXT		AFFF	
$B600					B600	512 BYTES EEPROM
	EXT		EXT		B7FF	
					BF00	BOOT ROM
					BFFF	
$D000					D000	12 KBYTES ROM/EPROM
$FFFF					FFFF	
	SINGLE CHIP	EXPANDED	BOOTSTRAP	SPECIAL TEST		

BFC0 / BFFF SPECIAL MODES INTERRUPT VECTORS

FFC0 / FFFF NORMAL MODES INTERRUPT VECTORS

E20 MEM MAP

MC68HC11E20/MC68HC711E20 Memory Map

MC68HC11E20 Register and Control Bit Assignments (1 of 2)

The register block begins at $1000 out of reset and can be remapped to any 4K boundary.

	Bit 7	6	5	4	3	2	1	Bit 0	
$1000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$1001									Reserved
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC
$1003	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$1004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$1005	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0	PORTCL
$1006									Reserved
$1007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
$1008	—	—	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$1009	—	—	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
$100A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	—	—	—	CFORC
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	—	—	—	OC1M
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	—	—	—	OC1D
$100E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (High)
$100F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (Low)
$1010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (High)
$1011	Bit 7	6	5	4	3	2	1	Bit 0	TIC1 (Low)
$1012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (High)
$1013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (Low)
$1014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (High)
$1015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (Low)
$1016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1 (High)
$1017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (Low)
$1018	Bit 15	14	13	12	11	10	9	Bit 8	TOC2 (High)
$1019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (Low)
$101A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (High)
$101B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (Low)
$101C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (High)
$101D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (Low)
$101E	Bit 15	14	13	12	11	10	9	Bit 8	TI4/O5 (High)
$101F	Bit 7	6	5	4	3	2	1	Bit 0	TI4/O5 (Low)
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1

MC68HC11E20 Register and Control Bit Assignments (2 of 2)

Address	Bit 7	6	5	4	3	2	1	Bit 0	Register
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
$1022	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I	TMSK1
$1023	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F	TFLG1
$1024	TOI	RTII	PAOVI	PAII	—	—	PR1	PR0	TMSK2
$1025	TOF	RTIF	PAOVF	PAIF	—	—	—	—	TFLG2
$1026	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0	PACTL
$1027	Bit 7	6	5	4	3	2	1	Bit 0	PACNT
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
$1029	SPIF	WCOL	—	MODF	—	—	—	—	SPSR
$102A	Bit 7	6	5	4	3	2	1	Bit 0	SPDR
$102B	TCLR	SCP2	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD
$102C	R8	T8	—	M	WAKE	—	—	—	SCCR1
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE	—	SCSR
$102F	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SCDR
$1030	CCF	—	SCAN	MULT	CD	CC	CB	CA	ADCTL
$1031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$1032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$1033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$1034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4
$1035	—	—	—	PTCON	BPRT3	BPRT2	BPRT1	BPRT0	BPROT
$1036	MBE	—	ELAT	EXCOL	EXROW	T1	T0	PGM	EPROG*
$1037									Reserved
$1038									Reserved
$1039	ADPU	CSEL	IRQE	DLY	CME	—	CR1	CR0	OPTION
$103A	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
$103B	ODD	EVEN	—	BYTE	ROW	ERASE	EELAT	EEPGM	PPROG
$103C	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
$103E	TILOP	—	OCCR	CBYP	DISR	FCM	FCOP	TCON	TEST1
$103F	—	—	—	—	NOSEC	NOCOP	ROMON	EEON	CONFIG

* MC68HC711E20 only.

RAM

The 768 bytes of on-chip RAM are located at $0000 after reset. If RAM and registers are both mapped to the same 4K boundary, the register block starts at $x000, and RAM starts at $x040. In this case, registers overlap the first $3F RAM addresses and that portion of RAM becomes inaccessible. Remapping is accomplished by writing appropriate values to the INIT register.

When power is removed from the MCU, RAM contents may be preserved using the MODB/V_{STBY} pin. A 5-volt nominal power source applied to this pin protects all 768 bytes of RAM.

INIT — RAM and Register Mapping $103D

Bit 7	6	5	4	3	2	1	Bit 0
RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0

RESET: 0   0   0   0   0   0   0   0

Can be written only once in first 64 cycles out of reset in normal modes or at any time in special mode.

RAM[3:0] — Internal RAM Map Position
These bits determine the upper four bits of the RAM address. At reset RAM is mapped to $0000. Refer to the memory map diagram.

REG[3:0] — 128-Byte Register Block Map Position
These bits determine the upper four bits of the register space address. At reset registers are mapped to $1000. Refer to the memory map diagram.

ROM/EPROM

The MC68HC711E20 has 20 Kbytes of ultraviolet-erasable EPROM (OTPROM in a non-windowed package). The MC68HC11E20 has 20 Kbytes of mask-programmed ROM. The ROMON control bit in the CONFIG register controls the presence of ROM/EPROM in the memory map. In special test, bootstrap, and single-chip modes, ROMON = 1 out of reset and the 20 Kbytes of ROM/EPROM is enabled and located in two blocks. The two blocks are 8 Kbytes and 12 Kbytes in size. The 8-Kbyte block is located at $9000–AFFF and the 12-Kbyte block is located at $D000–FFFF. In single-chip mode the ROM/EPROM is enabled, regardless of the value in the CONFIG register. To use the ROM/EPROM in expanded mode, begin in single-chip mode, then change to expanded mode by setting the MDA bit in HPRIO register.

EPROM can be programmed in any operating mode — special test, bootstrap, expanded, or single chip. Programming is accomplished through the EPROG register. Programming EPROM requires an external 12.25 volt nominal power supply (V_{PPE}).

To program the EPROM, complete the following steps using the EPROG register:

1. Set the ELAT bit in EPROG register.
2. Write data to the desired address.
3. Turn on programming voltage by setting the PGM bit in EPROG register.
4. Delay for 10 ms or more, as appropriate.
5. Clear the PGM bit in EPROG to turn off the programming voltage.
6. Clear the EPROG register to reconfigure the EPROM address and data buses for normal operation.

Although the external 12.25 V programming voltage must be applied to the $\overline{XIRQ}/V_{PPE}$ pin during EPROM programming, it should be equal to V_{DD} before verifying the data that was just programmed. It should equal V_{DD} during normal operation also. The $\overline{XIRQ}/V_{PPE}$ pin has a high voltage detect circuit that inhibits assertion of the ELAT bit when programming voltage is at low levels.

CAUTION

If the MCU is used in any operating mode while high voltage (12.25 V nominal) is present on the $\overline{XIRQ}/V_{PPE}$ pin, the $\overline{IRQ}/CE$ pin must be pulled high to avoid accidental programming or corruption of EPROM contents. After programming an EPROM location, $\overline{IRQ}/CE$ must also be pulled high before the address and data are changed to program the next location.

EPROG — EPROM Programming Control $1036

Bit 7	6	5	4	3	2	1	Bit 0
MBE	—	ELAT	EXCOL	EXROW	T1	T0	PGM

RESET: 0   0   0   0   0   0   0   0

MBE — Multiple-Byte Programming Enable

When multiple-byte programming is enabled, address bit 5 is considered a don't care so that bytes with address bit 5 = 0 and address bit 5 = 1 both get programmed. MBE can be read in any mode and always reads zero in normal modes. MBE can only be written in special modes.

0 = EPROM array configured for normal programming
1 = Program two bytes with the same data

Bit 6 — Not Implemented

Always reads zero

ELAT — EPROM Latch Control

When ELAT = 1, writes to EPROM cause address and data to be latched and the EPROM cannot be read. ELAT can be read any time. ELAT can be written any time except when PGM = 1; then the write to ELAT will be disabled.

0 = EPROM address and data bus configured for normal reads
1 = EPROM address and data bus configured for programming

EXCOL — Select Extra Columns

0 = User array selected
1 = User array is disabled and extra columns are accessed at bits [7:0]. Addresses use bits [13:5] and bits [4:0] are don't care. EXCOL can only be read in special modes and always returns zero in normal modes. EXCOL can be written in special modes only.

EXROW — Select Extra Rows

0 = User array selected
1 = User array is disabled and two extra rows are available. Addresses use bits [7:0] and bits [13:8] are don't care. EXROW can only be read in special modes and always returns zero in normal modes. EXROW can be written in special modes only.

T[1:0] — EPROM Test Mode Select Bits

T1	T2	Function Selected
0	0	Normal Mode
0	1	Reserved
1	0	Gate Stress
1	1	Drain Stress

These bits allow selection of either gate stress or drain stress test modes. They can be read only in special modes and always read zero in normal modes. T[1:0] can only be written in special modes.

PGM — EPROM Programming Voltage Enable

0 = Programming voltage to EPROM array disconnected
1 = Programming voltage to EPROM array connected

PGM can be read any time and can only be written when ELAT = 1.

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MC68HC11E20
MC68HC11E20TS/D

Electrically Erasable Programmable Read-Only Memory (EEPROM)

The 512 bytes of EEPROM in the MC68HC711E20 are located at $B600 through $B7FF. The EEON bit in the CONFIG register controls whether the EEPROM is present in the memory map. When EEON =1 (erased state), the EEPROM is enabled; when EEON = 0, the EEPROM is disabled and not present in the memory map. EEON is reset to the value last programmed into CONFIG.

An on-chip charge pump develops the high voltage required for programming and erasing. When the frequency of the E clock is less than 1 MHz, select the internal clock source to drive the EEPROM charge pump by writing one to the CSEL bit in the OPTION register.

Programming and erasing the EEPROM is controlled by the PPROG register, and dependent upon the block protect (BPROT) register value.

To erase the EEPROM, ensure that the proper bits of the BPROT register are cleared, then complete the following steps using the PPROG register:

1. Set the ERASE, EELAT, and appropriate BYTE and ROW bits in PPROG register.
2. Write to the appropriate EEPROM address with any data. Row erase only requires a write to any location in the row. Bulk erase is done by writing to any location in the array.
3. Set the ERASE, EELAT, EEPGM, and appropriate BYTE and ROW bits in PPROG register.
4. Delay for 10 ms or more, as appropriate.
5. Clear the EEPGM bit in PPROG to turn off the programming voltage.
6. Clear the PPROG register to reconfigure the EEPROM address and data buses for normal operation.

To program the EEPROM, ensure the proper bits of the BPROT register are cleared and use the PROG register to complete the following steps:

1. Set the EELAT bit in PPROG register.
2. Write data to the desired address.
3. Set EEPGM bit in PPROG.
4. Delay for 10 ms or more, as appropriate.
5. Clear the EEPGM bit in PPROG to turn off the programming voltage.
6. Clear the PPROG register to reconfigure the EEPROM address and data buses for normal operation.

CAUTION

Since it is possible to perform other operations while the EEPROM program/erase operation is in progress, it is common to start the operation and then return to the main program until the 10 ms is completed. When the EELAT bit is set at the beginning of a program/erase operation, the EEPROM is electronically removed from the memory map; thus, it is not accessible during the program/erase cycle. Care must be taken to ensure that EEPROM resources will not be needed by any routines in the code during the 10 ms program/erase time.

PPROG — EEPROM Programming Control $103B

	Bit 7	6	5	4	3	2	1	Bit 0
	ODD	EVEN	—	BYTE	ROW	ERASE	EELAT	EEPGM
RESET:	0	0	0	0	0	0	0	0

ODD — Program Odd Rows in Half of EEPROM (TEST)

EVEN — Program Even Rows in Half of EEPROM (TEST)

Bit 5 — Not implemented
    Always reads zero

BYTE — Byte/Other EEPROM Erase Mode

ROW — Row/All EEPROM Erase Mode

BYTE	ROW	Action
0	0	Bulk Erase (All 512 Bytes)
0	1	Row Erase (16 Bytes)
1	0	Byte Erase
1	1	Byte Erase

ERASE — Erase/Normal Control for EEPROM
    0 = Normal read or program mode
    1 = Erase mode

EELAT — EEPROM Latch Control
    0 = EEPROM address and data bus configured for normal reads
    1 = EEPROM address and data bus configured for programming or erasing

EEPGM — EEPROM Programming Voltage Enable
    0 = Programming voltage to EEPROM array disconnected
    1 = Programming voltage to EEPROM array connected

BPROT — Block Protect   **$1035**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	—	PTCON	BPRT3	BPRT2	BPRT1	BPRT0
RESET:	0	0	0	1	1	1	1	1

PTCON — Protect for CONFIG
    0 = CONFIG register can be programmed or erased normally
    1 = CONFIG register cannot be programmed or erased

BPRT[3:0] — Block Protect Bits for EEPROM
    0 = Protection disabled for associated block
    1 = Protection enabled for associated block

Bit Name	Block Protected	Block Size
BPRT0	$B600–$B61F	32 Bytes
BPRT1	$B620–$B65F	64 Bytes
BPRT2	$B660–$B6DF	128 Bytes
BPRT3	$B6E0–$B7FF	288 Bytes

NOTE

Block protect register bits can be written to zero (protection disabled) within 64 cycles of a reset in normal modes, or at any time in special modes. Block protect register bits can be written to one (protection enabled) at any time.

EEPROM Security Feature

Although it is not an operating mode, the security feature affects how the MCU behaves in certain modes. When the optional security feature has been specified prior to manufacture and enabled via the NOSEC bit in CONFIG, the MCU is restricted to operation in single-chip modes only. When the NOSEC bit equals zero, the MCU ignores the state of the MODA pin during reset. This allows the MCU to be operated in single-chip and bootstrap modes only. These modes of operation do not allow external visibility of the internal address and data buses. Although the security feature can easily be disabled when in bootstrap mode, the bootloader firmware residing in bootstrap ROM checks to see if the NOSEC bit is clear. If NOSEC is clear (security enabled), the bootloader program first erases the entire EEPROM array then writes $FF to all locations in RAM. The program then verifies that these two steps have been completed. If they have not, they are repeated. Once these steps have been verified, the reset sequence continues and the device is brought into bootstrap mode as usual. For more information refer to *M68HC11 Reference Manual* (M68HC11RM/AD).

Configuration Control Register (CONFIG)

The CONFIG register is used to define several system functions. CONFIG is made up of EEPROM cells and static working latches. The operation of the MCU is controlled directly by these latches and not the actual EEPROM byte. When programming the CONFIG register, the EEPROM byte is being accessed. When the CONFIG register is being read, the static latches are being accessed.

The CONFIG register can be read at any time. The value read is the one latched from the EEPROM cells during the last reset sequence. A new value programmed into this register cannot be read until a subsequent reset occurs. Unused bits always read as ones.

In normal modes (SMOD = 0), CONFIG bits can only be written using the EEPROM programming sequence, and are neither readable nor active until latched via the next reset. In special modes (SMOD = 1), CONFIG bits can be written at any time.

CONFIG — System Configuration Register $103F

Bit 7	6	5	4	3	2	1	Bit 0
—	—	—	—	NOSEC	NOCOP	ROMON	EEON

RESET: 0   0   0   0   1   —   —   —

Bits [7:4] — Not implemented
   Always read zero

NOSEC — Security Mode Disable
   The security feature, a mask option, protects the contents of RAM and EEPROM by restricting the operation of a protected device to single-chip modes. Changing to other modes while the device is protected forces erasure of all RAM and EEPROM contents. This option must be specified before manufacture.
   0 = RAM/EEPROM security mode enabled
   1 = RAM/EEPROM security mode disabled

NOCOP — COP Watchdog Timer Disable
   Refer to **Resets and Interrupts**.

ROMON — ROM/EPROM Enable
   If SMOD = 1, this bit can be written at any time. If SMOD = 0, this bit **cannot** be written. In single-chip mode ROMON is forced to one out of reset. In special test, boot, and normal expanded modes, ROMON is forced to zero out of reset.
   0 = 20 Kbytes of ROM/EPROM removed from the memory map
   1 = 20 Kbytes of ROM/EPROM present in the memory map

EEON — EEPROM Enable
   0 = 512 bytes EEPROM is removed from the memory map
   1 = 512 bytes EEPROM is present in the memory map

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Parallel Input/Output

The MC68HC11E20 has up to 38 input/output lines, depending on the operating mode. The data bus of this microcontroller is multiplexed with the low-order address outputs on port C.

Port A has three input-only pins, three output-only pins, and two bidirectional I/O pins. Port A shares functions with the timer system.

Port B is an 8-bit output-only port in single-chip mode, and the high-order address bus in expanded modes.

Port C is an 8-bit bidirectional port in single-chip mode, and the multiplexed low-order address and data bus in expanded modes.

Port D, a 6-bit bidirectional port, shares functions with the serial systems (SCI and SPI).

Port E is an 8-bit input-only port that shares functions with the A/D converter system.

Simple and full handshake input and output functions are available on ports B and C lines in single-chip mode. The following is a description of the handshake functions.

In simple strobed mode, port B is a strobed output port and port C is a latching input port. The two activities are available simultaneously.

The STRB output is pulsed for two E-clock periods each time there is a write to the PORTB register. The INVB bit in the PIOC register controls the polarity of STRB pulses. Port C levels are latched into the alternate port C latch (PORTCL) register on each assertion of the STRA input. STRA edge select, flag, and interrupt enable bits are located in the PIOC register. Any or all of the port C lines can still be used as general-purpose I/O while in strobed input mode.

Full handshake modes involve port C pins and the STRA and STRB lines. Input and output handshake modes are supported, and output handshake mode has a three-stated variation. STRA is an edge detecting input, and STRB is a handshake output. Control and enable bits are located in the PIOC register.

In full input handshake mode, the MCU uses STRB as a ready line to an external system. Port C logic levels are latched into PORTCL when the STRA line is asserted by the external system. The MCU then negates STRB. The MCU reasserts STRB after the PORTCL register is read. A mix of latched inputs, static inputs, and static outputs is allowed on port C, differentiated by the data direction bits and use of the PORTC and PORTCL registers.

In full output handshake mode, the MCU writes data to PORTCL which, in turn, asserts the STRB output to indicate that data is ready. The external system reads port C and asserts the STRA input to acknowledge that data has been received.

In the three-state variation of output handshake mode, lines intended as three-state handshake outputs are configured as inputs by clearing the corresponding DDRC bits. The MCU writes data to PORTCL and asserts STRB. The external system responds by activating the STRA input, which forces the MCU to drive the data in PORTCL out on all of the port C lines. The mode variation does not allow part of port C to be used for static inputs while other port C pins are being used for handshake outputs. Refer to the PIOC register description for further information.

The following table is a summary of the configuration and features of each port.

Port	Input Pins	Output Pins	Bidirectional Pins	Shared Functions
Port A	3	3	2	Timer
Port B	—	8	—	High Order Address
Port C	—	—	8	Data Bus/Low Order Address/General I/O
Port D	—	—	6	SCI and SPI
Port E	8	—	—	A/D Converter

Port pin function is mode dependent. Do not confuse pin function with the electrical state of the pin at reset. Port pins are either driven to a specified logic level or are configured as high impedance inputs. I/O pins configured as high-impedance inputs have port data that is indeterminate. The contents of the corresponding latches are dependent upon the electrical state of the pins during reset. In port descriptions, an "I" indicates this condition. Port pins that are driven to a known logic level during reset are shown with a value of either one or zero. Some control bits are unaffected by reset. Reset states for these bits are indicated with a "U".

PIOC — Parallel I/O Control   **$1002**

	Bit 7	6	5	4	3	2	1	Bit 0
	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB
RESET:	0	0	0	0	0	U	1	1

STAF — Strobe A Interrupt Status Flag
   STAF is set when the selected edge occurs on Strobe A and cleared by reading PIOC with STAF set followed by a PORTCL read (simple strobed or full input handshake mode) or PORTCL write (output handshake mode).
      0 = No Active Edge Detected
      1 = Selected Active Edge Detected

STAI — Strobe A Interrupt Enable Mask
      0 = STAF does not request interrupt
      1 = STAF requests interrupt

CWOM — Port C Wired-OR Mode (affects all eight port C pins)
      0 = Port C outputs are normal CMOS outputs
      1 = Port C outputs are open-drain outputs

HNDS — Handshake Mode
      0 = Simple strobe mode
      1 = Full input or output handshake mode

OIN — Output or Input Handshake Select
   HNDS must be set to one for this bit to have meaning.
      0 = Input handshake
      1 = Output handshake

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PLS — Pulse/Interlocked Handshake Operation

HNDS must be set to one for this bit to have meaning. Once activated, strobe B stays active until the selected edge of strobe A is detected when interlocked handshake is selected.

0 = Interlocked handshake

1 = Pulsed handshake (Strobe B pulses high for two E-clock cycles.)

EGA — Active Edge for Strobe A

0 = STRA falling edge selected

1 = STRA rising edge selected

INVB — Invert Strobe B

0 = Active level is logic zero

1 = Active level is logic one

Parallel I/O Control

	STAF Clearing Sequence	HNDS	OIN	PLS	EGA	Port B	Port C
Simple strobed mode	Read PIOC with STAF = 1 then read PORTCL	0	X	X	0 ↓ 1 ↑	Inputs latched into PORTCL on any active edge on STRA	STRB pulses on writes to PORTB
Full input handshake mode	Read PIOC with STAF = 1 then read PORTCL	1	0	0 = STRB active level 1 = STRB active pulse	1 ↓ 0 ↑	Inputs latched into PORTCL on any active edge on STRA	Normal output port, unaffected in handshake modes
Full output handshake mode	Read PIOC with STAF = 1 then write PORTCL	1	1	0 = STRB active level 1 = STRB active pulse	0 ↓ Port C Driven 1 ↑ Follow DDRC STRA Active Edge Follow DDRC	Driven as outputs if STRA at active level; follows DDRC if STRA not at active level	Normal output port, unaffected in handshake modes

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PORTA — Port A Data $1000

	Bit 7	6	5	4	3	2	1	Bit 0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	I	0	0	0	I	I	I	I
Alt. Pin Func.:	PAI	OC2	OC3	OC4	OC5/IC4	IC1	IC2	IC3
And/or:	OC1	OC1	OC1	OC1	OC1	—	—	—

PACTL — Pulse Accumulator Control $1026

Bit 7	6	5	4	3	2	1	Bit 0
DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0

RESET: 0   0   0   0   0   0   0   0

DDRA7 — Data Direction for Port A Bit 7
     0 = Input only
     1 = Output

PAEN — Pulse Accumulator System Enable
     Refer to **Pulse Accumulator**.

PAMOD — Pulse Accumulator Mode
     Refer to **Pulse Accumulator**.

PEDGE — Pulse Accumulator Edge Control
     Refer to **Pulse Accumulator**.

DDRA3 — Data Direction for Port A Bit 3
     Overridden if an output compare function is configured to control the PA3 pin.
         0 = Input
         1 = Output

I4/O5 — Input Capture 4/Output Compare 5
     Refer to **Main Timer**.

RTR[1:0] — Real-Time Interrupt (RTI) Rate
     Refer to **Main Timer**.

PORTB — Port B Data $1004

	Bit 7	6	5	4	3	2	1	Bit 0
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
S. Chip or Boot:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
RESET:	0	0	0	0	0	0	0	0
Expan. or Test:	ADDR15	ADDR14	ADDR13	ADDR12	ADDR11	ADDR10	ADDR9	ADDR8

In single-chip or bootstrap modes, port B pins are general-purpose outputs. In expanded or special test modes, port B pins are high order address outputs. In PROG mode, port B pins are high-order address inputs.

PORTC — Port C Data $1003

	Bit 7	6	5	4	3	2	1	Bit 0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
S. Chip or Boot:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:	I	I	I	I	I	I	I	I
Expan. or Test:	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

In single-chip and bootstrap modes, port C pins reset to high impedance inputs (DDRC bits are set to zero). It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. In expanded and special test modes, port C pins are multiplexed address/data bus and the port C register address is treated as an external memory location.

PORTCL — Port C Latched Data $1005

	Bit 7	6	5	4	3	2	1	Bit 0
	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
RESET:	I	I	I	I	I	I	I	I

PORTCL is used in the handshake clearing mechanism. When an active edge occurs on the STRA pin, port C data is latched into the PORTCL register. Reads of this register return the last value latched into PORTCL and clear STAF flag (following a read of PIOC with STAF set).

DDRC — Data Direction Register for Port C $1007

	Bit 7	6	5	4	3	2	1	Bit 0
	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
RESET:	0	0	0	0	0	0	0	0

DDC[7:0] — Data Direction for Port C
   0 = Input
   1 = Output
In handshake output mode, DDRC bits select the three-stated output option (DDCx = 1).

PORTD — Port D Data   **$1008**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	0	0	I	I	I	I	I	I
Alt. Pin Func.:	—	—	$\overline{SS}$	SCK	SDO/ MOSI	SDI/ MISO	TxD	RxD

In all modes, port D bits [5:0] can be used either for general-purpose I/O, or with the SCI and SPI subsystems. During reset, port D pins PD[5:0] are configured as high impedance inputs (DDRD bits cleared).

DDRD — Data Direction Register for Port D   **$1009**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0

Bits [7:6] — Not implemented
   Always read zero

DDD[5:0] — Data Direction for Port D
   0 = Input
   1 = Output

PORTE — Port E Data   **$100A**

	Bit 7	6	5	4	3	2	1	Bit 0
	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
RESET:	I	I	I	I	I	I	I	I
Alt. Pin Func.:	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

Port E has eight general-purpose input pins and shares functions with the A/D converter system. When any port E pins are being used as A/D inputs, PORTE should not be read during the sample portion of an A/D conversion.

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Resets and Interrupts

The MC68HC11E20 has 3 reset vectors and 18 interrupt vectors. The reset vectors are as follows:

- $\overline{\text{RESET}}$, or Power-On Reset
- Clock Monitor Fail
- COP Failure

The 18 interrupt vectors service 23 interrupt sources (3 nonmaskable, 20 maskable). The three nonmaskable interrupt vectors are as follows:

- $\overline{\text{XIRQ}}$ Pin (X-Bit Interrupt)
- Illegal Opcode Trap
- Software Interrupt

On-chip peripheral systems generate maskable interrupts, which are recognized only if the global interrupt mask bit (I) in the condition code register (CCR) is clear. Maskable interrupts are prioritized according to a default arrangement; however, any one source can be elevated to the highest maskable priority position by a software-accessible control register, HPRIO. The HPRIO register can be written at any time, provided the I bit in the CCR is set.

Twenty interrupt sources in the MC68HC11E20 are subject to masking by a global interrupt mask bit (I bit in the CCR). In addition to the global I bit, all of these sources, except the external interrupt ($\overline{\text{IRQ}}$) pin, are controlled by local enable bits in control registers. Most interrupt sources in the M68HC11 have separate interrupt vectors; therefore, there is usually no need for software to poll control registers to determine the cause of an interrupt.

For some interrupt sources, such as the SCI interrupts, flags are automatically cleared during the normal course of responding to the interrupt requests. For example, the RDRF flag in the SCI system is cleared by an automatic clearing mechanism consisting of a read of the SCI status register while RDRF is set, followed by a read of the SCI data register. The normal response to an RDRF interrupt request would be to read the SCI status register to check for receive errors, then to read the received data from the SCI data register. These two steps satisfy the automatic clearing mechanism without requiring any special instructions.

Refer to the following table for interrupt and reset vector assignments.

Vector Address	Interrupt Source	CCR Mask Bit	Local Mask	Priority (1=High)
FFC0, C1 – FFD4, D5	Reserved	—	—	—
FFD6, D7	SCI Serial System	I		23
	• SCI Receive Data Register Full		RIE	
	• SCI Receiver Overrun		RIE	
	• SCI Transmit Data Register Empty		TIE	
	• SCI Transmit Complete		TCIE	
	• SCI Idle Line Detect		ILIE	
FFD8, D9	SPI Serial Transfer Complete	I	SPIE	22
FFDA, DB	Pulse Accumulator Input Edge	I	PAII	21
FFDC, DD	Pulse Accumulator Overflow	I	PAOVI	20
FFDE, DF	Timer Overflow	I	TOI	19
FFE0, E1	Timer Input Capture 4/Output Compare 5	I	I4/O5I	17
FFE2, E3	Timer Output Compare 4	I	OC4I	14
FFE4, E5	Timer Output Compare 3	I	OC3I	13
FFE6, E7	Timer Output Compare 2	I	OC2I	12
FFE8, E9	Timer Output Compare 1	I	OC1I	11
FFEA, EB	Timer Input Capture 3	I	IC3I	10
FFEC, ED	Timer Input Capture 2	I	IC2I	9
FFEE, EF	Timer Input Capture 1	I	IC1I	8
FFF0, F1	Real-Time Interrupt	I	RTII	7
FFF2, F3	Parallel I/O Handshake	I	None	6
	IRQ (External Pin)	I	None	5
FFF4, F5	XIRQ Pin	X	None	4
FFF6, F7	Software Interrupt	None	None	*
FFF8, F9	Illegal Opcode Trap	None	None	*
FFFA, FB	COP Failure	None	NOCOP	3
FFFC, FD	Clock Monitor Fail	None	CME	2
FFFE, FF	RESET	None	None	1

* Same level as an instruction

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Bit 7	6	5	4	3	2	1	Bit 0
ADPU	CSEL	IRQE*	DLY*	CME	—	CR1*	CR0*

RESET: 0   0   0   1   0   0   0   0

* Can be written only once in first 64 cycles out of reset in normal mode, or at any time in special modes.

ADPU — Analog-to-Digital Converter Power Up
  Refer to **Analog-to-Digital Converter**.

CSEL — Clock Select
  Refer to **Analog-to-Digital Converter**.

IRQE — $\overline{\text{IRQ}}$ Select Edge-Sensitive Only
    0 = Low level recognition
    1 = Falling edge recognition

DLY — Enable Oscillator Startup Delay on Exit from STOP
    0 = No stabilization delay on exit from STOP
    1 = Stabilization delay enabled on exit from STOP

CME — Clock Monitor Enable
    0 = Clock monitor disabled; slow clocks can be used
    1 = Slow or stopped clocks cause clock failure reset

Bit 2 — Not implemented
    Always reads zero

CR[1:0] — COP Timer Rate Select

COP Timer Rate Select

CR[1:0]	Divide $E/2^{15}$ By	XTAL = 4.0 MHz Timeout −0/+32.8 ms	XTAL = 8.0 MHz Timeout −0/+16.4 ms	XTAL = 12.0 MHz Timeout −0/+10.9 ms
0 0	1	32.768 ms	16.384 ms	10.923 ms
0 1	4	131.072 ms	65.536 ms	43.691 ms
1 0	16	524.288 ms	262.140 ms	174.76 ms
1 1	64	2.097 sec	1.049 sec	699.05 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz

COPRST — Arm/Reset COP Timer Circuitry $103A

Bit 7	6	5	4	3	2	1	Bit 0
7	6	5	4	3	2	1	0

RESET: 0   0   0   0   0   0   0   0

> Write $55 (%01010101) to COPRST to arm COP watchdog clearing mechanism. Write $AA
> (%10101010) to COPRST to reset COP watchdog.

CONFIG — System Configuration Register $103F

Bit 7	6	5	4	3	2	1	Bit 0
—	—	—	—	NOSEC	NOCOP	ROMON	EEON

RESET: 0   0   0   0   1   1   1   1

Bits [7:4] — Not implemented
　　Always read zero

NOSEC — COP System Disable
　　Refer to **On-Chip Memory**.

NOCOP — COP System Disable
　　Resets to programmed value
　　　　0 = COP enabled (forces reset on timeout)
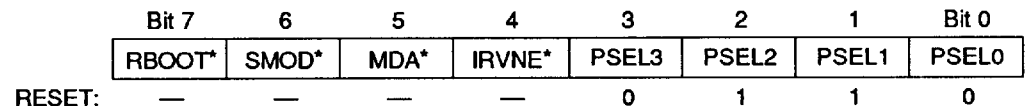　　　　1 = COP disabled (does not force reset on timeout)

ROMON — ROM/EPROM Enable
　　Refer to **On-Chip Memory**.

EEON — COP System Disable
　　Refer to **On-Chip Memory**.

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous   **$103C**

Bit 7	6	5	4	3	2	1	Bit 0
RBOOT*	SMOD*	MDA*	IRVNE*	PSEL3	PSEL2	PSEL1	PSEL0

RESET: —   —   —   —   0   1   1   0

*RBOOT, SMOD, MDA, and IRVNE reset depend on power-up initialization mode.

RBOOT — Read Bootstrap ROM
    Refer to **Operating Modes**.

SMOD — Special Mode Select
    Refer to **Operating Modes**.

MDA — Mode Select A
    Refer to **Operating Modes**.

IRVNE — Internal Read Visibility/Not E (IRVNE can be written once in any mode)
    Refer to **Operating Modes**.

PSEL[3:0] — Priority Select Bit 3 through Bit 0
    Can be written only while the I-bit in the CCR is set (interrupts disabled). These bits select one interrupt source to be elevated above all other I-bit related sources.

PSEL[3:0]				Interrupt Source Promoted
0	0	0	0	Timer Overflow
0	0	0	1	Pulse Accumulator Overflow
0	0	1	0	Pulse Accumulator Input Edge
0	0	1	1	SPI Serial Transfer Complete
0	1	0	0	SCI Serial System
0	1	0	1	Reserved (Default to $\overline{\text{IRQ}}$)
0	1	1	0	$\overline{\text{IRQ}}$ (External Pin)
0	1	1	1	Real-Time Interrupt
1	0	0	0	Timer Input Capture 1
1	0	0	1	Timer Input Capture 2
1	0	1	0	Timer Input Capture 3
1	0	1	1	Timer Output Compare 1
1	1	0	0	Timer Output Compare 2
1	1	0	1	Timer Output Compare 3
1	1	1	0	Timer Output Compare 4
1	1	1	1	Timer Output Compare 5/Input Capture 4

Main Timer

The design of the main timer is based on a free-running 16-bit counter with a four-stage programmable prescaler. A timer overflow function allows software to extend the system's timing capability beyond the counter's 16-bit range.

The timer has three input capture channels, four output compare channels, and one channel that can be configured as a fourth input capture or a fifth output compare.

Refer to the following table for a summary of the crystal-related frequencies and periods.

Timer Summary

Control Bits	XTAL Frequencies			
	4.0 MHz	8.0 MHz	12.0 MHz	Other Rates
	1.0 MHz	2.0 MHz	3.0 MHz	(E)
	1000 ns	500 ns	333 ns	(1/E)
PR[1:0]	Main Timer Count Rates			
0 0 1 count — overflow —	1.0 μs 65.536 ms	500 ns 32.768 ms	333 ns 21.845 ms	(E/1) (E/2^{16})
0 1 1 count — overflow —	4.0 μs 262.14 ms	2.0 μs 131.07 ms	1.333 μs 87.381 ms	(E/4) (E/2^{18})
1 0 1 count — overflow —	8.0 μs 524.29 ms	4.0 μs 262.14 ms	2.667 μs 174.76 ms	(E/8) (E/2^{19})
1 1 1 count — overflow —	16.0 μs 1.049 ms	8.0 μs 524.29 ms	5.333 μs 349.52 ms	(E/16) (E/2^{20})
RTR[1:0]	Periodic Interrupt (RTI) Rates			
0 0	8.192 ms	4.096 ms	2.731 ms	(E/2^{13})
0 1	16.384 ms	8.192 ms	5.461 ms	(E/2^{14})
1 0	32.768 ms	16.384 ms	10.923 ms	(E/2^{15})
1 1	65.536 ms	32.768 ms	21.845 ms	(E/2^{16})
CR[1:0]	COP Watchdog Timeout Rates			
0 0	32.768 ms	16.384 ms	10.923 ms	(E/2^{15})
0 1	131.072 ms	65.536 ms	43.691 ms	(E/2^{17})
1 0	524.288 ms	262.140 ms	174.76 ms	(E/2^{19})
1 1	2.097 sec	1.049 sec	699.05 ms	(E/2^{21})
Timeout Tolerance (− 0 ms/+...)	32.8 ms	16.4 ms	10.9 ms	(E/2^{15})

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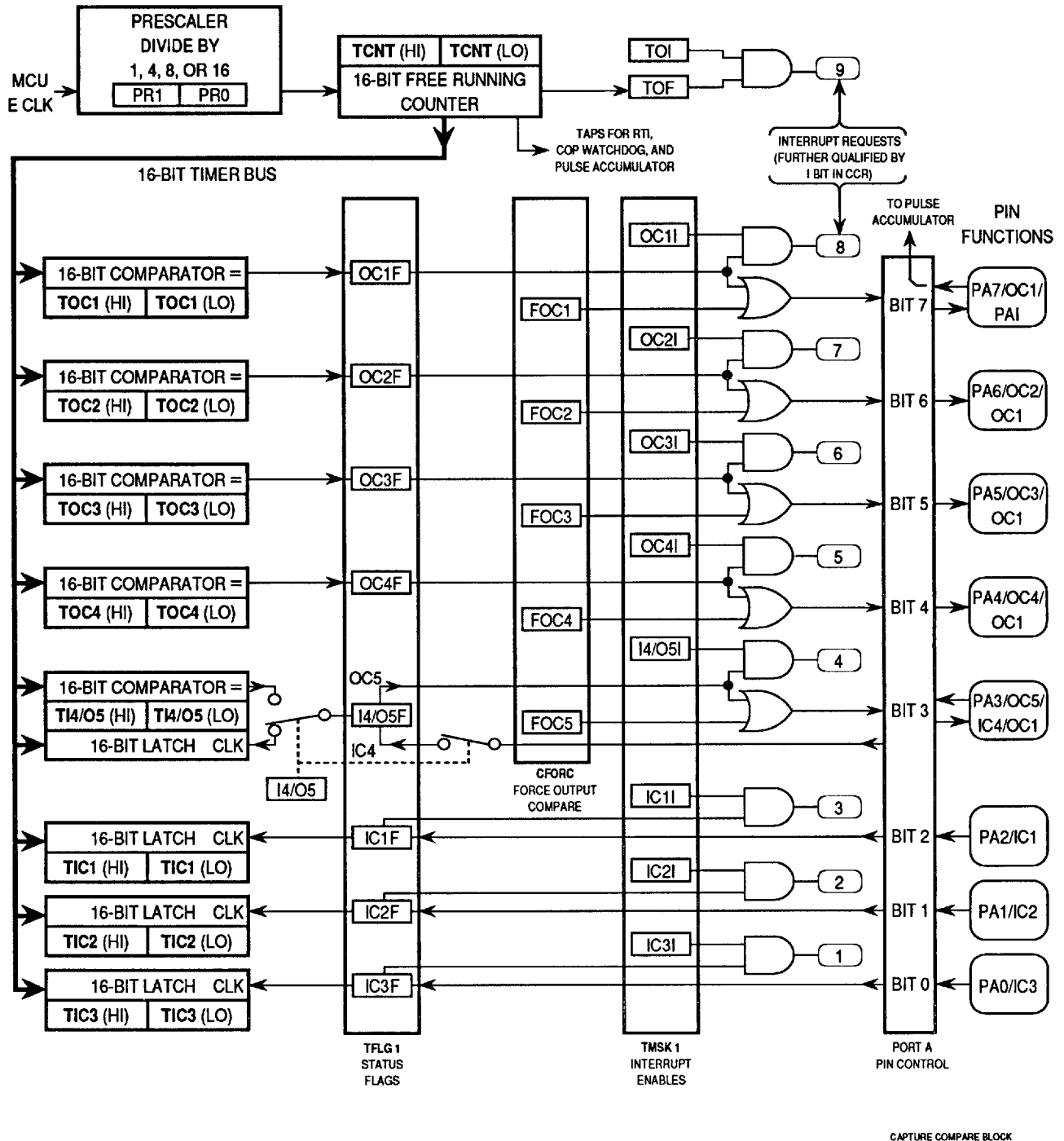
Timer Block Diagram

CFORC — Timer Compare Force $100B

Bit 7	6	5	4	3	2	1	Bit 0
FOC1	FOC2	FOC3	FOC4	FOC5	—	—	—

RESET: 0   0   0   0   0   0   0   0

FOC[5:1] — Force Output Compare
　　Write ones to force compare(s)
　　　0 = Not affected
　　　1 = Output x action occurs

Bits [2:0] — Not implemented
　　Always read zero

OC1M — Output Compare 1 Mask $100C

Bit 7	6	5	4	3	2	1	Bit 0
OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	—	—	—

RESET: 0   0   0   0   0   0   0   0

　　Set bit(s) to enable OC1 to control corresponding pin(s) of port A

Bits [2:0] — Not implemented
　　Always read zero

OC1D — Output Compare 1 Data $100D

Bit 7	6	5	4	3	2	1	Bit 0
OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	—	—	—

RESET: 0   0   0   0   0   0   0   0

　　If OC1Mx is set, data in OC1Dx is output to port A bit x on successful OC1 compares.

Bits [2:0] — Not implemented
　　Always read zero

TCNT — Timer Count $100E, $100F

	Bit 15	14	13	12	11	10	9	Bit 8	High
$100E	Bit 15	14	13	12	11	10	9	Bit 8	High
$100F	Bit 7	6	5	4	3	2	1	Bit 0	Low

TCNT resets to $1000
　　In normal modes, TCNT is a read-only register.

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TIC1–TIC3 — Timer Input Capture $1010–$1015

$1010	Bit 15	14	13	12	11	10	9	Bit 8	High TIC1
$1011	Bit 7	6	5	4	3	2	1	Bit 0	Low
$1012	Bit 15	14	13	12	11	10	9	Bit 8	High TIC2
$1013	Bit 7	6	5	4	3	2	1	Bit 0	Low
$1014	Bit 15	14	13	12	11	10	9	Bit 8	High TIC3
$1015	Bit 7	6	5	4	3	2	1	Bit 0	Low

TICx not affected by reset

TOC1–TOC4 — Timer Output Compare $1016–$101D

$1016	Bit 15	14	13	12	11	10	9	Bit 8	High TOC1
$1017	Bit 7	6	5	4	3	2	1	Bit 0	Low
$1018	Bit 15	14	13	12	11	10	9	Bit 8	High TOC2
$1019	Bit 7	6	5	4	3	2	1	Bit 0	Low
$101A	Bit 15	14	13	12	11	10	9	Bit 8	High TOC3
$101B	Bit 7	6	5	4	3	2	1	Bit 0	Low
$101C	Bit 15	14	13	12	11	10	9	Bit 8	High TOC4
$101D	Bit 7	6	5	4	3	2	1	Bit 0	Low

All TOCx register pairs reset to ones ($FFFF).

TI4/O5 — Timer Input Capture 4/Output Compare 5 $101E, $101F

$101E	Bit 15	14	13	12	11	10	9	Bit 8	High
$101F	Bit 7	6	5	4	3	2	1	Bit 0	Low

All TI4/O5 register pairs reset to ones ($FFFF).

TCTL1 — Timer Control 1 $1020

	Bit 7	6	5	4	3	2	1	Bit 0
	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
RESET:	0	0	0	0	0	0	0	0

OM[5:2] — Output Mode

OL[5:2] — Output Level

OMx	OLx	Action Taken on Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

TCTL2 — Timer Control 2 $1021

	Bit 7	6	5	4	3	2	1	Bit 0
	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
RESET:	0	0	0	0	0	0	0	0

Timer Control Configuration

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge

TMSK1 — Timer Interrupt Mask 1 $1022

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I
RESET:	0	0	0	0	0	0	0	0

OC1I–OC4I — Output Compare x Interrupt Enable
   If the OCxF flag bit is set while the OCxI enable bit is set, a hardware interrupt sequence is requested.

I4/O5I — Input Capture 4 or Output Compare 5 Interrupt Enable
   When I4/O5 in PACTL is one, I4/O5I is the input capture 4 interrupt bit. When I4/O5 in PACTL is zero, I4/O5I is the output compare 5 interrupt control bit.

IC1I–IC3I — Input Capture x Interrupt Enable
If the ICxF flag bit is set while the ICxI enable bit is set, a hardware interrupt sequence is requested.

NOTE

Bits in TMSK1 correspond bit for bit with flag bits in TFLG1. Ones in TMSK1 enable the corresponding interrupt sources.

TFLG1 — Timer Interrupt Flag 1 $1023

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

OC1F–OC4F — Output Compare x Flag
Set each time the counter matches output compare x value

I4/O5F — Input Capture 4/Output Compare 5 Flag
Set by IC4 or OC5, depending on which function was enabled by I4/O5 of PACTL

IC1F–IC3F — Input Capture x Flag
Set each time a selected active edge is detected on the ICx input line

---

TMSK2 — Timer Interrupt Mask 2 $1024

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	—	—	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt Enable
    0 = TOF interrupts disabled
    1 = Interrupt requested when TOF is set

RTII — Real-Time Interrupt Enable
    0 = RTIF interrupts disabled
    1 = Interrupt requested when PAOVF is set

PAOVI — Pulse Accumulator Overflow Interrupt Enable
Refer to **Pulse Accumulator**.

PAII — Pulse Accumulator Input Interrupt Enable
Refer to **Pulse Accumulator**.

Bits [3:2] — Not implemented
Always read zero

PR[1:0] — Timer Prescaler Select

In normal modes, PR0 and PR1 can only be written once, and the write must occur within 64 cycles after reset. The following table shows the prescaler selected with each combination of PR[1:0]. Refer to **Timer Summary** table for specific timing values.

PR[1:0]	Prescaler
0 0	÷ 1
0 1	÷ 4
1 0	÷ 8
1 1	÷ 16

NOTE

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

TFLG2 — Timer Interrupt Flag 2   **$1025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	—	—	—	—
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

TOF — Timer Overflow Flag
Set when TCNT changes from $FFFF to $0000

RTIF — Real-Time (Periodic) Interrupt Flag
Set periodically. Refer to RTR[1:0] in PACTL register.

PAOVF — Pulse Accumulator Overflow Flag
Refer to **Pulse Accumulator**.

PAIF — Pulse Accumulator Input Edge Flag
Refer to **Pulse Accumulator**.

Bits [3:0] — Not implemented
Always read zero

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PACTL — Pulse Accumulator Control $1026

Bit 7	6	5	4	3	2	1	Bit 0
DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0

RESET: 0   0   0   0   0   0   0   0

DDRA7 — Port A, Bit 7 Data Direction Control
    Refer to **Parallel Input/Output**.

PAEN — Pulse Accumulator System Enable
    Refer to **Pulse Accumulator**.

PAMOD — Pulse Accumulator Mode
    Refer to **Pulse Accumulator**.

PEDGE — Pulse Accumulator Edge Control
    Refer to **Pulse Accumulator**.

DDRA3 — Port A, Bit 3 Data Direction Control
    Refer to **Parallel Input/Output**.

I4/O5 — Input Capture 4/Output Compare 5
    Configure TI4/O5 for input capture or output compare
        0 = OC5 enabled
        1 = IC4 enabled

RTR[1:0] — Real-Time Interrupt (RTI) Rate

Real-Time Interrupt Rates

RTR[1:0]	Divide E By	XTAL = 4.0 MHz	XTAL = 8.0 MHz	XTAL = 12.0 MHz
0 0	2^{13}	8.19 ms	4.096 ms	2.731 ms
0 1	2^{14}	16.38 ms	8.192 ms	5.461 ms
1 0	2^{15}	32.77 ms	16.384 ms	10.923 ms
1 1	2^{16}	65.54 ms	32.768 ms	21.845 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz

OPTION — System Configuration Options   **$1039**

Bit 7	6	5	4	3	2	1	Bit 0
ADPU	CSEL	IRQE*	DLY*	CME	—	CR1*	CR0*

RESET: 0   0   0   1   0   0   0   0

*Can be written only once in first 64 cycles out of reset in normal modes or at any time in special modes.

ADPU — A/D Converter Power Up
    Refer to **Analog-to-Digital Converter**.

CSEL — Clock Select
    0 = A/D and EEPROM charge pumps use system E clock
    1 = A/D and EEPROM charge pumps use internal RC clock

IRQE — IRQ Select Edge-Sensitive Only
    Refer to **Resets and Interrupts**.

DLY — Enable Oscillator Startup Delay
    Refer to **Resets and Interrupts**.

CME — Clock Monitor Enable
    0 = Clock monitor disabled; slow clocks can be used
    1 = Slow or stopped clocks cause clock failure reset

Bit 2 — Not Implemented
    Always reads zero

CR[1:0] — COP Timer Rate Select
    Refer to the following table of COP timer rates.

COP Timer Rate Select

| CR[1:0]	Divide E/2^{15} By	XTAL = 4.0 MHz Timeout −0/+32.8 ms	XTAL = 8.0 MHz Timeout −0/+16.4 ms	XTAL = 12.0 MHz Timeout −0/+10.9 ms
0 0	1	32.768 ms	16.384 ms	10.923 ms
0 1	4	131.072 ms	65.536 ms	43.691 ms
1 0	16	524.288 ms	262.140 ms	174.76 ms
1 1	64	2.097 sec	1.049 sec	699.05 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz

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Pulse Accumulator

The MC68HC11E20 has an 8-bit counter that can be configured for gated time accumulation or to operate as a simple event counter. The pulse accumulator counter can be read or written at any time.

The PA7 pin can be configured to act as a clock in event counting mode, or as a gate signal to enable a free-running clock (E divided by 64) to the 8-bit counter in gated time accumulation mode.

		Common XTAL Frequencies		
	Selected Crystal	4.0 MHz	8.0 MHz	12.0 MHz
CPU Clock	(E)	1.0 MHz	2.0 MHz	3.0 MHz
Cycle Time	(1/E)	1000 ns	500 ns	333 ns
Pulse Accumulator (in Gated Mode)				
$(E/2^6)$	1 count –	64.0 μs	32.0 μs	21.330 μs
$(E/2^{14})$	overflow –	16.384 ms	8.192 ms	5.491 ms
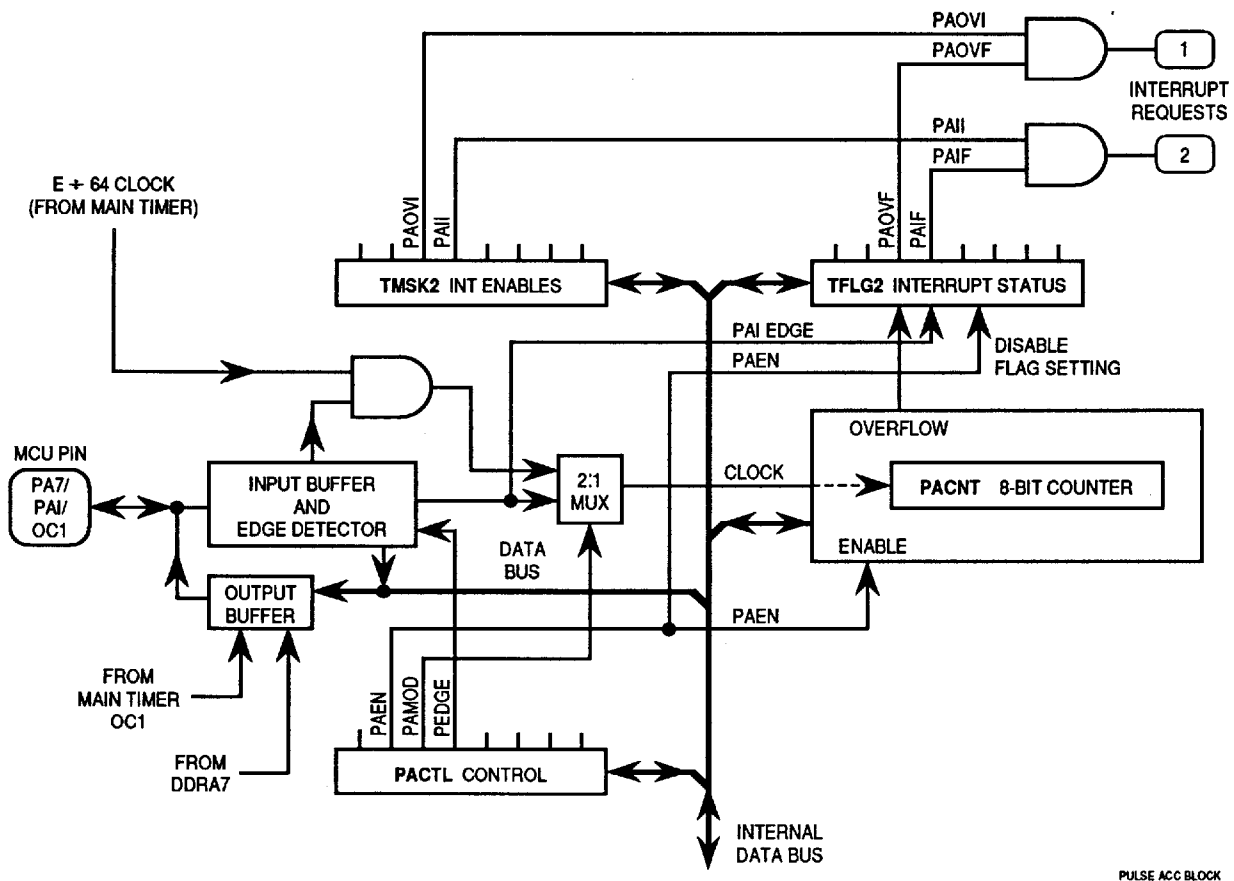
Pulse Accumulator System Block Diagram

TMSK2 — Timer Interrupt Mask 2   **$1024**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	—	—	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt Enable
  Refer to **Main Timer**.

RTII — Real-Time Interrupt Enable
  Refer to **Main Timer**.

PAOVI — Pulse Accumulator Overflow Interrupt Enable
  0 = PAOVF interrupts disabled
  1 = Interrupt requested when PAOVF is set to one

PAII — Pulse Accumulator Input Edge Interrupt Enable
  0 = PAIF interrupts disabled
  1 = Interrupt requested when PAIF is set to one

Bits [3:2] — Not implemented
  Always read zero

PR[1:0] — Timer Prescaler Select
  Refer to **Main Timer**.

NOTE

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2
enable the corresponding interrupt sources.

TFLG2 — Timer Interrupt Flag 2   **$1025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	—	—	—	—
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

TOF — Timer Overflow Flag
  Refer to **Main Timer**.

RTIF — Real-Time (Periodic) Interrupt Flag
  Refer to **Main Timer**.

PAOVF — Pulse Accumulator Overflow Flag
  Set when PACNT changes from $FF to $10

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PAIF — Pulse Accumulator Input Edge Flag
Set each time a selected active edge is detected on the PAI input line

Bits [3:0] — Not implemented
Always read zero

PACTL — Pulse Accumulator Control $1026

Bit 7	6	5	4	3	2	1	Bit 0
DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0

RESET: 0   0   0   0   0   0   0   0

DDRA7 — Port A, Bit 7 Data Direction Control
Refer to **Parallel Input/Output**.

PAEN — Pulse Accumulator System Enable
0 = Pulse accumulator disabled
1 = Pulse accumulator enabled

PAMOD — Pulse Accumulator Mode
0 = Event counter
1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control

PAMOD	PEDGE	Action on Clock
0	0	PAI falling edge increments the counter.
0	1	PAI rising edge increments the counter.
1	0	A zero on PAI inhibits counting.
1	1	A one on PAI inhibits counting.

DDRA3 — Port A, Bit 3 Data Direction Control
Refer to **Parallel Input/Output**.

I4/O5 — Input Capture 4/Output Compare 5
Refer to **Main Timer**.

RTR[1:0] — Real-Time Interrupt Rate
Refer to **Main Timer**.
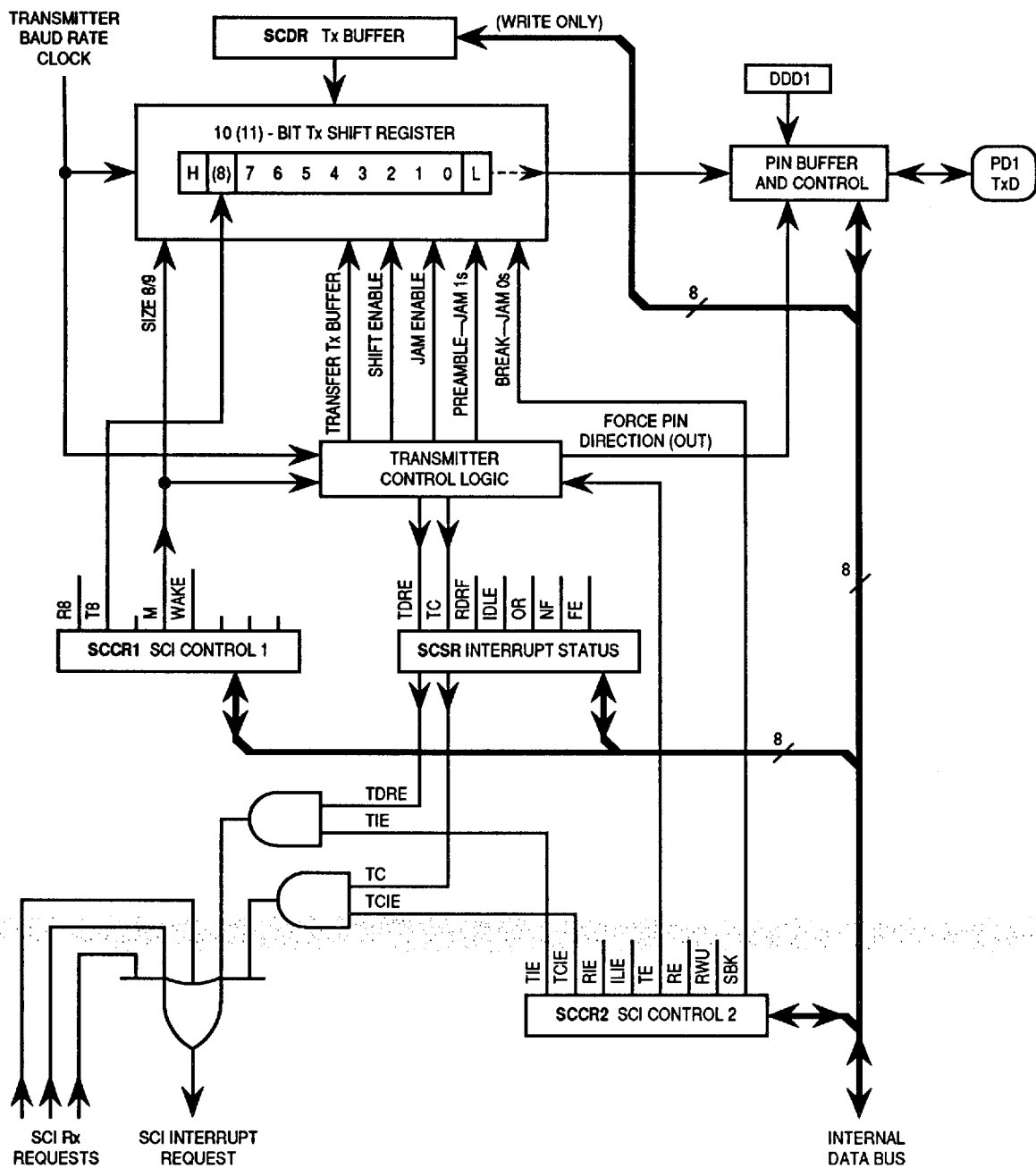

PACNT — Pulse Accumulator Counter $1027

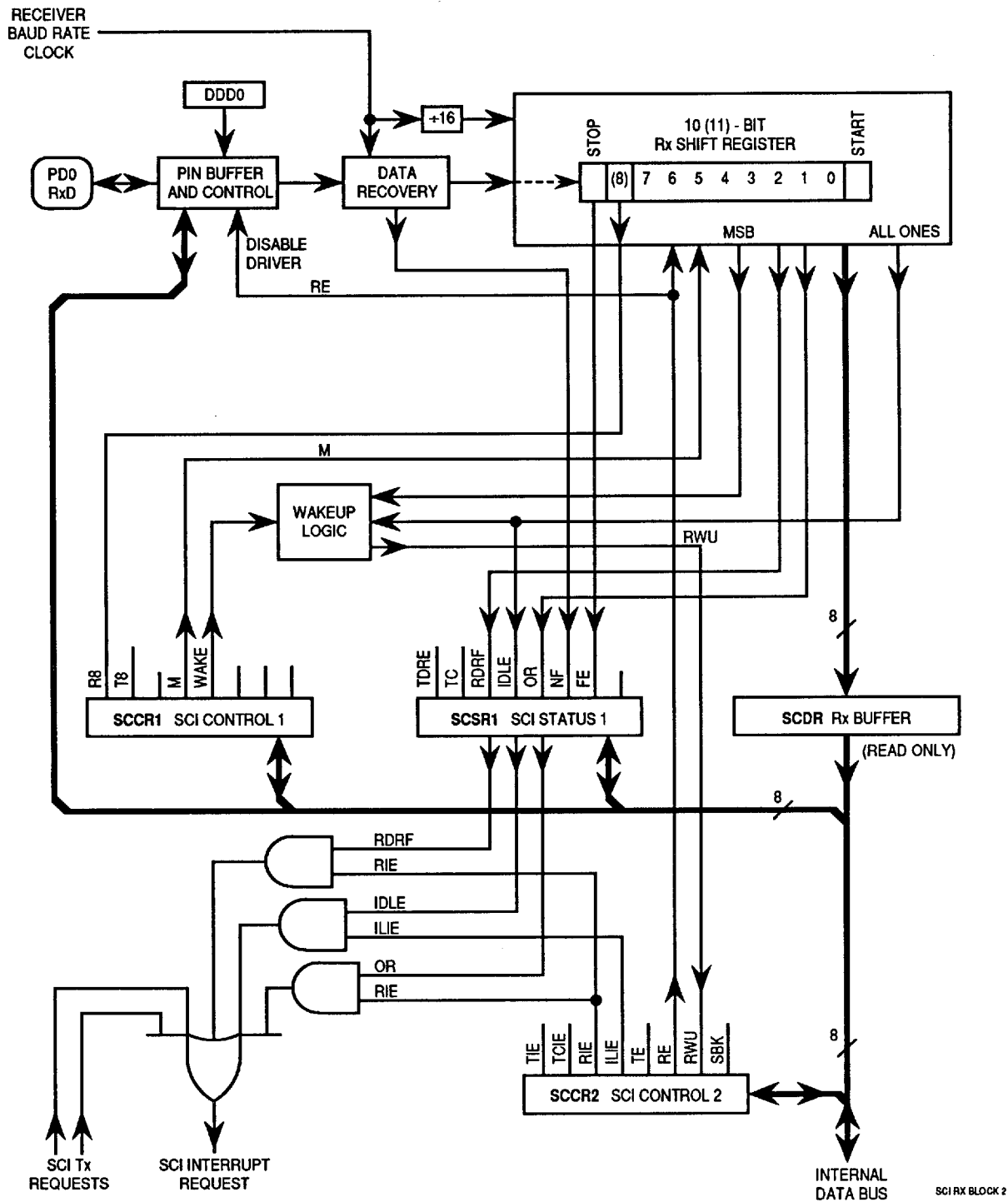| Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

Can be read and written, unaffected by reset.

Serial Communications Interface

The SCI is a universal asynchronous receiver transmitter (UART) serial communications interface, an independent serial I/O subsystem in the MC68HC11E20. It has a standard NRZ format (one start bit, eight or nine data bits and one stop bit) and several baud rates available. The SCI transmitter and receiver are independent, but use the same data format and bit rate. An extra bit in the baud rate control register (BAUD) adds a divide-by-39 to the SCI clock prescaler. Refer to the two tables in the BAUD register description for a summary of the SCI baud rate values.
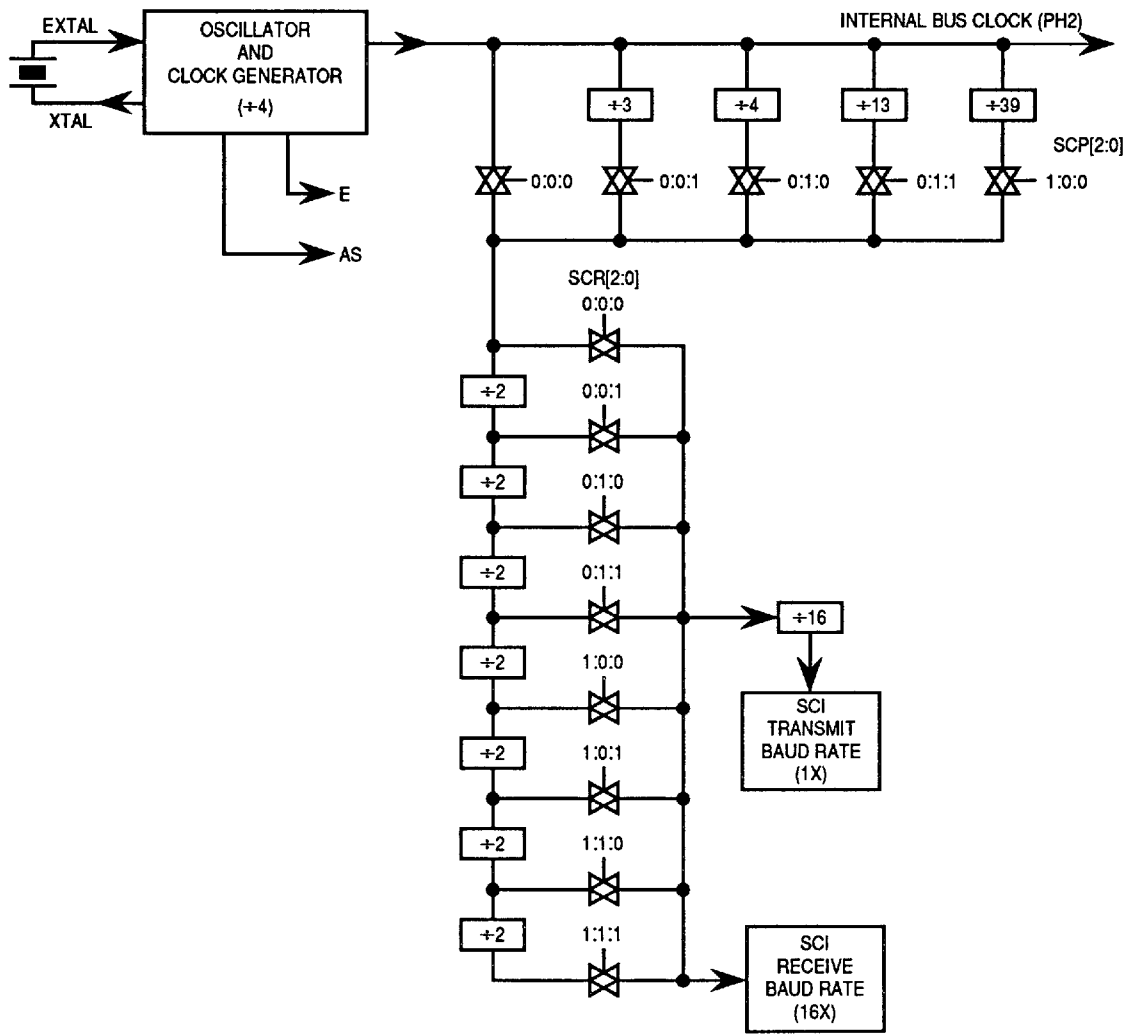
SCI Transmitter Block Diagram

SCI Receiver Block Diagram

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EXTAL

OSCILLATOR
AND
CLOCK GENERATOR
(÷4)

XTAL

E

AS

INTERNAL BUS CLOCK (PH2)

÷3   ÷4   ÷13   ÷39

SCP[2:0]

0:0:0   0:0:1   0:1:0   0:1:1   1:0:0

SCR[2:0]
0:0:0

÷2   0:0:1

÷2   0:1:0

÷2   0:1:1

÷16

÷2   1:0:0

SCI
TRANSMIT
BAUD RATE
(1X)

÷2   1:0:1

÷2   1:1:0

÷2   1:1:1

SCI
RECEIVE
BAUD RATE
(16X)

SCI BAUD GENERATOR /39

SCI Baud Generator Circuit Diagram

BAUD — Baud Rate Control Register   **$102B**

	Bit 7	6	5	4	3	2	1	Bit 0
	TCLR	SCP2	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
RESET:	0	0	0	0	0	U	U	U

TCLR — Clear Baud Rate Counters (TEST)

SCP[2:0] — SCI Baud Rate Prescaler Selects

SCP[2:0]	Divide Internal Clock By	Crystal Frequency				
		4.0 MHz	4.9152 MHz	8.0 MHz	8.3886 MHz	12.0 MHz
0 0 0	1	62500	76800	125000	131072	187500
0 0 1	3	20833	25600	41667	43691	62500
0 1 0	4	15625	19200	31250	32768	46875
0 1 1	13	4800	5907	9600	10082	14423
1 0 0	39	1602	1969	3205	3361	4808

RCKB — SCI Baud Rate Clock Check (TEST)

SCR[2:0] — SCI Baud Rate Selects
   Selects receiver and transmitter bit rate based on output from baud rate prescaler stage. Refer to SCI baud rate generator block diagram.

SCR[2:0]	Divide Prescaler By	Highest Baud Rate (Prescaler Output from Previous Table)				
		131072	76800	32768	19200	4800
0 0 0	1	131072	76800	32768	19200	4800
0 0 1	2	65536	38400	16384	9600	2400
0 1 0	4	32768	19200	8192	4800	1200
0 1 1	8	16384	9600	4096	2400	600
1 0 0	16	8192	4800	2048	1200	300
1 0 1	32	4096	2400	1024	600	150
1 1 0	64	2048	1200	512	300	75
1 1 1	128	1024	600	256	150	37.5

SCCR1 — SCI Control Register 1 $102C

	Bit 7	6	5	4	3	2	1	Bit 0
	R8	T8	—	M	WAKE	—	—	—
RESET:	U	U	0	0	0	0	0	0

R8 — Receive Data Bit 8

    0 = SCI receiver configured for 8-bit data characters.

    1 = If M bit is set, R8 stores the ninth data bit in the receive data character.

T8 — Transmit Data Bit 8

    0 = SCI transmitter configured for 8-bit data characters.

    1 = If M bit is set, R8 stores the ninth data bit in the transmit data character.

Bit 5 — Not implemented

  Always reads zero

M — Mode (Select Character Format)

    0 = Start bit, 8 data bits, 1 stop bit

    1 = Start bit, 9 data bits, 1 stop bit

WAKE — Wakeup by Address Mark/Idle

    0 = Wakeup by IDLE line recognition

    1 = Wakeup by address mark (most significant data bit set)

Bits [2:0] — Not implemented

  Always read zero

SCCR2 — SCI Control Register 2   **$102D**

Bit 7	6	5	4	3	2	1	Bit 0
TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK

RESET: 0   0   0   0   0   0   0   0

TIE — Transmit Interrupt Enable
    0 = TDRE interrupts disabled
    1 = SCI interrupt requested when TDRE status flag is set

TCIE — Transmit Complete Interrupt Enable
    0 = TC interrupts disabled
    1 = SCI interrupt requested when TC status flag is set

RIE — Receiver Interrupt Enable
    0 = RDRF and OR interrupts disabled
    1 = SCI interrupt requested when RDRF flag or the OR status flag is set

ILIE — Idle Line Interrupt Enable
    0 = IDLE interrupts disabled
    1 = SCI interrupt requested when IDLE status flag is set

TE — Transmitter Enable
    0 = Transmitter disabled
    1 = Transmitter enabled

RE — Receiver Enable
    0 = Receiver disabled
    1 = Receiver enabled

RWU — Receiver Wakeup Control
    0 = Normal SCI receiver
    1 = Wakeup enabled and receiver interrupts inhibited

SBK — Send Break
    0 = Break generator off
    1 = Break codes generated as long as SBK = 1

SCSR — SCI Status Register   **$102E**

Bit 7	6	5	4	3	2	1	Bit 0
TDRE	TC	RDRF	IDLE	OR	NF	FE	—

RESET: 1   1   0   0   0   0   0   0

TDRE — Transmit Data Register Empty Flag
    This flag is set when SCDR is empty. Clear the TDRE flag by reading SCSR1 with TDRE set and then
    writing to SCDR.
        0 = SCDR busy
        1 = SCDR empty

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TC — Transmit Complete Flag

This flag is set when the transmitter is idle (no data, preamble, or break transmission in progress). Clear the TC flag by reading SCSR1 with TC set and then writing to SCDR.

   0 = Transmitter busy
   1 = Transmitter idle

RDRF — Receive Data Register Full Flag

Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again. RDRF is set if a received character is ready to be read from SCDR. Clear the RDRF flag by reading SCSR1 with RDRF set and then reading SCDR.

   0 = SCDR empty
   1 = SCDR full

IDLE — Idle Line Detected Flag

This flag is set if the RxD line is idle. Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again. The IDLE flag is inhibited when RWU = 1. Clear IDLE by reading SCSR1 with IDLE set and then reading SCDR.

   0 = RxD line is active
   1 = RxD line is idle

OR — Overrun Error Flag

OR is set if a new character is received before a previously received character is read from SCDR. Clear the OR flag by reading SCSR1 with OR set and then reading SCDR.

   0 = No overrun
   1 = Overrun detected

NF — Noise Error Flag

NF is set if majority sample logic detects anything other than a unanimous decision. Clear NF by reading SCSR1 with NF set and then reading SCDR.

   0 = Unanimous decision
   1 = Noise detected

FE — Framing Error

FE is set when a zero is detected where a stop bit was expected. Clear the FE flag by reading SCSR1 with FE set and then reading SCDR.

   0 = Stop bit detected
   1 = Zero detected

Bit 0 — Not implemented
   Always reads zero

**SCDR** — SCI Data Register   **$102F**

	Bit 7	6	5	4	3	2	1	Bit 0
	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0
RESET:	U	U	U	U	U	U	U	U

Receive and transmit are double buffered. Reads access the receive data buffer, and writes access the transmit data buffer. When the M bit in SCCR1 is set, R8 and T8 in SCCR1 store the ninth bit in receive and transmit data characters.

Serial Peripheral Interface

The SPI allows the MCU to communicate synchronously with peripheral devices and other microprocessors. When configured as a master, data transfer rates can be as high as one-half the E clock rate (1.5 Mbits per second for a 3-MHz bus frequency). When configured as a slave, data transfers can be as fast as the E clock rate (3 Mbits per second for a 3-MHz bus frequency).

When the SPI is enabled, all pins that are defined by the configuration as inputs are inputs regardless of the state of the DDR bits for those pins. All pins that are defined as outputs will be outputs only if the DDR bits for those pins are set to one. Any SPI output whose corresponding DDR bit is set to zero can be used as a general-purpose input. If the SPI system is in master mode and DDRD bit 5 is set to one, the port D bit 5 pin becomes a general-purpose output instead of the SS input to the SPI system. The MODF mode error flag function for which SS was used becomes disabled to avoid interference between the general-purpose output function and the SPI system.

SPI Block Diagram

: ■ 6367248 0137172 94T ■
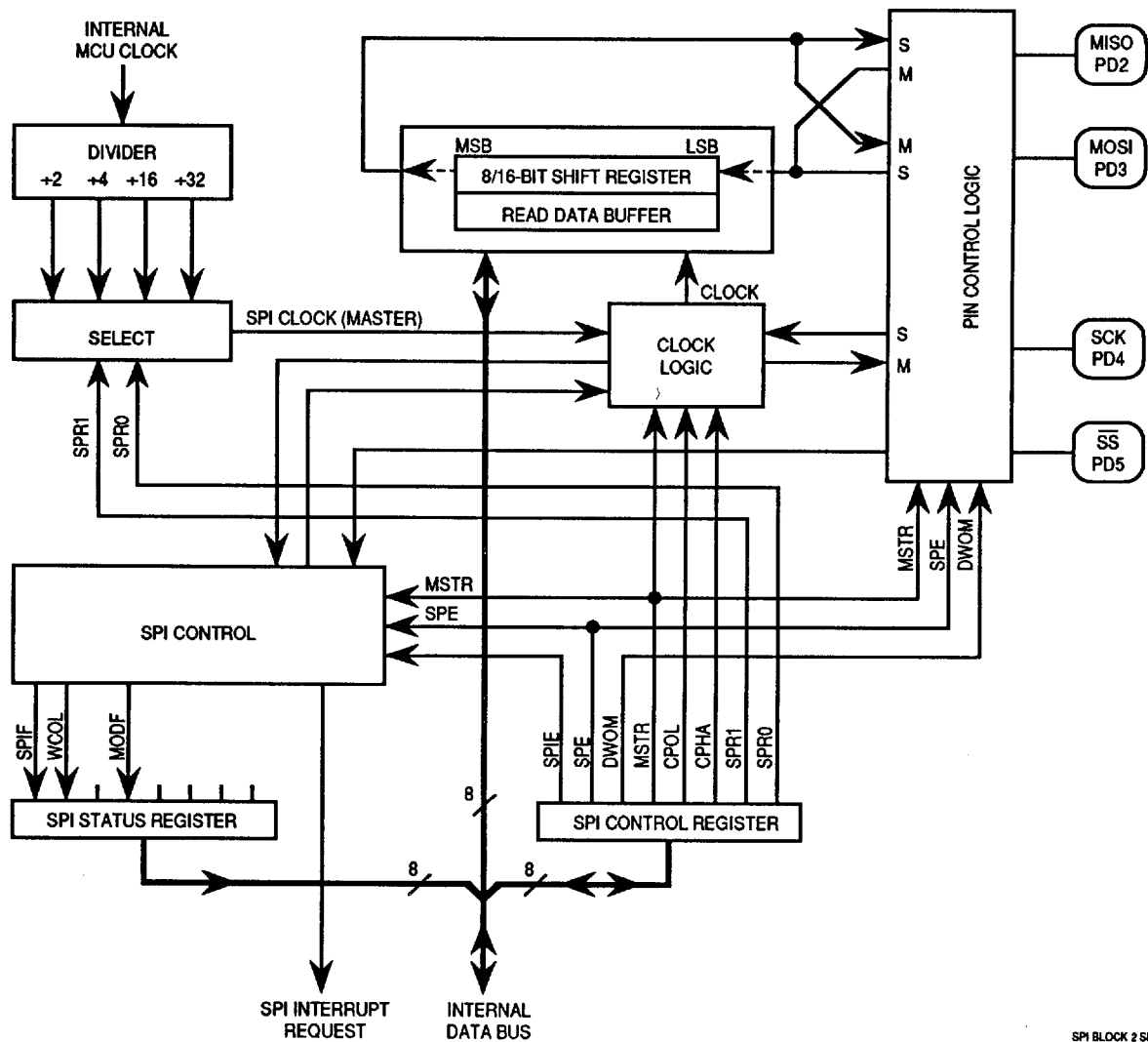
SPCR — SPI Control Register $1028

|	Bit 7	6	5	4	3	2	1	Bit 0
	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

SPIE — Serial Peripheral Interrupt Enable
    0 = SPI interrupts disabled
    1 = SPI interrupts enabled

SPE — Serial Peripheral System Enable
    0 = SPI off
    1 = SPI on

DWOM — Port D Wired-OR Mode Option for Port D Pins PD[5:0]
    See also WOMS bit in SCCR1.
        0 = Normal CMOS outputs
        1 = Open-drain outputs

MSTR — Master Mode Select
    0 = Slave mode
    1 = Master mode

CPOL, CPHA — Clock Polarity, Clock Phase
    Refer to **SPI Transfer Format**.
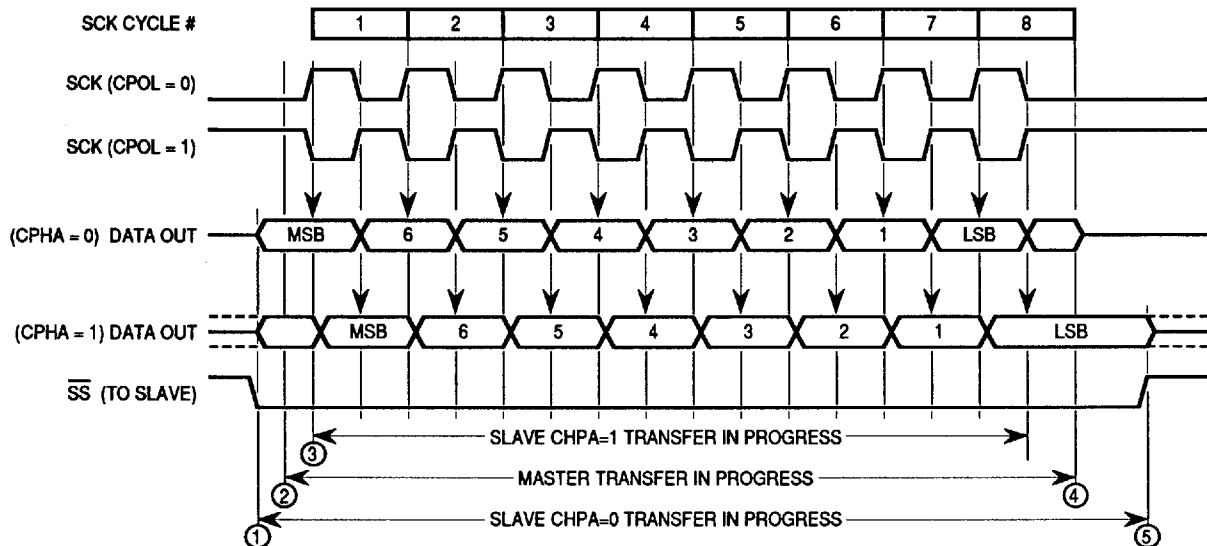
1. $\overline{SS}$ ASSERTED
2. MASTER WRITES TO SPDR
3. FIRST SCK EDGE
4. SPIF SET
5. $\overline{SS}$ NEGATED

SPI TRANSFER FORMAT 1

SPI Transfer Format

SPR[1:0] — SPI Clock Rate Selects

SPR[1:0]	E Clock Divide By	Frequency at E = 2 MHz (Baud)
0 0	2	1.0 MHz
0 1	4	500 kHz
1 0	16	125 kHz
1 1	32	62.5 kHz

SPSR — SPI Status Register $1029

Bit 7	6	5	4	3	2	1	Bit 0
SPIF	WCOL	—	MODF	—	—	—	—

RESET: 0   0   0   0   0   0   0   0

SPIF — SPI Transfer Complete Flag
    This flag is set when an SPI transfer is complete (after eight SCK cycles in a data transfer). Clear this flag by reading SPSR (with SPIF = 1), then access SPDR.
        0 = No SPI transfer complete or SPI transfer still in progress
        1 = SPI transfer complete

WCOL — Write Collision Error Flag
    This flag is set if the MCU tries to write data into SPDR while an SPI data transfer is in progress. Clear this flag by reading SPSR (WCOL = 1), then access SPDR.
        0 = No write collision error
        1 = SPDR written while SPI transfer in progress

Bit 5 — Not implemented
    Always reads zero

MODF — Mode Fault (Mode fault terminates SPI operation)
    MODF is set when $\overline{SS}$ is pulled low while MSTR = 1. Clear this flag by reading SPSR with MODF set, then write to SPCR.
        0 = No mode fault error
        1 = $\overline{SS}$ pulled low in master mode

Bits [3:0] — Not implemented
    Always read zero

SPDR — SPI Data Register $102A

| Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

SPI is double buffered in, single buffered out.

Analog-to-Digital Converter

The analog-to-digital (A/D) converter system uses an all-capacitive charge-redistribution technique to convert analog signals to digital values. The MC68HC11E20 A/D converter system, an 8-channel, multiplexed-input, successive-approximation converter, is accurate to ±1 least significant bit (LSB). It does not require external sample and hold circuits because of the type of charge-redistribution technique used.
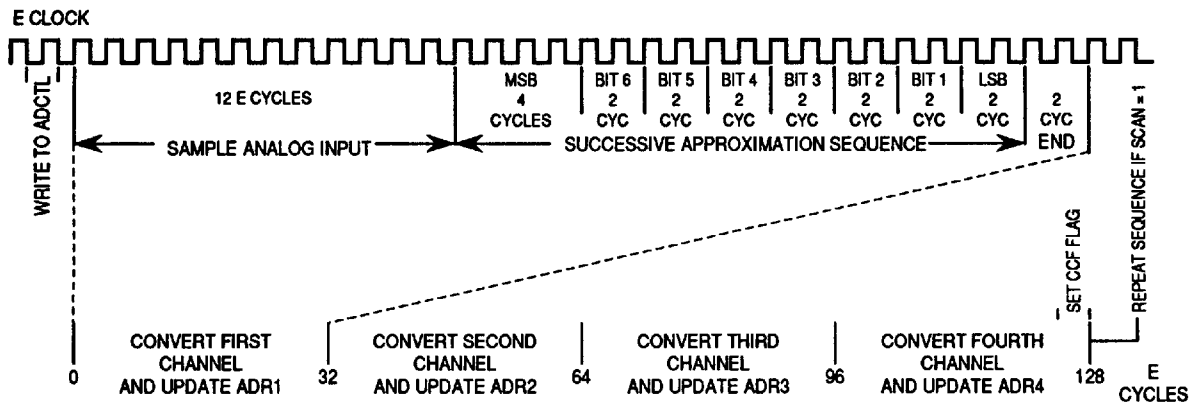
Dedicated pins V_{RH} and V_{RL} provide the reference supply voltage inputs.

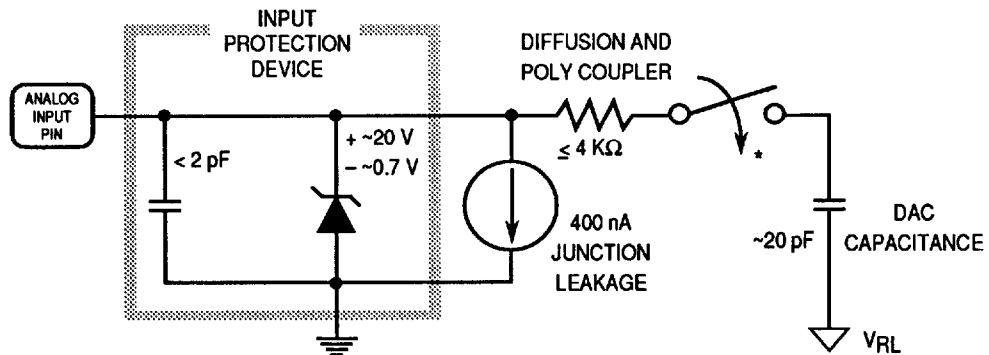A multiplexer allows the single A/D converter to select one of 16 analog signals.
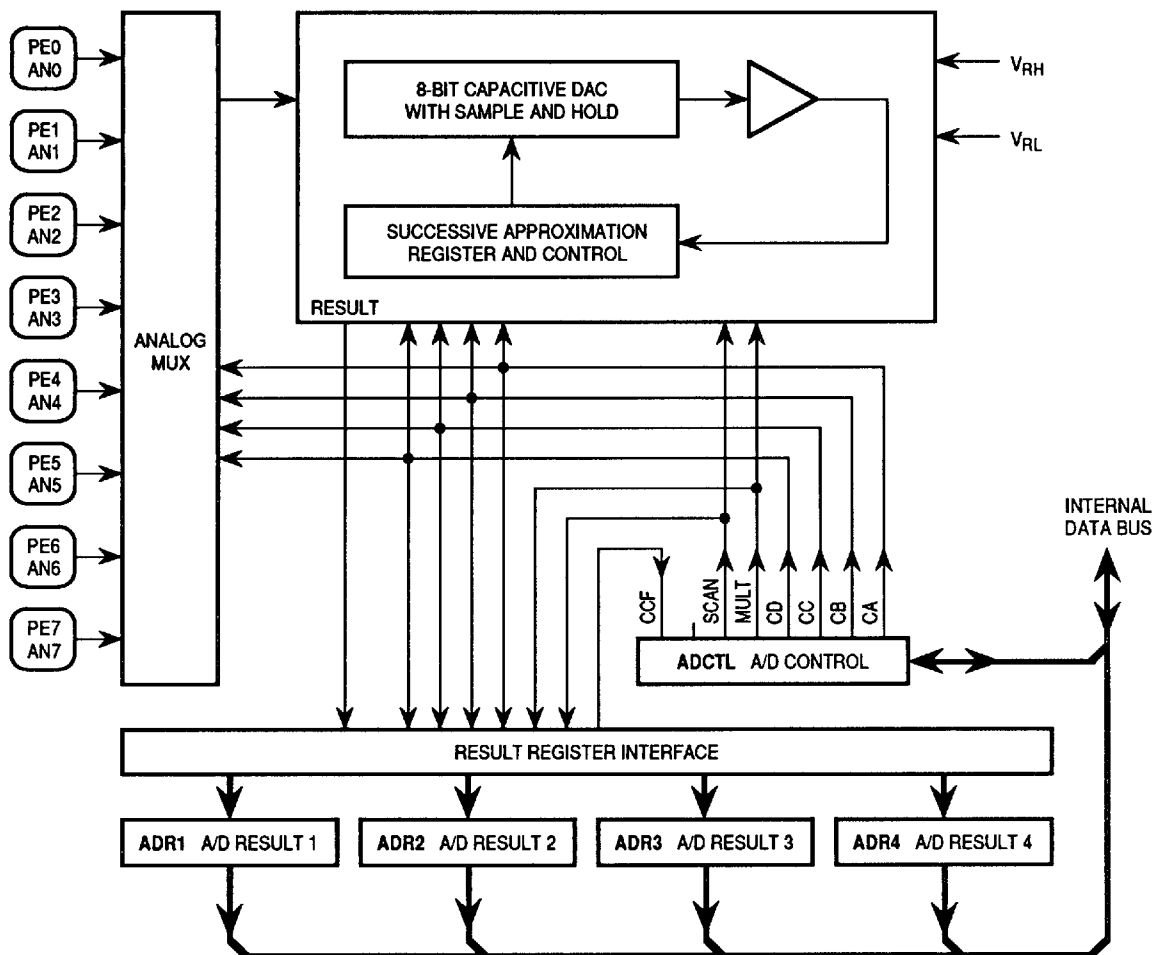
AD BLOCK

A/D Converter Block Diagram

A/D CONVERSION TIM

Timing Diagram for a Sequence of Four A/D Conversions

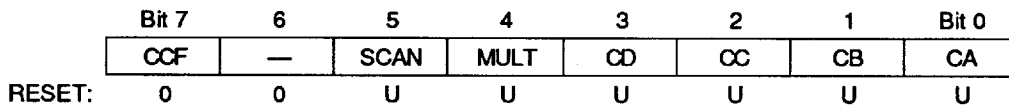*THIS ANALOG SWITCH IS CLOSED ONLY DURING THE 12-CYCLE SAMPLE TIME.

ANALOG INPUT PIN

Electrical Model of an Analog Input Pin (Sample Mode)

ADCTL — A/D Control/Status   **$1030**

Bit 7	6	5	4	3	2	1	Bit 0
CCF	—	SCAN	MULT	CD	CC	CB	CA

RESET: 0   0   U   U   U   U   U   U

CCF — Conversions Complete Flag
    CCF is set after an A/D conversion cycle and cleared when ADCTL is written.

Bit 6 — Not implemented
    Always reads zero

SCAN — Continuous Scan Control
    0 = Do four conversions and stop
    1 = Convert four channels in selected group continuously

MULT — Multiple Channel/Single Channel Control
    0 = Convert single channel selected
    1 = Convert four channels in selected group

CD:CA — Channel Select D through A

A/D Converter Channel Assignments

Channel Select Control Bits				Channel Signal	Result in ADRx if MULT = 1	Result in ADRx if MULT = 0
CD	CC	CB	CA			
0	0	0	0	AD0	ADR1	ADR[4:1]
0	0	0	1	AD1	ADR2	ADR[4:1]
0	0	1	0	AD2	ADR3	ADR[4:1]
0	0	1	1	AD3	ADR4	ADR[4:1]
0	1	0	0	AD4	ADR1	ADR[4:1]
0	1	0	1	AD5	ADR2	ADR[4:1]
0	1	1	0	AD6	ADR3	ADR[4:1]
0	1	1	1	AD7	ADR4	ADR[4:1]
1	0	0	0	Reserved	—	—
1	0	0	1	Reserved	—	—
1	0	1	0	Reserved	—	—
1	0	1	1	Reserved	—	—
1	1	0	0	V_{RH}	ADR1	ADR[4:1]
1	1	0	1	V_{RL}	ADR2	ADR[4:1]
1	1	1	0	$(V_{RH})/2$	ADR3	ADR[4:1]
1	1	1	1	Test/Reserved*	ADR4	ADR[4:1]

*Used for factory testing

ADR[1:4] — A/D Results   **$1031–$1034**

$1031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$1032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$1033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$1034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4

Analog Input to 8-Bit Result Translation Table

	Bit 7	6	5	4	3	2	1	Bit 0
% (1)	50%	25%	12.5%	6.25%	3.12%	1.56%	0.78%	0.39%
Volts (2)	2.500	1.250	0.625	0.3125	0.1562	0.0781	0.0391	0.0195

(1) % of V_{RH}–V_{RL} (2) Volts for V_{RL} = 0; V_{RH} = 5.0 V

OPTION — System Configuration Options   **$1039**

Bit 7	6	5	4	3	2	1	Bit 0
ADPU	CSEL	IRQE*	DLY*	CME	—	CR1*	CR0*

RESET: 0   0   0   1   0   0   0   0

*Can be written only once in first 64 cycles out of reset in normal modes, any time in special modes.

ADPU — A/D Converter Power-Up
   0 = A/D converter powered down
   1 = A/D converter powered up

CSEL — Clock Select
   0 = A/D and EEPROM use system E clock
   1 = A/D and EEPROM use internal RC clock

IRQE — IRQ Select Edge-Sensitive Only
   Refer to **Resets and Interrupts**.

DLY — Enable Oscillator Startup Delay
   Refer to **Resets and Interrupts**.

CME — Clock Monitor Enable
   Refer to **Resets and Interrupts**.

Bit 2 — Not Implemented
   Always reads zero

CR[1:0] — COP Timer Rate Select
   Refer to **Main Timer**.