

S-8081B

CR TIMER

The S-8081B is a CMOS CR timer developed for appliances and industrial equipment use. It consists of a CR oscillator, a 20-stage divider, a power-on clear circuit, a trigger input chattering rejection circuit, an internal voltage regulator, a level shift circuit, and an output driver. It can be used as a high-precision, long-time monostable timer.

■ Features

- Wide power supply operating range : 4.5 to 16.5 V
- Low current consumption : 200 μ A max.(C = 200 k Ω , R = 0.0047 μ F, open output)
- Time can be set by external CR
- Excellent oscillation stability because of built-in voltage regulator
- Power-on clear circuit is integrated
- Both trigger I/O inverting operation and set/reset operation can be performed

■ Applications

- Time switch
- Long time delay generator

■ Pin Arrangement and Markings

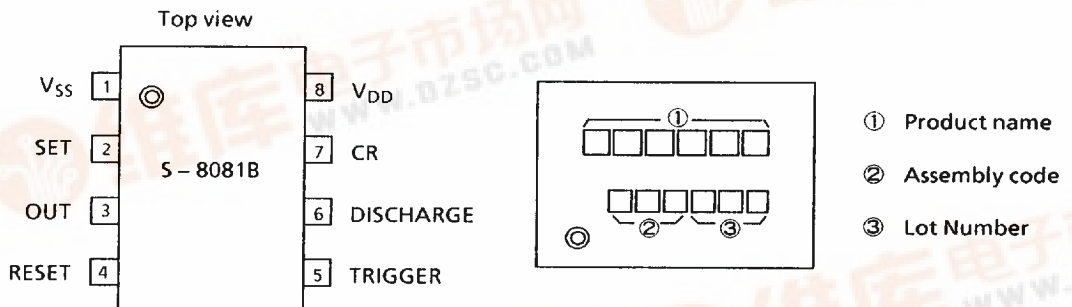


Figure 1

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■ Block Diagram

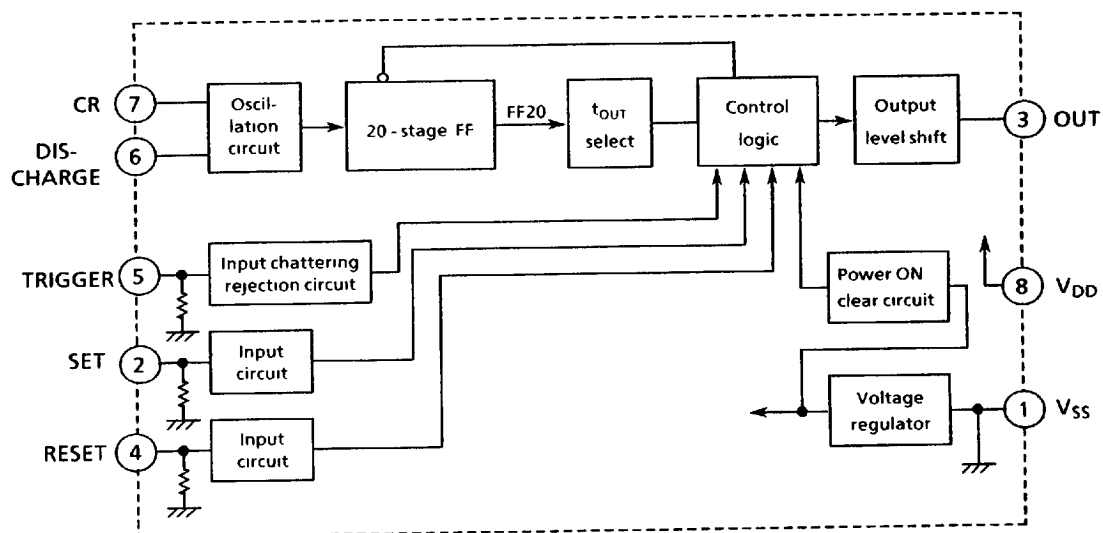
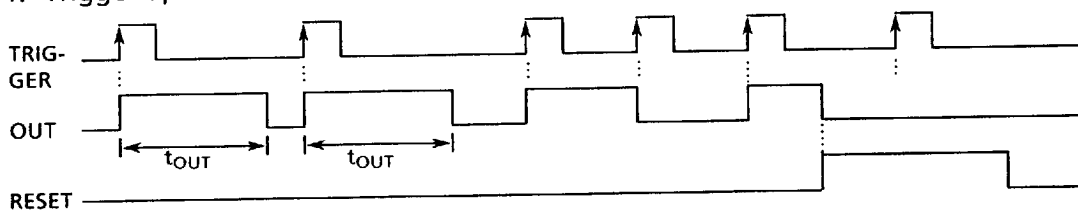


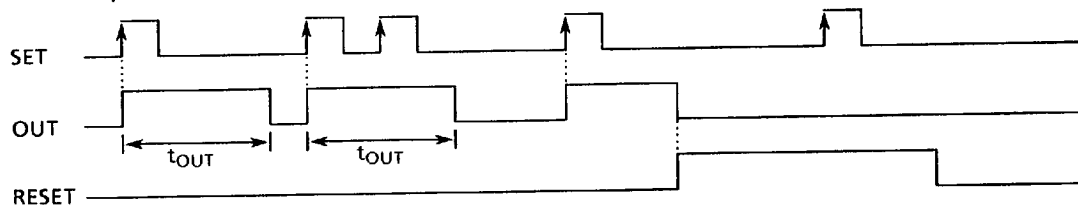
Figure 2

■ Timing Chart

1. Trigger operation



2. Set operation



$$t_{OUT} = t_{OSC} \times 2^{19}$$

$$t_{OSC} \approx K \times R_T \times C_T$$

$$R_T \geq 50 \text{ k}\Omega$$

Figure 3

■ Operation

1. SET terminal

At the rise of SET terminal, OUT goes high (V_{DD}) and frequency dividing operation starts.
This terminal has a pull-down resistor built in.

2. RESET terminal

By bringing RESET terminal high (V_{DD}), OUT goes low (V_{SS}) and the internal counter is reset.
Set or trigger input is ignored when reset is high.
This terminal has a pull-down resistor built in.

3. TRIGGER terminal

At the rise of TRIGGER terminal, OUT level is inverted. When OUT changes from low (V_{SS}) to high (V_{DD}), frequency dividing operation starts. When OUT changes from high (V_{DD}) to low (V_{SS}), the internal counter is reset. This terminal has a chattering rejection circuit and a pull-down resistor built in.

Chattering rejection time $\approx t_{osc} \times 8$

4. CR and DISCHARGE terminals

CR oscillation circuit can be constructed by connecting a timing capacitor C_T between V_{DD} and CR terminals, and by connecting a timing resistor R_T between CR and DISCHARGE terminals.

Set the oscillation period (t_{osc}) following the formula below.

$$t_{osc} = K \times R_T \times C_T$$

K : time constant coefficient

$$R_T \geq 50 \text{ k}\Omega$$

5. OUT terminal

At the rise of SET or TRIGGER terminal, OUT goes high (V_{DD}) and frequency dividing operation starts. OUT goes low (V_{SS}) after $t_{osc} \times 2^{19}$.

When OUT is high (V_{DD}) if TRIGGER rises or RESET goes high (V_{DD}), OUT goes low (V_{SS}) and the internal counter is reset.

Note: To start trigger operation when SET is in operation, the counter must be reset before TRIGGER is input.

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Absolute Maximum Ratings

Table 1

Unless otherwise specified: Ta = 25°C

Item	Symbol	Conditions	Ratings	Unit
Power supply voltage	V _{DD}	V _{SS} = 0 V	18	V
Input/output voltage*	V _{IN} , V _{OUT}		V _{SS} - 0.3 to V _{DD} + 0.3	V
Operating temperature	T _{opr}		- 30 to + 85	°C
Storage temperature	T _{stg}		- 40 to + 125	°C
Power dissipation	P _D	at 25°C	300	mW

* Excluding DISCHARGE terminal

Electrical Characteristics

Table 2

V_{DD} = 12 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating power supply voltage	V _{DD}		4.5	—	16.5	V
Operating current consumption	I _{DD}	R = 200 kΩ Open output C = 0.0047 μF	—	—	200	μA
SET, RESET, TRIGGER input pull-down resistance	R _{down}	V _{IH} = V _{DD}	50	—	400	kΩ
High level input voltage	V _{IH}		V _{DD} - 0.5	—	V _{DD}	V
Low level input voltage	V _{IL}		V _{SS}	—	V _{SS} + 0.5	
High level output current	I _{OH}	V _{OH} = 5.7 V V _{DD} = 8.0 V	10	15	—	mA
Low level output current	I _{OL}	V _{OL} = 2.3 V V _{DD} = 8.0 V	20	30	—	
Low level output voltage	V _{OL}	V _{DD} = 5.0 V I _{OUT} = 3.2mA	—	—	0.4	V
Time constant coefficient	K	C = 0.0047 μF R = 200 kΩ	1.276	1.450	1.624	—
CR osc	Power supply voltage fluctuation*	Δf/fosc / ΔV _{DD} V _{DD} = 4.5 to 16 V C = 0.0047 μF R = 200 kΩ	—	0.05	—	%/V
	Temperature fluctuation*	Δf/fosc / ΔT Ta = - 20 to + 60°C C = 0.0047 μF R = 200 kΩ	—	0.10	—	%/°C

* Fluctuation of IC only

■ Dimensions

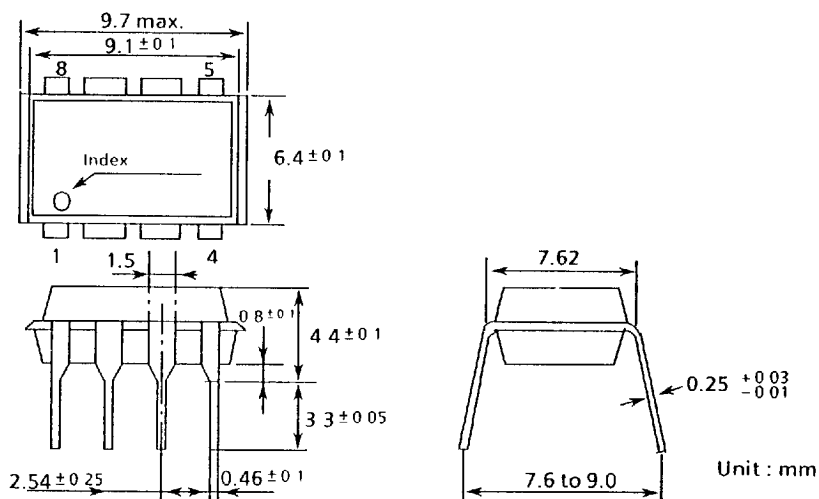


Figure 4

■ Application Circuit Example

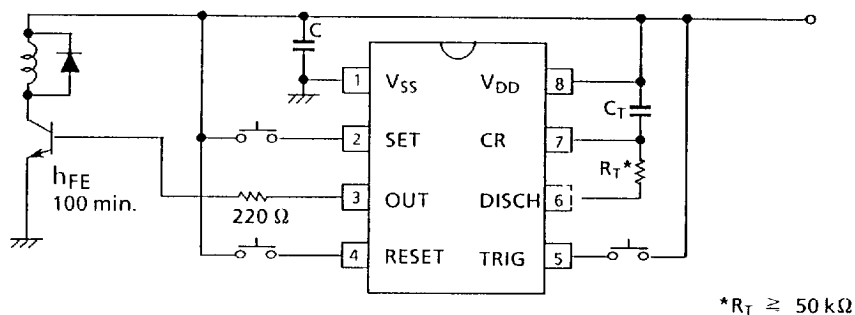


Figure 5

* $R_T \geq 50 \text{ k}\Omega$

■ Notes

- Since each of SET, RESET and TRIGGER terminal has a pull-down resistor built in, the input level should be decided in adding a value of pull-down resistance when input is pulled up.
- The S-8081B has an accelerating test mode to check its F.F. function in a shorter time. When SET or TRIGGER terminal and RESET terminal are operated with the timing shown in Figure 6, the IC enters the accelerating test mode. That is, OUT goes low faster than preset and t_{OUT} is shorter than the specified time.

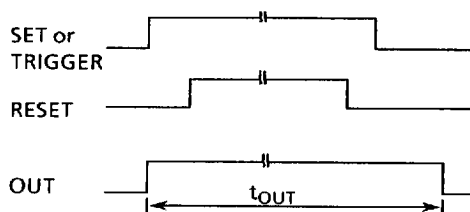


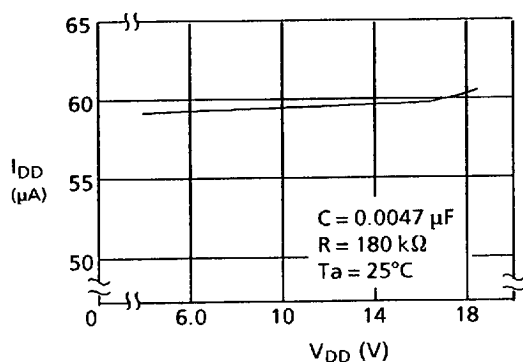
Figure 6

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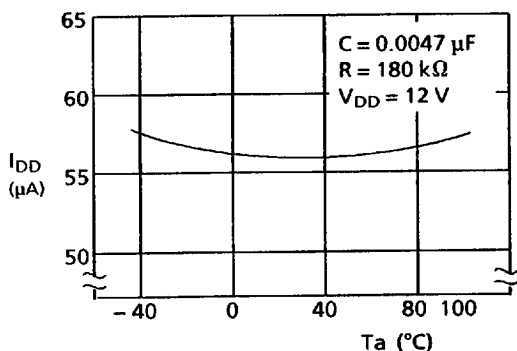
■ Characteristics

1 Current consumption characteristics

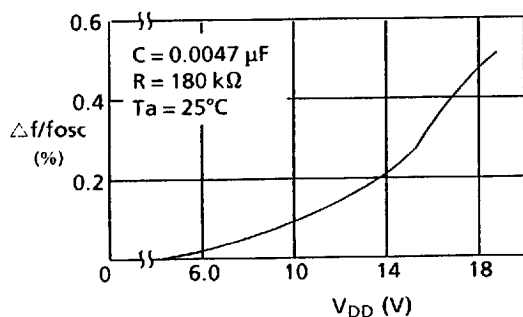
1.1 Operating current consumption I_{DD} – Power supply voltage V_{DD}



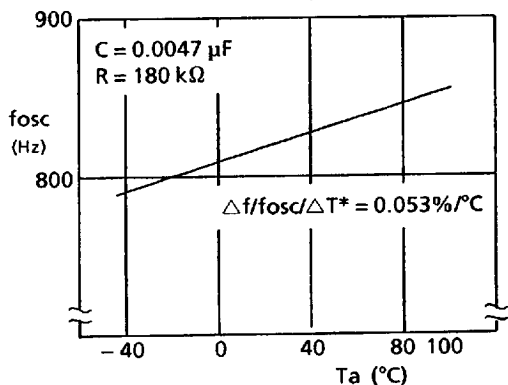
1.2 Operating current consumption I_{DD} – Ambient temperature T_a



2 Oscillation frequency $\Delta f/f_{osc}$ – Power supply voltage V_{DD}

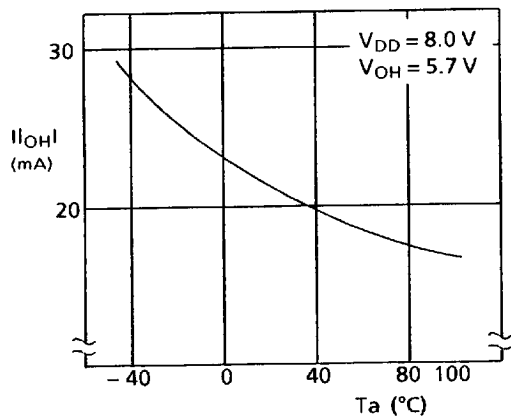


3 Oscillation frequency f_{osc} – Ambient temperature T_a

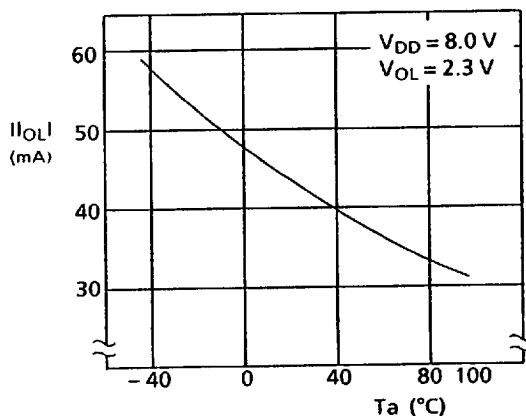


* $\Delta f/f_{osc}/\Delta T$ is fluctuation of IC only.

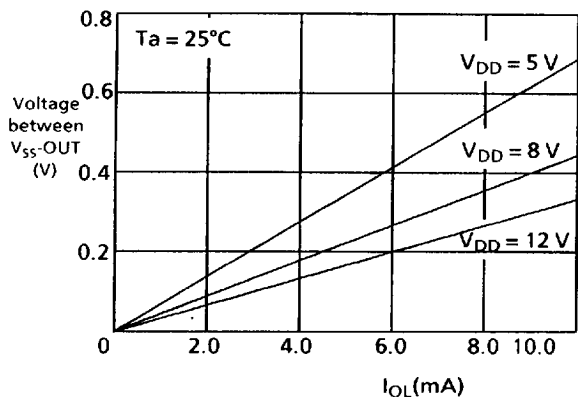
4 High level output current I_{OHL} – Ambient temperature T_a



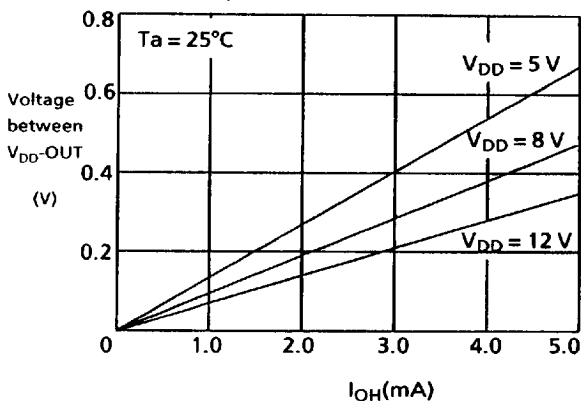
5 Low level output current I_{OL} – Ambient temperature T_a



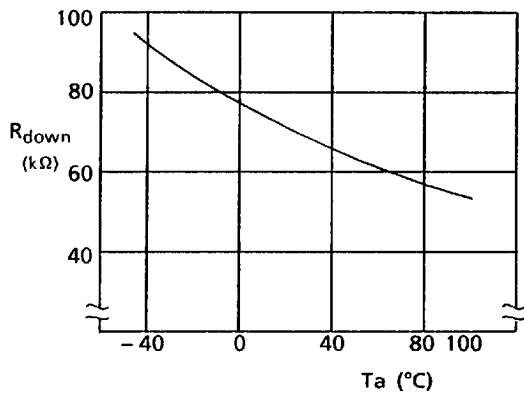
6 Output Nch driver characteristics



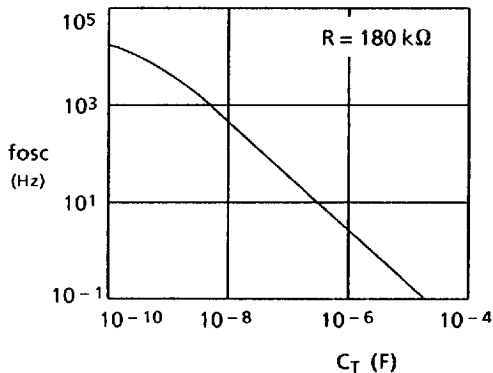
7 Output Pch driver characteristics



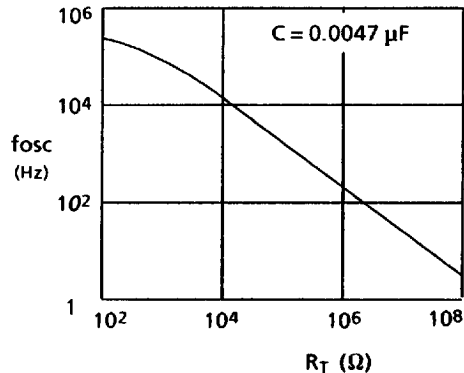
8 Pull-down resistance R_{down} - Ambient temperature T_a



9 Oscillation frequency f_{osc} - External capacitance C_T

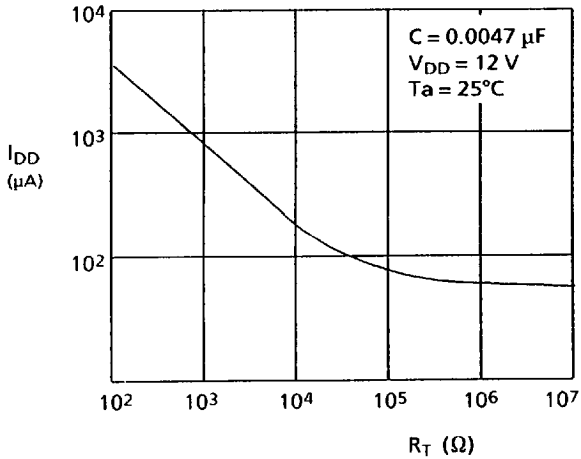


10 Oscillation frequency f_{osc} - External resistance R_T



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11 Current consumption I_{DD} -
External resistance R_T



12 Current consumption I_{DD} -
External Capacitance C_T

