19-1952; Rev 0; 1/01.

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Low-Voltage, SOT23 µP Supervisors with Power Fail In/Out, Manual Reset, and Watchdog Timer

General Description

The MAX6701–MAX6708 microprocessor (μ P) supervisory circuits reduce the complexity and components required to monitor power-supply functions in μ P systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX6701–MAX6708 family provides four functions: a reset output during power-up, power-down and brownout conditions; an independent watchdog output that goes low if the watchdog input has not been toggled within 1.6s; a 0.62V threshold detector for power-fail warning; and an active-low manual reset input.

The MAX6701–MAX6708 family offers several pinout options to accommodate a variety of multivoltage microprocessor supervision applications.

The MAX6701/MAX6702/MAX6703 monitor three supply voltages (one fixed threshold and two adjustable) to drive a single reset output and include a manual reset input and a watchdog timer with an independent output. The MAX6704 monitors a single supply voltage to drive complementary reset outputs and includes an independent adjustable power fail in/power fail out comparator, a manual reset input, and a reset based watchdog timer. The MAX6705/MAX6706/MAX6707 monitor a single supply voltage to drive a single reset output and include an independent adjustable power fail in/power fail out comparator, a manual reset input, and a reset based watchdog timer. The MAX6705/MAX6706/MAX6707 monitor a single supply voltage to drive a single reset output and include an independent adjustable power fail in/power fail out comparator, a manual reset input, and a watchdog timer with an independent output. The MAX6708 is the same as the MAX6704 but without the watchdog timer function.

Applications

Computers Controllers Intelligent Instruments Automotive Systems Critical µP Power Monitoring White Goods Networking Telecommunications

Typical Operating Circuit appears at end of data sheet.

_Features

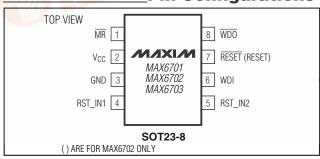
- Small 8-Pin SOT23 Package
- Precision Monitoring of +5.0V, +3.3V, +3.0V, +2.5V Supply Voltages
- 140ms Reset Timeout Delay
- Power Fail Input with Independent Output; Monitors Inputs Down to 0.62V (MAX6704– MAX6708)
- Dual Adjustable Reset Input for Triple Voltage Monitoring (MAX6701/MAX6702/MAX6703)
- 1.6s Watchdog Timeout Period (MAX6701–MAX6707)
- Independent Watchdog Output (MAX6701/MAX6702/MAX6703/MAX6705/ MAX6706/MAX6707)
- Manual Reset Input
- Four Reset Output Stage Options Active-Low Push-Pull (MAX6701, MAX6705) Active-Low Open-Drain (MAX6703, MAX6707) Active-High Push-Pull (MAX6702, MAX6706) Dual Active-Low/High Push-Pull (MAX6704, MAX6708)
- Guaranteed Reset Valid to Vcc = 1V
- Immune to Short Negative V_{CC} Transients
- Low Cost, Few External Components

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE		
MAX6701_ KA-T	-40°C to +125°C	SOT23-8		
MAX6702_ KA-T	-40°C to +125°C	SOT23-8		
MAX6703_ KA-T	-40°C to +125°C	SOT23-8		

Insert the desired suffix letter (from the Threshold Suffix Guide table) into the blank to complete the part number. All devices must be ordered in increments of 2500 pieces. Sample stock is typically held on standard versions only. Contact factory for availability.

Ordering Information continued at end of data sheet. Pin Configurations



Pin Configurations continued at end of data sheet.

_ Maxim Integrated Products 1

or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

V _{CC}	0.3V to +6.0V
Open-Drain RESET, WDO, PFO .	
Push-Pull RESET, RESET, WDO, I	PFO0.3V to (V _{CC} + 0.3V)
MR, WDI, PFI, RST_IN1, RST_IN2	0.3V to (V _{CC} + 0.3V)
Input Current (V _{CC})	20mÅ
Output Current (RESET, RESET, F	

Continuous Power Dissipation (T_A = +70°C) 8-Pin SOT23 (derate 8.9mW/°C above +70°C)......714mW Operating Temperature Range40°C to +125°C Junction Temperature+150°C Storage Temperature Range65°C to +150°C Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.25V to +5.5V for L/M versions, V_{CC} = +2.55V to +3.6V for the T/S/R versions, V_{CC} = +2.1V to +2.75V for the Z/Y versions. T_A = -40°C to +125°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CON	MIN	ТҮР	МАХ	UNITS		
		$T_A = 0^{\circ}C$ to $+125^{\circ}C$		1.0		5.5		
Operating Voltage Range	Vcc	$T_A = -40^{\circ}C \text{ to } +125^{\circ}C$	°C	1.2		5.5	V	
		V _{CC} < 5.5V, no load			12	25		
Supply Current MR Unconnected	Icc	V _{CC} < 3.6V, no load	1		9	20	μA	
Wirt Oneonneeted		V _{CC} < 3.6V, no load	I (MAX6708 only)		6	20		
		MAX670_L	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	4.50	4.63	4.75		
			$T_A = -40^{\circ}C \text{ to } + 125^{\circ}C$	4.47		4.78		
		MAX670_M	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	4.25	4.38	4.50		
			$T_A = -40^{\circ}C \text{ to } + 125^{\circ}C$	4.22		4.53		
V _{CC} Reset Threshold (V _{CC} falling)		MAX670_T	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	3.00	3.08	3.15	- V	
	VTH		$T_A = -40^{\circ}C \text{ to } + 125^{\circ}C$	2.97		3.17		
		MAX670_S	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	2.85	2.93	3.00		
			$T_A = -40^{\circ}C \text{ to } + 125^{\circ}C$	2.83		3.02		
		MAX670_R	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	2.55	2.63	2.70		
			$T_A = -40^{\circ}C \text{ to } + 125^{\circ}C$	2.53		2.72		
		MAX670_Z	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	2.25	2.32	2.38		
			$T_A = -40^{\circ}C \text{ to } + 125^{\circ}C$	2.24		2.40		
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	2.12	2.19	2.25		
		MAX670_Y	$T_A = -40^{\circ}C \text{ to } + 125^{\circ}C$	2.11		2.27		
Reset Threshold Temperature Coefficient	ΔV_{TH}				60		ppm/°C	
V _{CC} to Reset Output Delay		V _{CC} falling at 10mV	/µs		12		μs	
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	140	200	280		
Reset Timeout Period	t _{RP}		$T_A = -40^{\circ}C \text{ to } + 125^{\circ}C$	120		300	ms	
PFI, RST_IN1, RST_IN2			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	602	618	634		
Threshold		$V_{CC} = 1.8V$ to 5.5V	$T_A = -40^{\circ}C \text{ to } + 125^{\circ}C$	593		642	- mV	
PFI, RST_IN1, RST_IN2 Hysteresis					6		mV	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.25V to +5.5V for L/M versions, V_{CC} = +2.55V to +3.6V for the T/S/R versions, V_{CC} = +2.1V to +2.75V for the Z/Y versions. T_A = -40°C to +125°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL		MIN	ТҮР	МАХ	UNITS			
PFI, RST_IN1, RST_IN2 Leakage			$T_{A} = -40^{\circ}C \text{ to } +85^{\circ}C$	-50		+50			
Current		(Note 2)	T _A = -40°C to +125°C	-200		+200	nA		
PFI to PFO Delay	tPF				1		μs		
	VIL				0	.3 x Vcc			
MR Input Voltage	VIH			0.7 x V _C)		V		
MR Minimum Input Pulse				1			μs		
MR Glitch Rejection					100		ns		
MR to Reset Delay	t _{MD}			Ì	200		ns		
MR Pullup Resistance				25	50	75	kΩ		
Watahdag Timagut Pariod		$T_A = -40^{\circ}C$ to +	-85°C	1.12	1.6	2.4			
Watchdog Timeout Period	twd	$T_A = -40^{\circ}C$ to +	-125°C	0.96		2.52	S		
WDI Pulse Width	twdi	(Note 2)		50			ns		
	VIL				0	.3 x V _{CC}	Vcc ,,		
WDI Input Voltage	VIH			0.7 x V _C	2		- V		
WDI Input Current	Iwdi	$WDI = 0 \text{ or } V_{CC}$		-1		+1	μA		
RESET, WDO Output Low	V _{OL}	$V_{CC} \ge 1.0V$, ISIN (T _A = 0°C to +1			0.3				
		$V_{CC} \ge 1.2V$, ISIN	νκ = 100μA, output asserted			0.3	V		
(Push-Pull or Open-Drain)		V _{CC} ≥ 2.55V, I _{SI}			0.3]			
		V _{CC} ≥ 4.25V, I _{SI}	NK = 3.2mA, output asserted			0.4			
		V _{CC} ≥ 1.80V, I _{SI}			0.3	v			
PFO Output Low	VOL	V _{CC} ≥ 2.55V, I _{SI}			0.3				
(Push-Pull or Open-Drain)		V _{CC} ≥ 4.25V, I _{SI}			0.4	Ì			
RESET, WDO, PFO Output High		$V_{CC} \ge 2.7V, I_{SIN}$ asserted	0.8 x V _C	0					
(Push-Pull Only)	V _{OH}	V _{CC} ≥ 4.75V, I _S asserted	0.8 x V _C	0		V			
RESET, WDO, PFO Output Open-Drain Leakage Current	I _{LKG}	$V_{CC} > V_{TH}$, output not asserted				1.0	μA		
	(Та Vcc Voн Vcc	$V_{CC} \ge 1.0V$, I_{SC} ($T_A = 0^{\circ}C$ to +1	0.8 × V _C	C					
RESET Output High (Push-Pull		$V_{CC} \ge 1.2V, I_{SC}$	0.8 × V _C	C		v			
Only)		$V_{CC} \ge 2.55V, I_S$ asserted	0.8 x V _C	D		v			
		V _{CC} ≥ 4.25V, I _S asserted	OURCE = 800µA, reset	0.8 x V _C	0				

ELECTRICAL CHARACTERISTICS (continued)

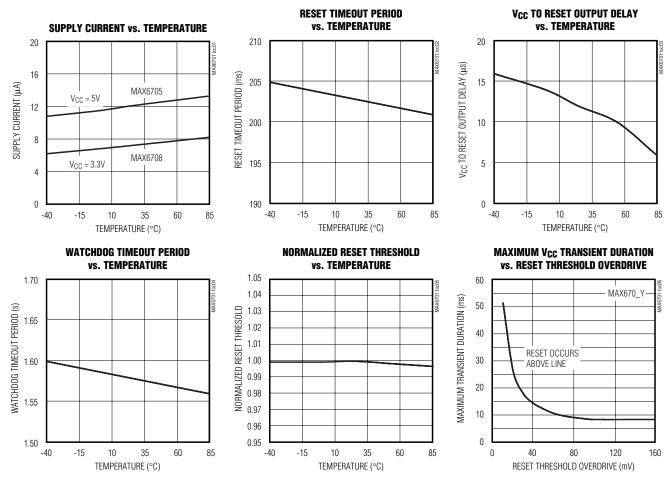
 $(V_{CC} = +4.25V \text{ to } +5.5V \text{ for L/M versions}, V_{CC} = +2.55V \text{ to } +3.6V \text{ for the T/S/R versions}, V_{CC} = +2.1V \text{ to } +2.75V \text{ for the Z/Y versions}.$ T_A = -40°C to +125°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		TYP	MAX	UNITS
RESET Output Low (Push-Pull	Mai	$V_{CC} \ge 2.7V$, $I_{SINK} = 1.2mA$, reset not asserted			0.3	V
Only)	Vol	$V_{CC} \ge 4.75V$, $I_{SINK} = 3.2mA$, reset not asserted			0.4	v

Note 1: Over temperature limits are guaranteed by design and not production tested. Devices are tested at $T_A = +25^{\circ}C$. **Note 2:** Guaranteed by design. Not production tested.

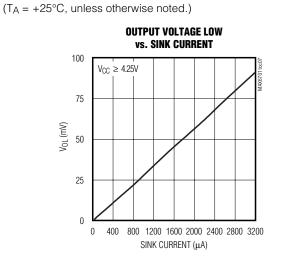
$(T_A = +25^{\circ}C, unless otherwise noted.)$

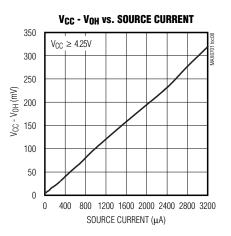
Typical Operating Characteristics



M/IXI/M







Pin Description

MAX6701 MAX6702 MAX6703	MAX6704	MAX6705 MAX6706 MAX6707	MAX6708	NAME	FUNCTION
1	1	1	1	MR	Active-Low, Manual Reset Input, Internal $50k\Omega$ Pullup to V _{CC} . Pull low to force a reset. Reset remains active as long as $\overline{\text{MR}}$ is low and for the reset timeout period after $\overline{\text{MR}}$ goes high. Leave unconnected or connect to V _{CC} if unused.
2	2	2	2	V _{CC}	Supply Voltage for MAX6701–MAX6708 and Input for Primary Reset Threshold Monitor. Push-pull outputs are powered by V_{CC}
3	3	3	3	GND	Ground
_	4	4	4	PFI	Power Fail Voltage Monitor Input. High-impedance input for internal power fail comparator. Connect this pin to an external resistive divider network to set the reset threshold voltage; $0.62V$ (typ) threshold. Connect to GND or V _{CC} when not used.
_	5	5	5	PFO	Power Fail Monitor Output. Open-drain or push-pull active-low. PFO goes low when PFI is less than 0.62V.
6	6	6	_	WDI	Watchdog Input. If WDI remains high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and WDO is asserted on the MAX6704 (resets are asserted for the reset timeout period). The internal watchdog timer clears whenever reset is asserted, or WDI sees a rising or falling edge. The watchdog function cannot be disabled.
	—		6	N.C.	No Connection

Pin	Description	(continued)
. – – – –		

MAX6701 MAX6702 MAX6703	MAX6704	MAX6705 MAX6706 MAX6707	MAX6708	NAME	FUNCTION
7	7	7	7	RESET	Active-Low Reset Output (Open-Drain or Push-Pull). RESET changes from high to low when the V _{CC} input drops below the selected reset threshold (or RST_IN1/ RST_IN2 for the MAX6701/MAX6702/MAX6703), MR is pulled low, or the watchdog triggers a reset (MAX6704 only). RESET remains low for the reset timeout period after the reset conditions are terminated.
8	_	8	—	WDO	Active-Low Watchdog Output (Open-Drain or Push-Pull). $\overline{\text{WDO}}$ is asserted whenever the watchdog times out and does not deassert until the watchdog is cleared. $\overline{\text{WDO}}$ also asserts when V _{CC} or RST_IN_ are below reset thresholds or $\overline{\text{MR}}$ is pulled low. $\overline{\text{WDO}}$ deasserts after a valid WDI transition (without a reset timeout period).
7*	8	7*	8	RESET	Active-High Reset Output (Push-Pull). RESET changes from low to high when the V _{CC} input drops below the selected reset threshold (or RST_IN1/RST_IN2 for MAX6701/MAX6702/MAX6703), MR is pulled low, or the watchdog triggers a reset (MAX6704 only). RESET remains high for the reset timeout period after the reset conditions are terminated. *RESET active-high for the MAX6702/MAX6706.
4	_	_	_	RST_IN1	Input for User Adjustable V _{CC2} Monitor. High-impedance input for second internal reset comparator. Connect this pin to an external resistive-divider network to set the reset threshold voltage; 0.62V (typ) threshold. Connect to V _{CC} when not used. Reset is asserted when either V _{CC} , RST_IN1, or RST_IN2 are below threshold.
5	_	_	_	RST_IN2	Input for User Adjustable V_{CC3} Monitor. High-impedance input for third internal reset comparator. Connect this pin to an external resistive-divider network to set the reset threshold voltage; 0.62V (typ) threshold. Connect to V_{CC} when not used. Reset is asserted when either V_{CC} , RST_IN1, or RST_IN2 are below threshold.

Detailed Description

Reset Output

A microprocessor's (μ P's) reset input starts the μ P in a known state. The MAX6701–MAX6708 assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{\text{RESET}}$ is a guaranteed logic low of 0.4V or less. As V_{CC} rises, $\overline{\text{RESET}}$

stays low. After V_{CC} rises above the reset threshold, an internal timer holds RESET low for about 200ms. RESET pulses low whenever V_{CC} dips below the reset threshold, including brownout conditions. If a brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. On power-down, once V_{CC} falls below the reset threshold, RESET stays low and is guaranteed to be 0.4V or less, until V_{CC} drops below 1V.

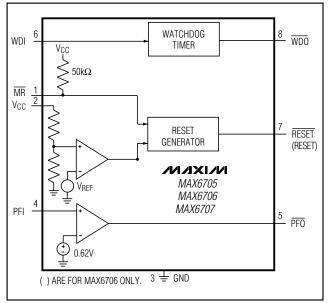


Figure 1. MAX6705/MAX6706/MAX6707 Block Diagram

The MAX6702/MAX6704/MAX6706/MAX6708 activehigh RESET output is simply the complement of the RESET output, and is guaranteed to be valid with V_{CC} down to 1V. (See Figure 4.)

Watchdog Timer

The MAX6701–MAX6707 watchdog circuit monitors the μ P's activity. If the μ P does not toggle the watchdog input (WDI) within 1.6s, WDO goes low. When RESET is asserted, the watchdog timer stays cleared and does not count. As soon as reset is released, the timer will start counting. WDO deasserts after a valid transition is detected at WDI. Pulses as short as 50ns can be detected.

Typically, \overline{WDO} will be connected to the nonmaskable interrupt (NMI) input of a μ P. When V_{CC} drops below the reset threshold, \overline{WDO} will go low whether or not the watchdog timer has timed out yet. Normally this would trigger an NMI, but RESET goes low simultaneously, and thus overrides the NMI.

The MAX6704 watchdog circuit does not have an independent watchdog output (WDO). If the μ P does not toggle the watchdog input within 1.6s, the MAX6704 will assert a reset output pulse for the reset timeout period. (See Figure 5.)

Manual Reset

The manual reset input (\overline{MR}) allows reset to be triggered by a pushbutton switch. The switch is effectively

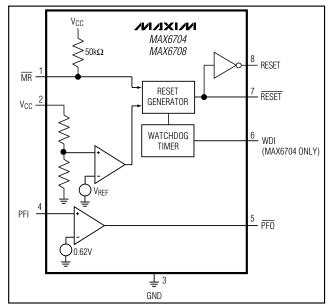


Figure 2. MAX6704/MAX6708 Block Diagram

debounced by the reset pulse width. MR is CMOS logic compatible, so it can be driven by an external logic line. MR can be used to force a watchdog timeout to generate a reset pulse in the MAX6701–MAX6708. Simply connect WDO to MR.

Power-Fail Comparator

The uncommitted power-fail comparator can be used for various purposes because its noninverting input and output are externally available. The inverting input is internally connected to a 0.62V reference. To build an early warning circuit for power failure, connect the PFI pin to a voltage divider (see *Typical Operating Circuit*). Choose the voltage-divider ratio so that the voltage at PFI falls below 0.62V just before the regulator drops out. Use PFO to interrupt the μ P so it can prepare for an orderly power-down. The low input current at this pin allows for large resistor values in the divider.

Reset-In Information

The MAX6701/MAX6702/MAX6703 include two adjustable reset inputs for monitoring up to a total of three system voltages (including V_{CC}). The thresholds for the monitored RST_IN supplies are externally set with resistor-divider networks (Figure 6). The reset output is asserted if any of the monitored supplies (V_{CC}, RST_IN1, or RST_IN2) go below its specified threshold and remain asserted for the reset timeout period after all supplies are above their thresholds.



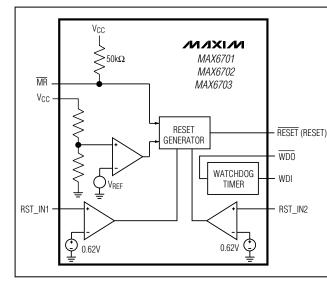


Figure 3. MAX6701/MAX6702/MAX6703 Block Diagram

Applications Information

Ensuring a Valid RESET Output Down to VCC = 0

When V_{CC} falls below 1V, the MAX6701–MAX6708 RESET output no longer sinks current—it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pulldown resistor is added to the RESET pin as shown in Figure 7, any stray charge or leakage currents will be drained to ground, holding RESET low. A resistor value (R1) is not critical; $100k\Omega$ is large enough not to load RESET and small enough to pull RESET to ground. This application works for push-pull output only (not for open-drain resets).

Monitoring Other System Voltages

Other systems can be monitored by connecting a voltage divider to PFI and adjusting the ratio appropriately. In noisy systems, a capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. Reset can be asserted on other voltages in addition to the V_{CC} supply line. Connect PFO to MR to initiate a reset output pulse when PFI drops below 0.62V. Figure 8 shows the MAX6701–MAX6708 configured to assert a reset output when the secondary supply falls below the reset threshold.

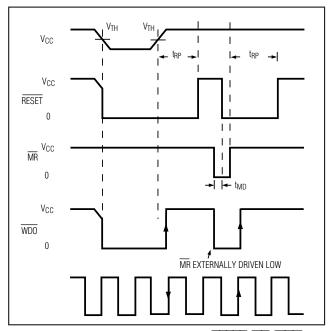


Figure 4. MAX6705/MAX6706/MAX6707 RESET, MR, WDO, and WDI Timing. The MAX6706 RESET output is the inverse of the RESET shown.

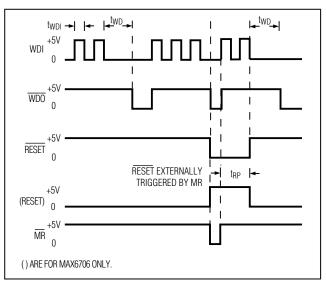


Figure 5. MAX6705/MAX6706/MAX6707 Watchdog Timing

MAX6701-MAX6708

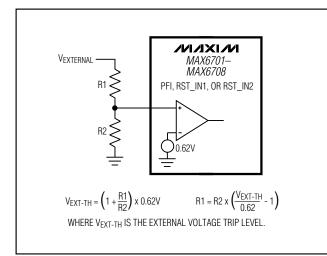
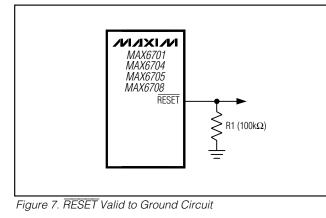


Figure 6. Calculating Adjustable Voltage Thresholds



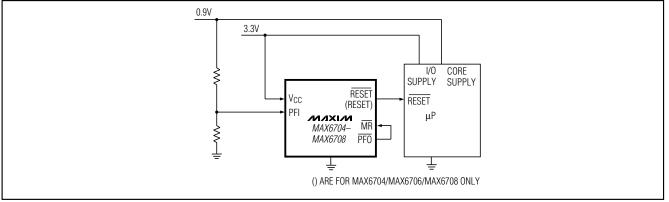


Figure 8. Monitoring Other System Voltages

Threshold Suffix Guide

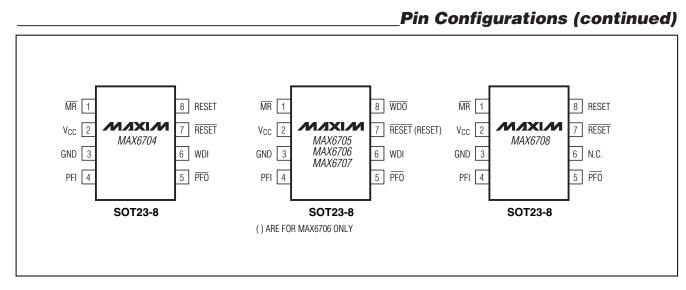
SUFFIX	RESET THRESHOLD (V)			
L	4.63			
Μ	4.38			
Т	3.08			
S	2.93			
R	2.63			
Z	2.32			
Y	2.19			

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX6704 _KA-T	-40°C to +125°C	SOT23-8
MAX6705_ KA-T	-40°C to +125°C	SOT23-8
MAX6706_ KA-T	-40°C to +125°C	SOT23-8
MAX6707_ KA-T	-40°C to +125°C	SOT23-8
MAX6708_ KA-T	-40°C to +125°C	SOT23-8

Bold indicates standard version.





Selector Guide

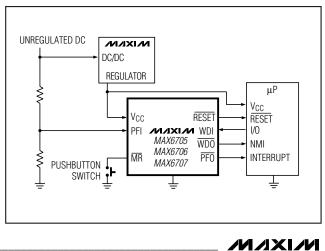
PART	RESET PP-LOW	RESET PP-HIGH	RESET OD-LOW	WDI	WDO	PFI, PFO	RST_IN1, RST_IN2
MAX6701	~			~	✔ PP		~
MAX6702		~		~	🖌 PP		~
MAX6703			~	~	V OD		~
MAX6704	~	~		~		✔ PP	
MAX6705	~			~	V PP	✔ PP	
MAX6706		~		~	✔ PP	✔ PP	
MAX6707			~	~	V OD	V OD	
MAX6708	~	~				✔ PP	

PP = Push-Pull OD = Open-Drain

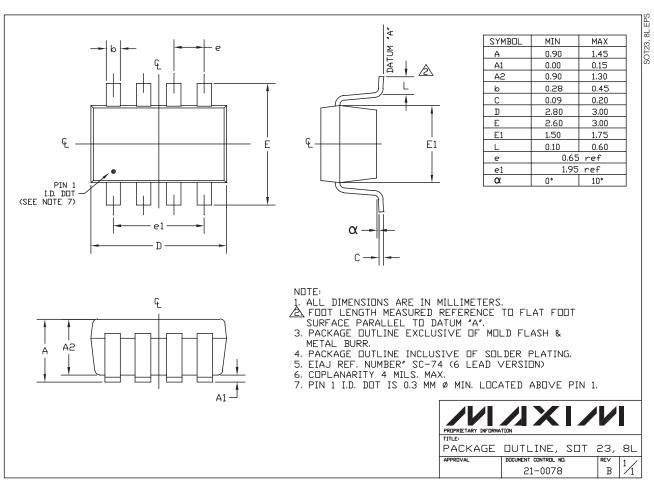
Chip Information

TRANSISTOR COUNT: 716 PROCESS: BICMOS

Typical Operating Circuit



MAX6701-MAX6708



Package Information MAX6701-MAX6708

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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_ 11