Winbond Electronics Corp.

128K × 8 CMOS STATIC RAM

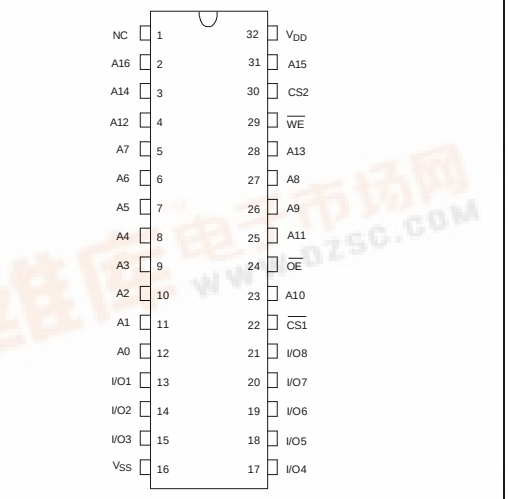
GENERAL DESCRIPTION

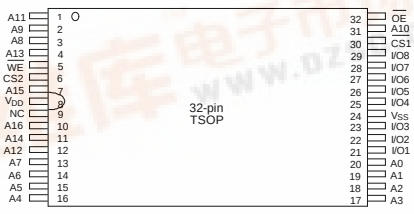
The W24010 is a normal-speed, very low-power CMOS static RAM organized as 131072 × 8 bits that operates on a wide voltage range from 2.7V to 5.5V power supply. The W24010 family, W24010-70LE and W24010-70LI, can meet the requirement of various operating temperature. This device is manufactured using Winbond's high performance CMOS technology.

FEATURES

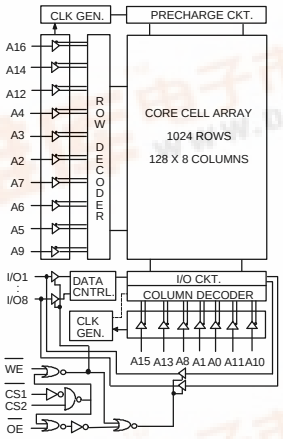
- Low power consumption:
  - Active: 350 mW (max.)
  - Standby: 15 µW (max.) /3V
    50 µW (max.) /5V
- Access time: 70 nS (max.) /5V
  100 nS (max.) /3V
- Single 3V/5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Packaged in 32-pin 600 mil DIP, 450 mil SOP, standard type one TSOP (8 mm × 20 mm) and small type one TSOP (8 mm × 13.4 mm)

PIN CONFIGURATIONS





BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A16	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
$\overline{CS1}$, CS2	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

Publication Release Date: November 1998
Revision A6

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	MODE	I/O1- I/O8	V_{DD} CURRENT
H	X	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
X	L	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High Z	I_{DD}
L	H	L	H	Read	Data Out	I_{DD}
L	H	X	L	Write	Data In	I_{DD}

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER		RATING	UNIT
Supply Voltage to V_{SS} Potential		-0.5 to +7.0	V
Input/Output to V_{SS} Potential		-0.5 to V_{DD} +0.5	V
Allowable Power Dissipation		1.0	W
Storage Temperature		-65 to +150	°C
Operating Temperature	LE	-20 to 85	°C
	LI	-40 to 85	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5V ±10%; V_{DD} = 3V ±10%; V_{SS} = 0V; T_A (°C) =-20 to 85 for LE, -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	5V			3V			UNIT
			MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
Input Low Voltage	V_{IL}	-	-0.5	-	+0.8	-0.5	-	+0.6	V
Input High Voltage	V_{IH}	-	+2.2	-	V_{DD} +0.5	+2.0	-	V_{DD} +0.5	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}	-1	-	+1	-1	-	+1	µA
Output Leakage Current	I_{LO}	VI/O = V_{SS} to V_{DD}, $\overline{CS1}$ = V_{IH} (min.) or CS2 = V_{IL} (max.) or $\overline{OE}$ = V_{IH} (min.) or $\overline{WE}$ = V_{IL} (max.)	-1	-	+1	-1	-	+1	µA
Output Low Voltage	V_{OL}	I_{OL} = +2.1 mA	-	-	0.4	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0 mA	2.4	-	-	2.2	-	-	V

Operating Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS	5V			3V			UNIT
			MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
Operating Power Supply Current	I_{DD}	$\overline{CS1}$ = V_{IL} (max.) and CS2 = V_{IH} (min.) I/O = 0 mA Cycle = min. Duty = 100%	-	-	70	-	-	30	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$ = V_{IH} (min.) or CS2 = V_{IL} (max.) Cycle = min. Duty = 100%	-	-	3	-	-	1	mA
	I_{SB1}	$\overline{CS1}$ ≥ V_{DD} -0.2V or CS2 ≤ 0.2V	-	1.0	10	-	0.5	5	µA

Note: Typical parameter is measured under ambient temperature T_A = 25° C and V_{DD} = 5V/ 3V

CAPACITANCE

(V_{DD} = 5 V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	8	pF

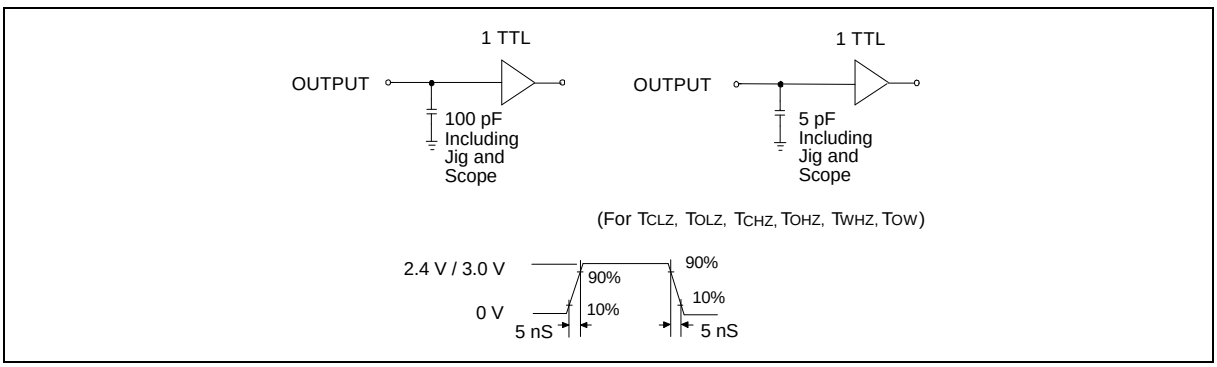
Note: These parameters are sampled but not 100% tested.

AC Characteristics

AC Test Conditions

PARAMETER		CONDITIONS
Input Pulse Levels	3V	0V to 2.4V
	5V	0V to 3.0V
Input Rise and Fall Times		5 nS
Input and Output Timing Reference Level		1.5V
Output Load		See the drawing below

AC Test Loads and Waveform



AC Characteristics, continued

(V_{DD} = 5 V ±10%; V_{DD} = 3 V ±10%; V_{SS} = 0 V; T_A (°C) =-20 to 85 for LE, -40 to 85 for LI)

Read Cycle

PARAMETER	SYM.	5 V		3 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	100	-	nS
Address Access Time	T_{AA}	-	70	-	100	nS
Chip Select Access Time	T_{ACS}	-	70	-	100	nS
Output Enable to Output Valid	T_{AOE}	-	35	-	50	nS
Chip Selection to Output in Low Z	T_{CLZ}*	10	-	15	-	nS
Output Enable to Output in Low Z	T_{OLZ}*	5	-	5	-	nS
Chip Deselection to Output in High Z	T_{CHZ}*	-	30	-	35	nS
Output Disable to Output in High Z	T_{OHZ}*	-	30	-	35	nS
Output Hold from Address Change	T_{OH}	10	-	15	-	nS

* These parameters are sampled but not 100% tested

Write Cycle

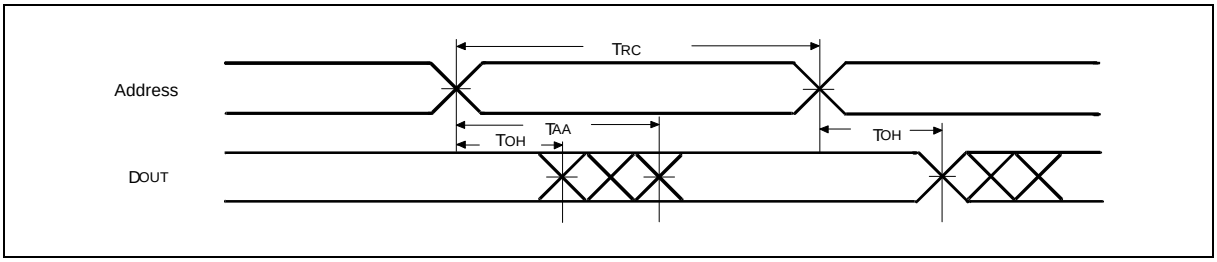
PARAMETER	SYM.	5 V		3 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	T_{WC}	70	-	100	-	nS
Chip Selection to End of Write	T_{CW}	50	-	70	-	nS
Address Valid to End of Write	T_{AW}	50	-	70	-	nS
Address Setup Time	T_{AS}	0	-	0	-	nS
Write Pulse Width	T_{WP}	50	-	70	-	nS
Write Recovery Time ($\overline{CS1}$, CS2, $\overline{WE}$)	T_{WR}	0	-	0	-	nS
Data Valid to End of Write	T_{DW}	30	-	50	-	nS
Data Hold from End of Write	T_{DH}	0	-	0	-	nS
Write to Output in High Z	T_{WHZ}*	-	25	-	30	nS
Output Disable to Output in High Z	T_{OHZ}*	-	25	-	30	nS
Output Active from End of Write	T_{OW}	5	-	10	-	nS

* These parameters are sampled but not 100% tested

TIMING WAVEFORMS

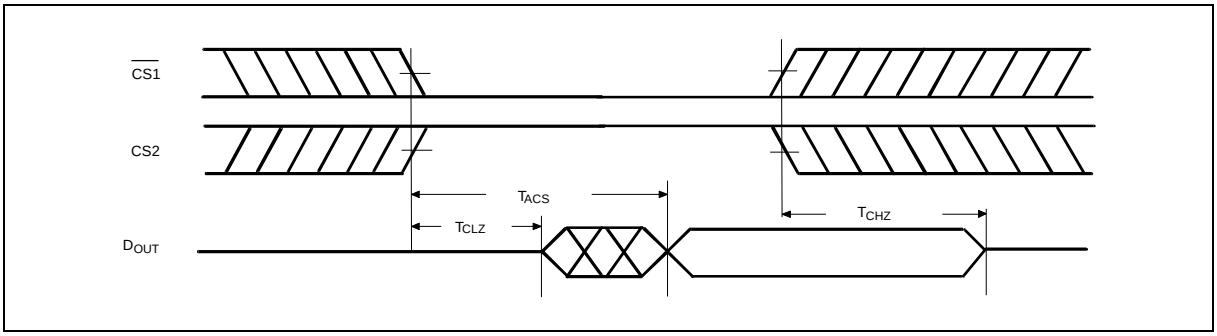
Read Cycle 1

(Address Controlled)



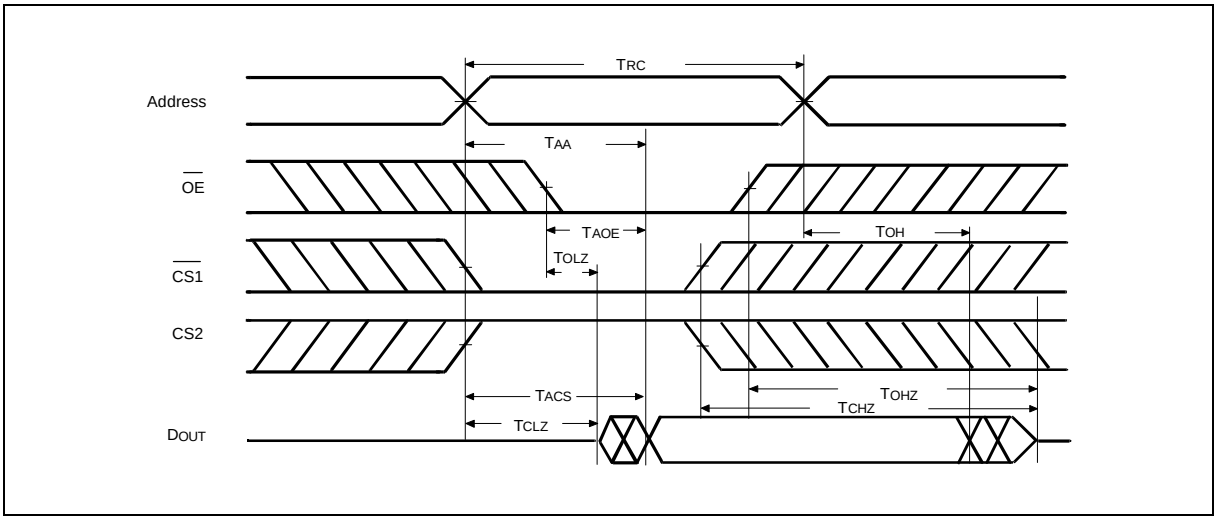
Read Cycle 2

(Chip Select Controlled)



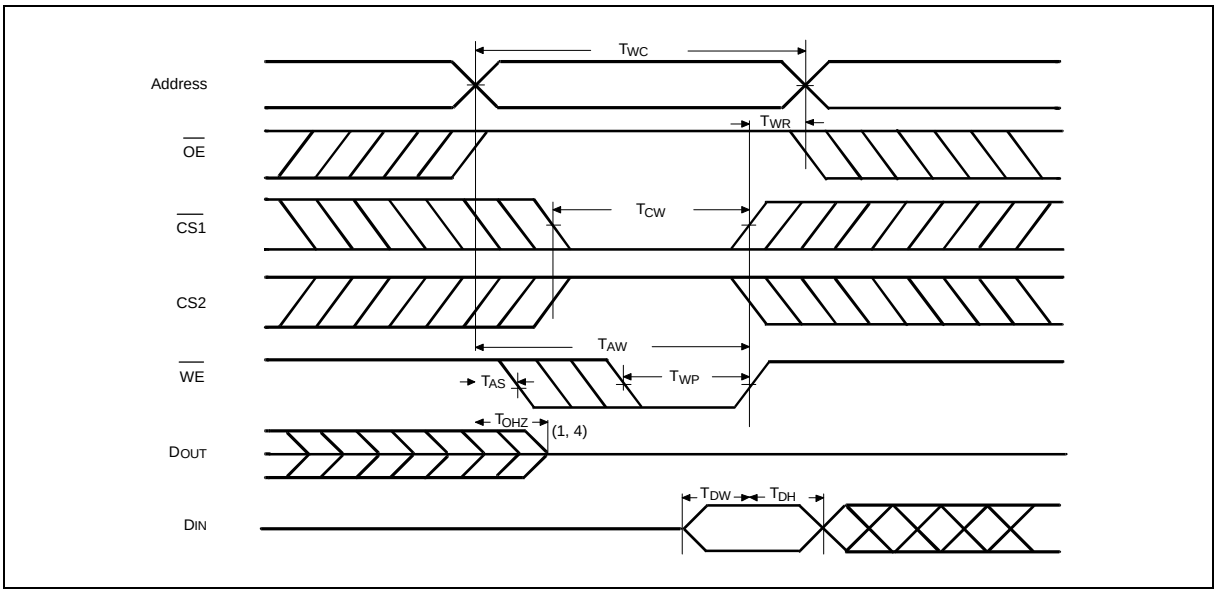
Read Cycle 3

(Output Enable Controlled)



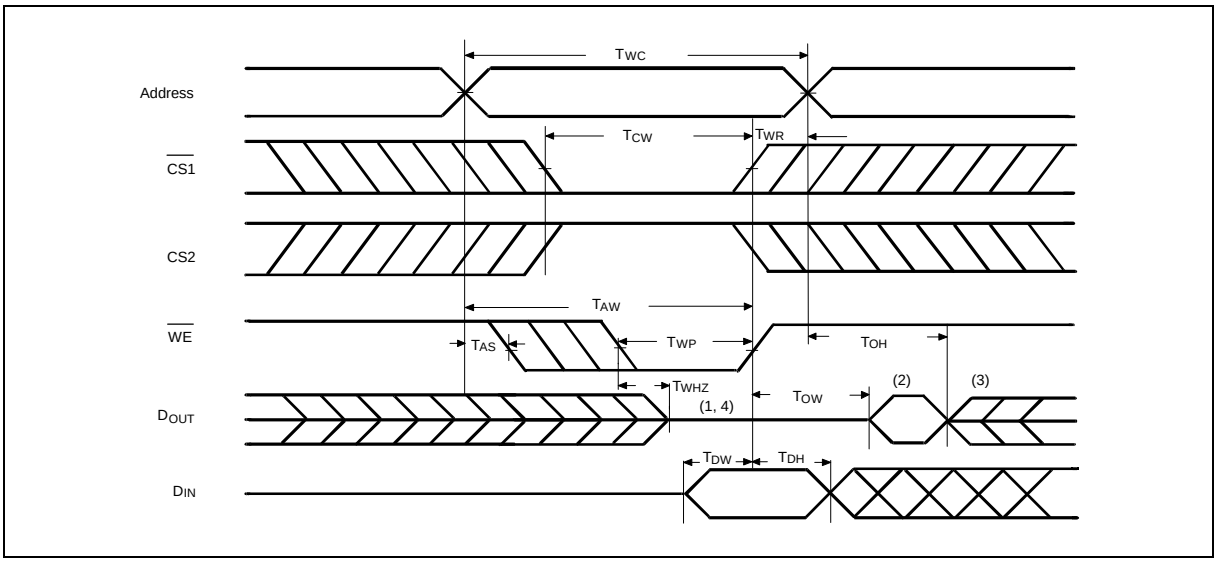
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

($\overline{OE}$ = VIL Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ±500 mV from steady state with CL = 5 pF. This parameter is guaranteed but not 100% tested.

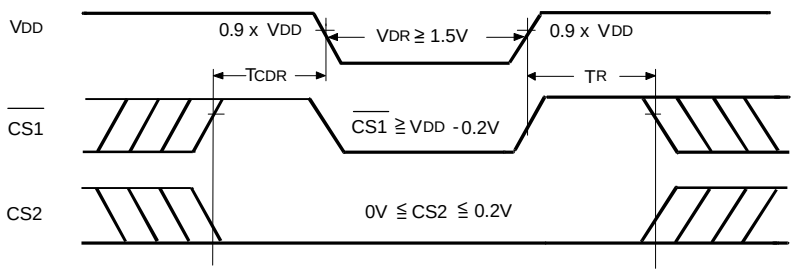
DATA RETENTION CHARACTERISTICS

(T_A (°C) =-20 to 85 for LE; -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{DD}$ -0.2V or CS2 ≤ 0.2V	2.0	-	-	V
Data Retention Current	I_{DDDR}	$\overline{CS1} \geq V_{DD}$ -0.2V or CS2 ≤ 0.2V, V_{DD} = 3V	-	-	5	µA
Chip Deselect to Data Retention Time	T_{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	T_R		T_{RC}*	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



ORDERING INFORMATION

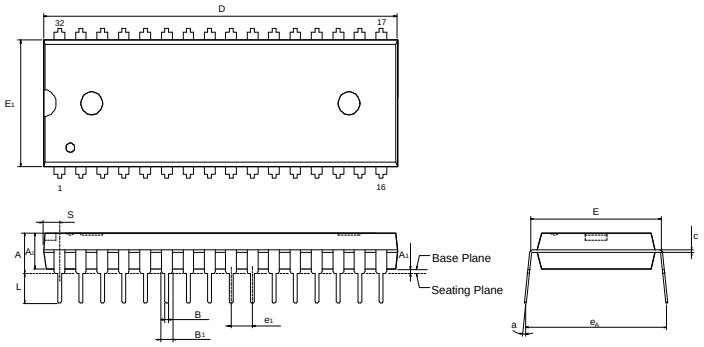
PART NO.	ACCESS TIME (nS)	OPERATING VOLTAGE (V)	OPERATING TEMPERATURE (°C)	PACKAGE
W24010-70LE	70/100	5V/3V	-20 to 85	600 mil DIP
W24010S-70LE	70/100	5V/3V	-20 to 85	450 mil SOP
W24010T-70LE	70/100	5V/3V	-20 to 85	Standard type one TSOP
W24010Q-70LE	70/100	5V/3V	-20 to 85	Small type one TSOP
W24010-70LI	70/100	5V/3V	-40 to 85	600 mil DIP
W24010S-70LI	70/100	5V/3V	-40 to 85	450 mil SOP
W24010T-70LI	70/100	5V/3V	-40 to 85	Standard type one TSOP
W24010Q-70LI	70/100	5V/3V	-40 to 85	Small type one TSOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

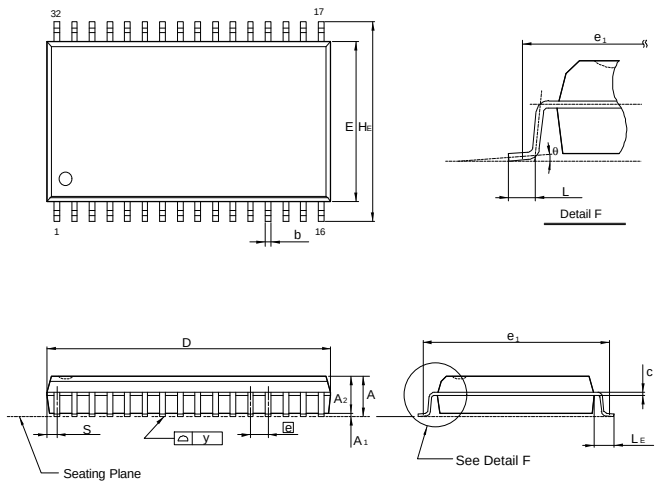
32-pin P-DIP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.650	1.660	—	41.91	42.16
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.545	0.550	0.555	13.84	13.97	14.10
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.085	—	—	2.16

Notes:
1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches
6. General appearance spec. should be based on final visual inspection spec.

32-pin SOP Wide Body

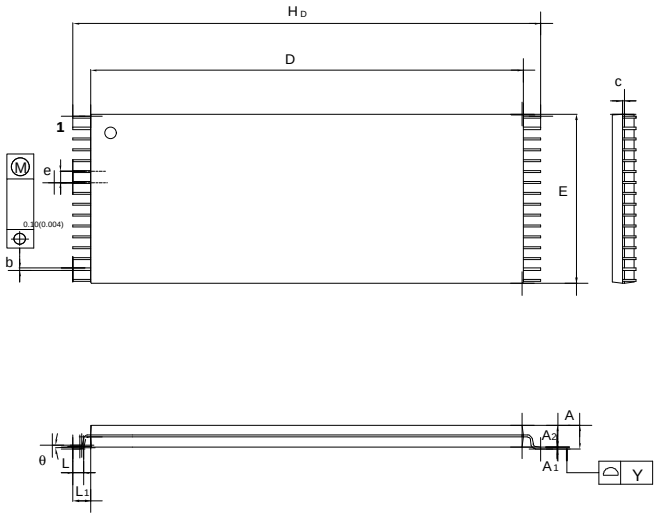


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.118	—	—	3.00
A_1	0.004	—	—	0.10	—	—
A_2	0.101	0.106	0.111	2.57	2.69	2.82
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.006	0.008	0.012	0.15	0.20	0.31
D	—	0.805	0.817	—	20.45	20.75
E	0.440	0.445	0.450	11.18	11.30	11.43
e	0.044	0.050	0.056	1.12	1.27	1.42
H_E	0.546	0.556	0.556	13.87	14.12	14.38
L	0.023	0.031	0.039	0.58	0.79	0.99
L_E	0.047	0.055	0.063	1.19	1.40	1.60
S	—	—	0.036	—	—	0.91
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:
1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimensions D & E include mold mismatch and determined at the mold parting line.
4. Controlling dimension: Inches
5. General appearance spec should be based on final visual inspection spec.

Package Dimensions, continued

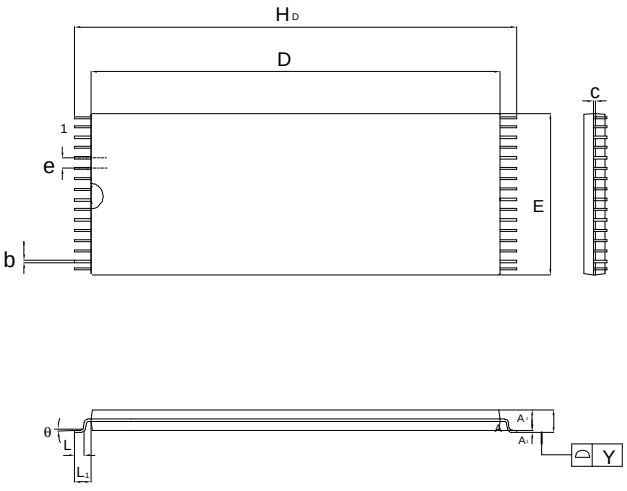
32-pin Standard Type One TSOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.005	0.006	0.007	0.12	0.15	0.17
D	0.720	0.724	0.728	18.30	18.40	18.50
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.780	0.787	0.795	19.80	20.00	20.20
e	—	0.020	—	—	0.50	—
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	—	0.031	—	—	0.80	—
Y	0.000	—	0.004	0.00	—	0.10
θ	1	3	5	1	3	5

Controlling dimension: Millimeters

32-pin Small Type One TSOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.049	—	—	1.25
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.27
c	0.0056	0.0059	0.0062	0.14	0.15	0.16
D	0.461	0.465	0.469	11.70	11.80	11.90
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.520	0.528	0.536	13.20	13.40	13.60
e	—	0.020	—	—	0.50	—
L	0.012	0.020	0.028	0.30	0.50	0.70
L_1	0.027	—	—	0.675	—	—
Y	0.000	—	0.004	0.00	—	0.10
θ	0	3	5	0	3	5

Controlling dimension: Millimeters

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Jun. 1996	-	Initial Issued
A2	Dec. 1996	-	NA
A3	Feb. 1998	1, 2, 4, 7, 8	Delete operating temperature (SL = 0 to 70 °C)
A4	Apr. 1998	3	Add standby power supply current (I_{SB1}) typical parameter when operation temperature TA = 25° C
A5	Jun. 1998	2, 3	Correct Operating Characteristics: add $\overline{CS1}$, CS2 test conditions
		7	Correct data retention characteristics: add $\overline{CS1}$, CS2 test conditions
A6	Nov. 1998	1, 8, 10, 11	Deduct reverse type one TSOP package

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