Winbond Electronics Corp.

SERIAL VOICE SRAM (128K · 1 BIT)

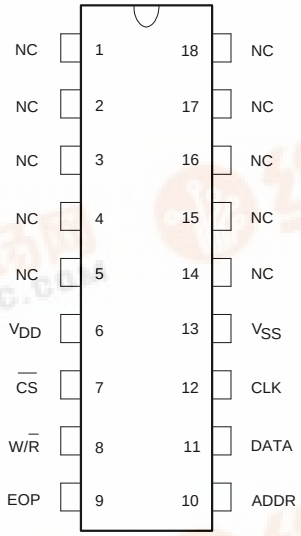
GENERAL DESCRIPTION

The W55206B is a normal speed, low power CMOS static RAM organized as 128K × 1 bit that operates on a single 5V power supply. Manufactured using Winbond's high performance CMOS technology, the W55206B is designed for extensive use in voice recording applications.

FEATURES

- Single 3.6V to 5.5V power supply
- Low power consumption
- Fully static operation
- Low data retention voltage
- Easy to cascade

PIN CONFIGURATION



PIN DESCRIPTION

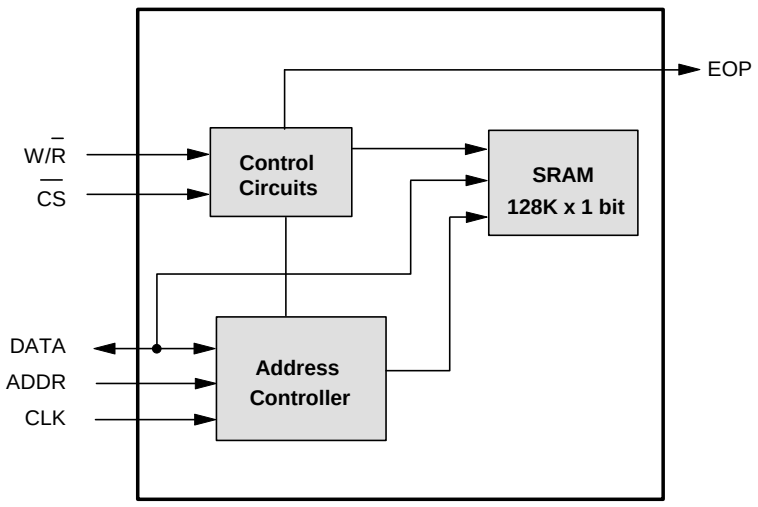
NO.	PIN	I/O	DESCRIPTION
6	V_{DD}	PWR	Positive power supply
7	$\overline{CS}$	I	Chip-inhibit for $\overline{CS}$ = 1; chip-select for $\overline{CS}$ = 0 or open (with internal pull-low resistor)

Publication Release Date: September 1996
Revision A1

Pin Description, continued

NO.	PIN	I/O	DESCRIPTION
8	W/$\overline{R}$	I	Write-in control for W/$\overline{R}$ = 1, read-out control for W/$\overline{R}$ = 0
9	EOP	O	End signal output
10	ADDR	I	Clock input for start address
11	DATA	I/O	Bidirectional data pin
12	CLK	I	Clock input for address increment
13	V_{SS}	PWR	Ground

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

- TRUTH TABLE

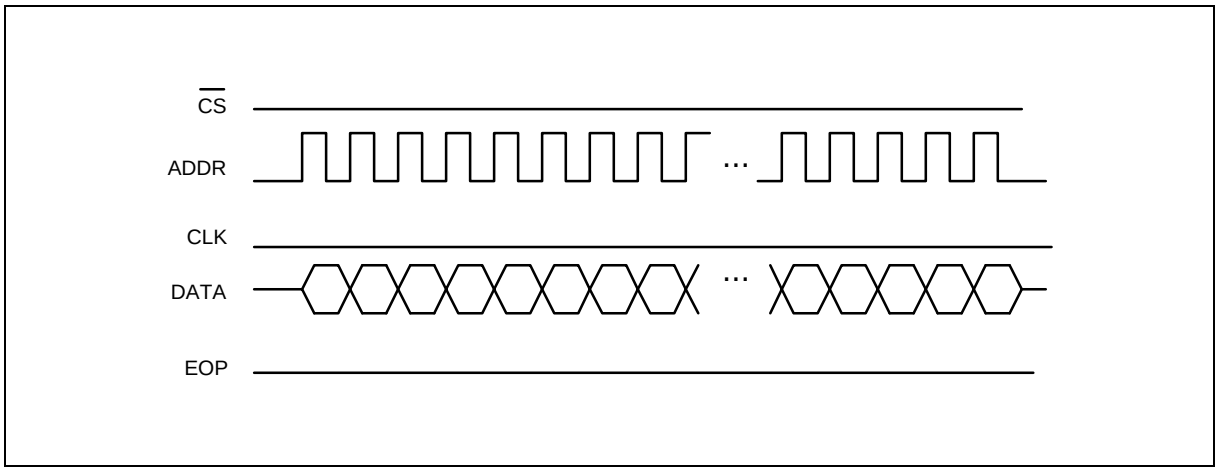
$\overline{CS}$	W/$\overline{R}$	MODE	DATA PIN	V_{DD} CURRENT
H	X	Not selected	High Z	I_{SB}
L	H	Write	Data in	I_{OP}
L	L	Read	Data out	I_{OP}

- When the chip is unselected, the W/$\overline{R}$ signal will be transmitted to the EOP pin.
- Before a read or write operation, the address counter must be reset by sending an ADDR pulse and setting DATA = 0.

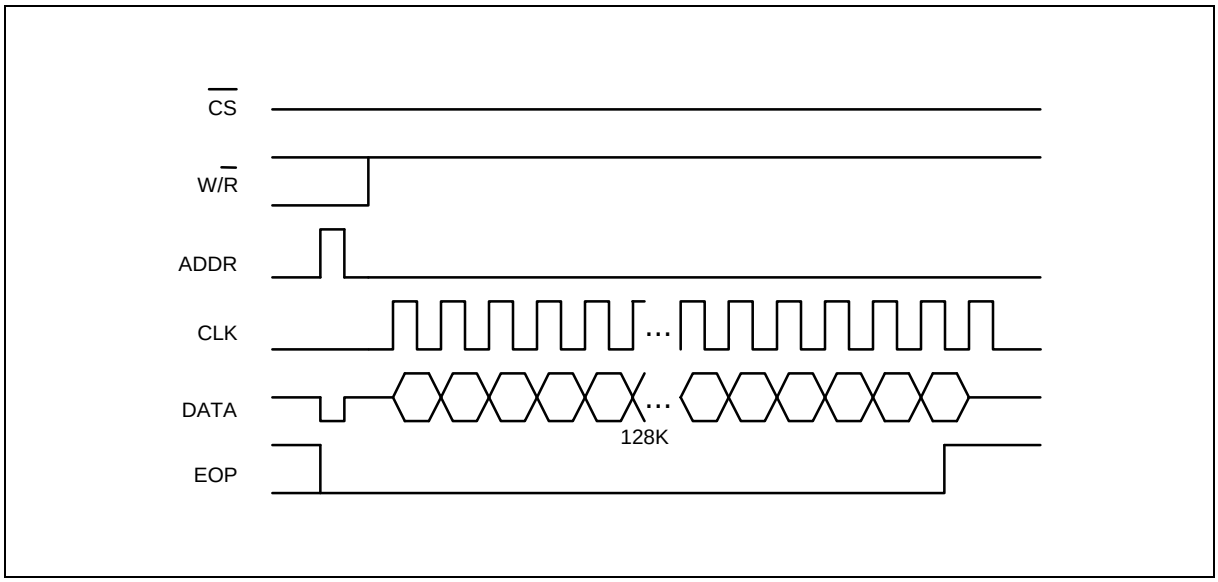
- After power on, the read operation is disabled. A read operation may be performed only after a write operation is completed.
- In write-in operation, the EOP signal will change from low to high and remain high when the final address of the chip is encountered. It will change to low again with the next ADDR pulse.
- In read-out operation, the EOP pin will generate one pulse signal when the final address of the SRAM chip is encountered.

The timing of the loading start address for write-in/read-out operations is shown below:

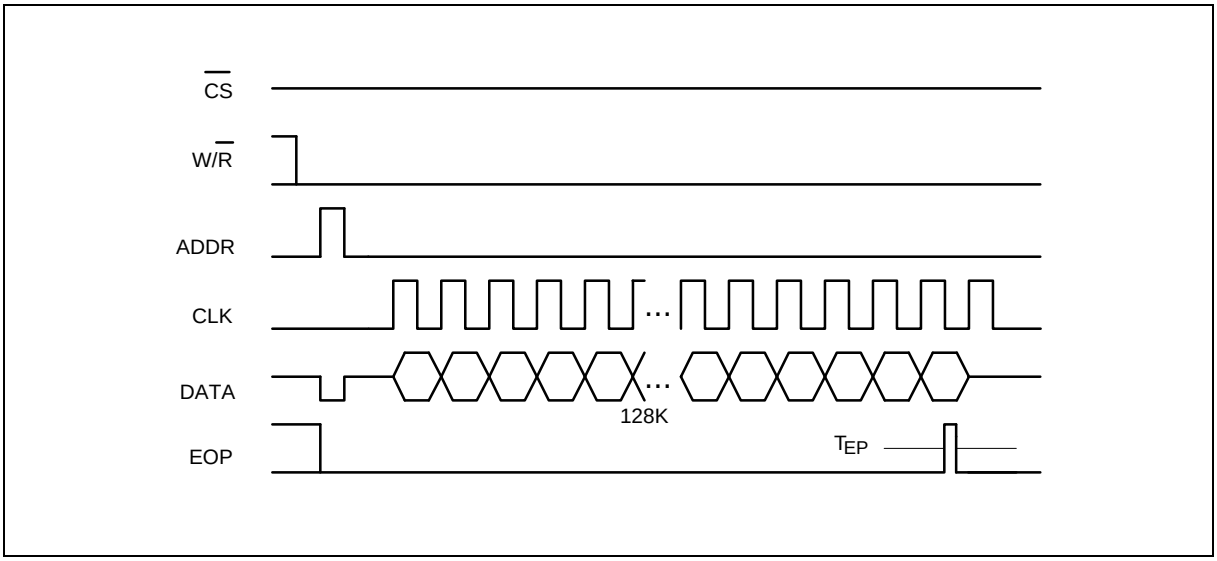
- Load start address for write-in/read-out operations:



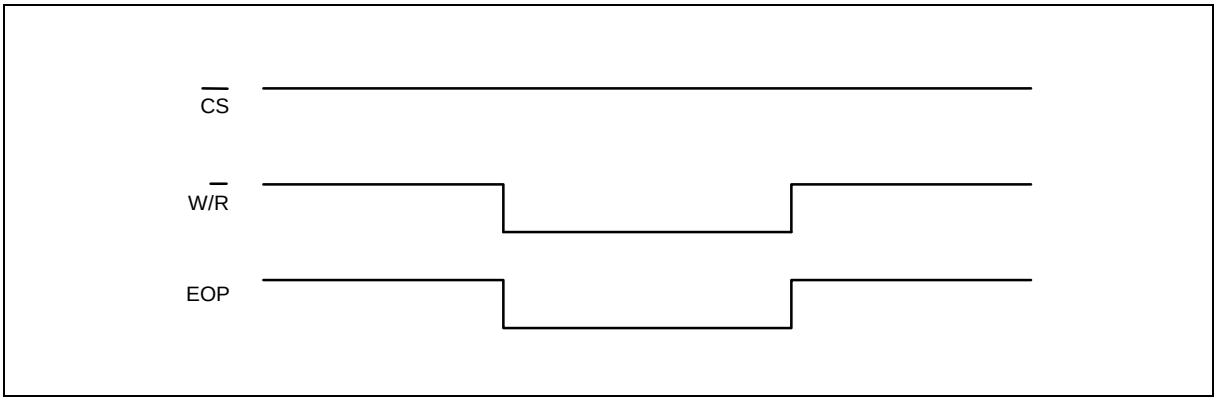
- Write-in operation:



- Read-out operation:



- No operation (standby)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}–V_{SS}	-0.3 to +5.5	V
Input Voltage	V_{IN}	V_{SS} -0.2 to V_{DD} +0.2	V
Output Voltage	V_O	V_{SS} to V_{DD}	V
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

T_A = 25° C, V_{DD} = 5.0V, V_{SS} = 0.0V

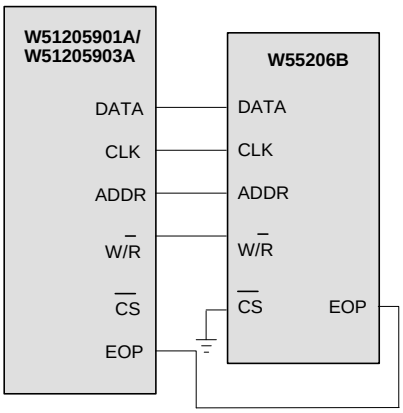
PARAMETER	SYMBOL	CONDITIONS	LIMIT			UNIT
			MIN.	TYP.	MAX.	
Operating Voltage	V_{DD}	-	3.6	5.0	5.5	V
Operating Current	I_{OP}	Fc = 1 MHz	-	-	15	mA
V_{DD} for Data Retention	V_{DR}	$\overline{CS} \geq V_{DD}$ -0.2V	2.4	-	5.5	V
Data Retention Current	I_{DDDR}	$V_{DD} \geq$ 3V, $\overline{CS} \geq$ 2.8V	-	-	10	µA
Standby Current	I_{SB}	-	-	2	10	µA
Input Voltage (for ADDR, CLK, W/$\overline{R}$ and $\overline{CS}$ pins)	V_{IH}	-	2.8	-	6.0	V
	V_{IL}	-	-0.5	-	+0.8	
Input Current (for $\overline{CS}$)	I_{IH}	V_I = 5.0V	-	-	5	µA
Output Current (for EOP)	I_{OH}	V_O = 4.0V	4	6	-	mA
	I_{OL}	V_O = 0.8V	-4	-8	-	

AC CHARACTERISTICS

Ta = 25° C, V_{DD} = 5.0V, V_{SS} = 0.0V

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP	MAX.	UNIT
Clock Frequency (for CLK and ADDR)	Fc	-	-	-	1	MHz
Data Hold Time	T_{WH}	Write mode	0	-	-	nS
Data Hold Time	T_{RH}	Read mode	0	-	-	nS
Data Hold Time (for ADDR)	T_{AH}	-	0	-	-	nS
Data Access Time	T_{RA}	Read mode	-	-	80	nS
Data Setup Time	T_{WS}	Write mode	250	-	-	nS
Data Setup Time (for ADDR)	T_{AS}	-	250	-	-	nS
EOP Pulse Width (for ADDR)	T_{EP}	Read mode	100	-	-	nS
High Level Duration of Clock for CLK and ADDR	T_H	-	400	-	-	nS
Low Level Duration of Clock for CLK and ADDR	T_L	-	600	-	-	nS
W/$\overline{R}$ Signal Setup Time for Write Mode	T_{SUR}	-	300	-	-	nS
W/$\overline{R}$ Signal Setup Time for Write Mode	T_{SUW}	-	300	-	-	nS
Time Width Between ADDR and CLK Clock	T_D	-	1	-	-	µS

TYPICAL APPLICATION CIRCUIT (For reference only)



* W51205901A/W51205903A substrate connected to V_{SS} for C.O.B.

* W55206B substrate connected to V_{DD} for C.O.B.

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