Winbond USB Scanner Processor

W6668F

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W6668F Data Sheet Revision History

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WINBOND USB SCANNER PROCESSOR

1. GENERAL DESCRIPTION

The W6668 is a highly integrated USB scanner control processor. It provides the system required signals for all necessary of a CCD/CIS scanner, the signal interface includes CCD/CIS sensor, image buffer memory, motor drive, lamp/LED drive and other mechanical input/output signals. The processor accept and process the analog image data, convert to digital data and store the data to the image buffer and then transfer to the host through USB bus. The scanner commands and status are transfer from or to the PC through USB bus without the aid of micro controller. The command and status also can be transfered through serial port and accessed by 8051 without the aids of USB port and windows operation system.

The only required additional active components are SRAM or DRAM for scanning image buffer, power regulator for 5V and 3.3V power source (if 3.3V component is in use) and power transistor array for the step motor.

2. FEATURES AND APPLICATIONS

Features:

Complete scanner on one chip solution for sheetfeed and flatbed scanners.

Internal timing generator for 300, 600 or 1200 dpi CCD/CIS sensor.

Builtin control signals for CCD lamp, CCD electric shutter, or CIS LED driver.

Multiple CCD transfer gate driver supported to extend CCD exposure time.

Exposure time of multiple CCD transfer gate driver can be programmed individually.

Horizontal and vertical of 1200, 800, 600, 400, 300, 200, 150, 100, 75 or 50 dpi selectable.

Three channels analog input with clamp circuit individually.

Integrated Correlated Double Sampler (CDS).

Integrated 6-bit Programmable Gain Amplifier (PGA) range from 1 to 6.

Integrated 8 + sign bits offset adjustment.

16-bit A/D Converter.

14-bit no missing Code Guaranteed.

24 MHz system clock and 1 MHz or 1.5 MHz or 2 MHz of pixel rate selectable by software reseting.

16-bit/8-bit image data capture.

R channel or G channel or B channel can be used in monochrome mode.

CIS LED light on overlap feature supported to get pure black and white monochrome scan.

Supports black and white of line art data format.

Direct access many types of SRAM/DRAM as image buffer.

32K, 64K, 128K, 256K or 512K with 8-bit data size of SRAM can be used.

64K, 256K, 1M or 4M with 8-bit or 16-bit data size of DRAM can be used.

Builtin shading and gamma correction process.

Shading and gamma process or gamma process only can be disabled.

8-bit or 16-bit of shading coefficient can be used.

8-bit or 14-bit of gamma coefficient can be used.

Full step, half step or micro step of step motor can be use.

Motor coil current can be fine tuned.

Support external bipolar PWM motor driver interface.

Motor speed can be selected from 2 times to 1/16 of exposure time each step.

0 to 255 back tracking step can be programmed.

Motor speed up and slow down with full, ½, ¼, 1/8 scan speed during scanning and back tracking.

Auto parking procedure supported.

Motor speed of scanning or auto-parking can be programmed individually.

CCD lamp PWM driver supported when external bipolar PWM motor driver is used.

LED indicator with on/off or 1/2 Hz, 1 Hz flash mode provided.

7-bit of general I/O port with latched and un-latched input port can be read.

Internal PLL provided to generate 48 MHz for USB SIE use.

Builtin USB transceiver, SIE and SIL processor.

Serial ROM interface for vendor ID and product ID code configuration.

USB Specification Version 1.1 Compliant.

High speed USB device with 12M bps data transmission rate.

Support suspend/resume mode, automatically/Host suspend and Host wake up (resume).

External wake up supported to wake up Host.

Support 1 device configuration and 1 device interface.

Support 4 endpoints includes:

Endpoint 0: Control transfer, 8 bytes packet size of bi-direction data transfer for device setup and configuration.

Endpoint 1: Bulk out transfer, 4 bytes or 8 bytes packet size of unidirection data transfer for scanner control command or scanner table download from Host to scanner.

Endpoint 2: Bulk in transfer, 64 bytes packet size double buffer of unidirection data transfer for scanner image data to Host. One or two bytes of unidirection data transfer for register data read or table read back to Host.

Endpoint 3: Interrupt transfer, 1 bytes packet size of unidirection data transfer for interrupt information to Host.

Bulid in USB 1.1 standard command decoder.

1.1 Mega byte transfer rate during image scan in.

Software USB driver for Win98 supported.

Support serial port access bypass USB interface.

Power saving mode supported.

CMOS compatible.

5 V analog and digital power required.

Builtin 5V to 3.3V regulator for the power source of internal logic and USB interface circuit.

100-pin PQFP package (W6668F).

Applications:

Flatbed Scanners.

Sheetfeed Scanners.

Film Scanners.

3. PIN CONFIGURATION

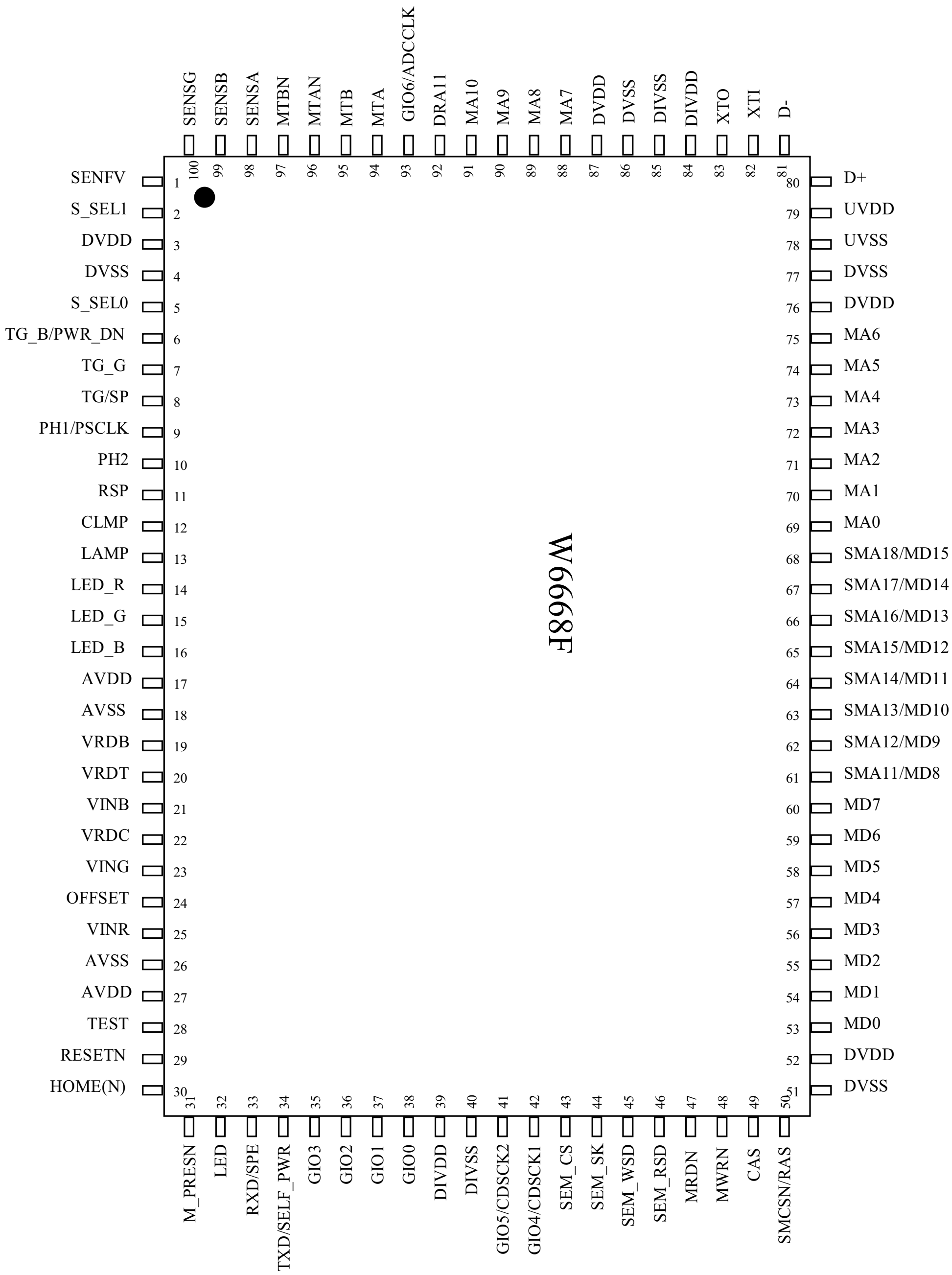


Fig.3-1 W6668F Pin Assignment.

4. PIN DESCRIPTIONS

Pin	Name	Type (mA)	Description
CCD/CIS Interface:			
8	TG(_R)/SP	DO(4)	CCD Transfer Gate (R channel) or CIS Start Pulse.
7	TG_G	DO(4)	CCD Transfer Gate of G channel channel if three channel TG signal is enabled.
6	TG_B/ PWR_DN	DO(4) DI	CCD Transfer Gate of B channel channel if three channel TG signal is enabled. Power down or USB Suspend output, polarity setting during hardware reset, active low if set low at the end of hardware reset.
9	PH1/PSCLK	DO(4)	CCD Phase 1 clock or CIS pixel shift clock.
10	PH2	DO(4)	CCD Phase 2 clock.
11	RSP	DO(6)	CCD or CIS Reset Pulse.
12	CLMP	DO(4)	CCD Clamp or CIS Clamp.
14	LED_R	DO(2)	CIS red channel LED driver or CCD red channel electric shutter.
15	LED_G	DO(2)	CIS green channel LED driver or CCD green channel electric shutter.
16	LED_B	DO(2)	CIS blue channel LED driver or CCD blue channel electric shutter.
5	S_SEL0 *SMTA*	DO(2)	CCD/CIS sensor channel Select 0. *Slave motor driver signal, positive A phase.*
2	S_SEL1 *SMTB*	DO(2)	CCD/CIS sensor channel Select 1. *Slave motor driver signal, positive B phase.*
Analog Signals Input:			
25	VINR	AI	Analog Input, R channel.
23	VING	AI	Analog Input, G channel.
21	VINB	AI	Analog Input, B channel.
Analog Reference:			
20	VRDT	AO	ADC Reference Voltage (Top), top level of the ADC reference range.
19	VRDB	AO	ADC Reference Voltage (Bottom), bottom level of the ADC reference range.
22	VRDC	AO	ADC Reference Voltage (Internal), internal bias level of the ADC reference voltage.
24	OFFSET	AO/AI	Clamp Offset Voltage Output or offset voltage input in CIS mode.

4. Pin Description, continued

Pin	Name	Type (mA)	Description
Analog Power:			
17,27	AVDD	AP	Analog Power (2 pins).
18,26	AVSS	AP	Analog Ground (2 pins).
Image Buffer Interface:			
75-69	MA[6:0]	DO(2)	Address line [8:0] of SRAM or address line [8:0] of DRAM.
91-88	MA[10:7]	DO(2)	Address line [10:9] of SRAM or address line [10:9] of DRAM.
92	DRA11/ *SMTAN*	DO(2)	Row address line 11 of DRAM. *Slave motor driver signal, negative A phase.*
68-61	SMA[18:11]/ MD[15:8]	DO/ DIO(2)	Address line [18:11] of SRAM, high byte data bus of DRAM or data bus of DRAM if 8-bit data is configured.
60-53	MD[7:0]	DIO(2)	Data bus of SRAM or low byte data bus of DRAM .
50	SMCSN/ RAS	DO(2)	Chip Select of SRAM or Raw address strobe of DRAM.
49	CAS	DO(2)	Column Address Strobe of DRAM.
47	MRDN	DO(2)	Memory Read control signal, active low.
48	MWRN	DO(2)	Memory Write control signal, also can be used as RD/WR signal of DRAM or SRAM, active low.
Motor Control Driver Signal:			
94	MTA	DO(2)	Motor driver signal, positive A phase.
95	MTB	DO(2)	Motor driver signal, positive B phase.
96	MTAN	DO(2)	Motor driver signal, negative A phase.
97	MTBN	DO(2)	Motor driver signal, negative B phase.
98	SENSA	AI	Motor phase A current sense input signal.
99	SENSB	AI	Motor phase B current sense input signal.
100	SENSG	AI	GND (reference) signal of motor phase current sense input.
1	SENFV	AI/AO	Full voltage of motor sense signal.

4. Pin Description, continued

Pin	Name	Type (mA)	Description
Serial ROM Interface:			
43	SEM_CS/ *DFT_PDS3*	DO(2) *DI*	Serial EEPROM Chip Select. *Default vendorID and product ID select bit 3.*
44	SEM_SK/ DFT_PDS2	DO(2) *DI*	Serial EEPROM Serial Clock. *Default vendorID and product ID select bit 2.*
45	SEM_WSD/ DFT_PDS1	DO(2) *DI*	Serial EEPROM command Write Serial Data. *Default vendorID and product ID select bit 1.*
46	SEM_RSD/ DFT_PDS0	DI	Serial EEPROM Read Serial Data. *Default vendorID and product ID select bit 0.*
USB Interface:			
80	D+	AIO	USB D plus signal.
81	D-	AIO	USB D minus signal.
Crystal Driver:			
82	XTI	DI	Clock driver input signal, may be used as external clock input.
83	XTO	DO	Clock driver output signal.
I/O Signals:			
30	HOME(N)	DI	Optical module home sensor, may be active high or active low.
32	LED	DO(2)	LED indicator.
13	LAMP	DO(2)	CCD Lamp driver, active high.
31	M_PRESN	DI	Manual Push button input, active low, also used as remote wake up input.
35-38	GIO[3:0]	DI/DO (2)	General Input Output port [3:0].
42	GIO4/ CDSCK1	DI/DO (2)	General Input Output port 4 or AFE circuit CDSCK1 clock signal.
41	GIO5/ CDSCK2	DI/DO (2)	General Input Output port 5 or AFE circuit CDSCK2 clock signal.
93	GIO6/ ADCCLK/ *SMTBN*	DI/DO (2)	General Input Output port 6 or AFE circuit ADCCLK clock signal. *Slave motor driver signal, negative B phase.*

4. Pin Description, continued

Pin	Name	Type (mA)	Description
Serial Port Signal:			
33	RXD/SPE	DI/DO	Receive Data pin or Serial Port Enable (high setting during reset), must left open when USB port is enabled.
34	TXD/ SELF_PWR	DO/DI (2)	Transmit Data pin when serial port is enabled or device SELF Power configured if it is high when serial port is disabled.
Other Signal:			
29	RESETN	DI	Reset input, hardware reset input, active low.
28	TEST	DI	Test Input, must left open in normal operation.
Power:			
3,52, 76,87	DVDD	DP	Digital Power 5.0V (4 pins).
4,51, 77,86	DVSS	DP	Digital Ground (4 pins).
39,84	DIVDD	DP	Digital Internal Power 3.3V (2 pins).
40,85	DIVSS	DP	Digital Internal Ground (2 pins).
79	UVDD	AP	USB transceiver Power 3.3V.
78	UVSS	AP	USB transceiver Ground.

Type: AP is Analog Power, AI is Analog Input, AO is Analog Output, DP is Digital Power, DI is Digital Input, DO is Digital Output.

5. BLOCK DIAGRAM & REGISTERS LIST

5.1 Block Diagram

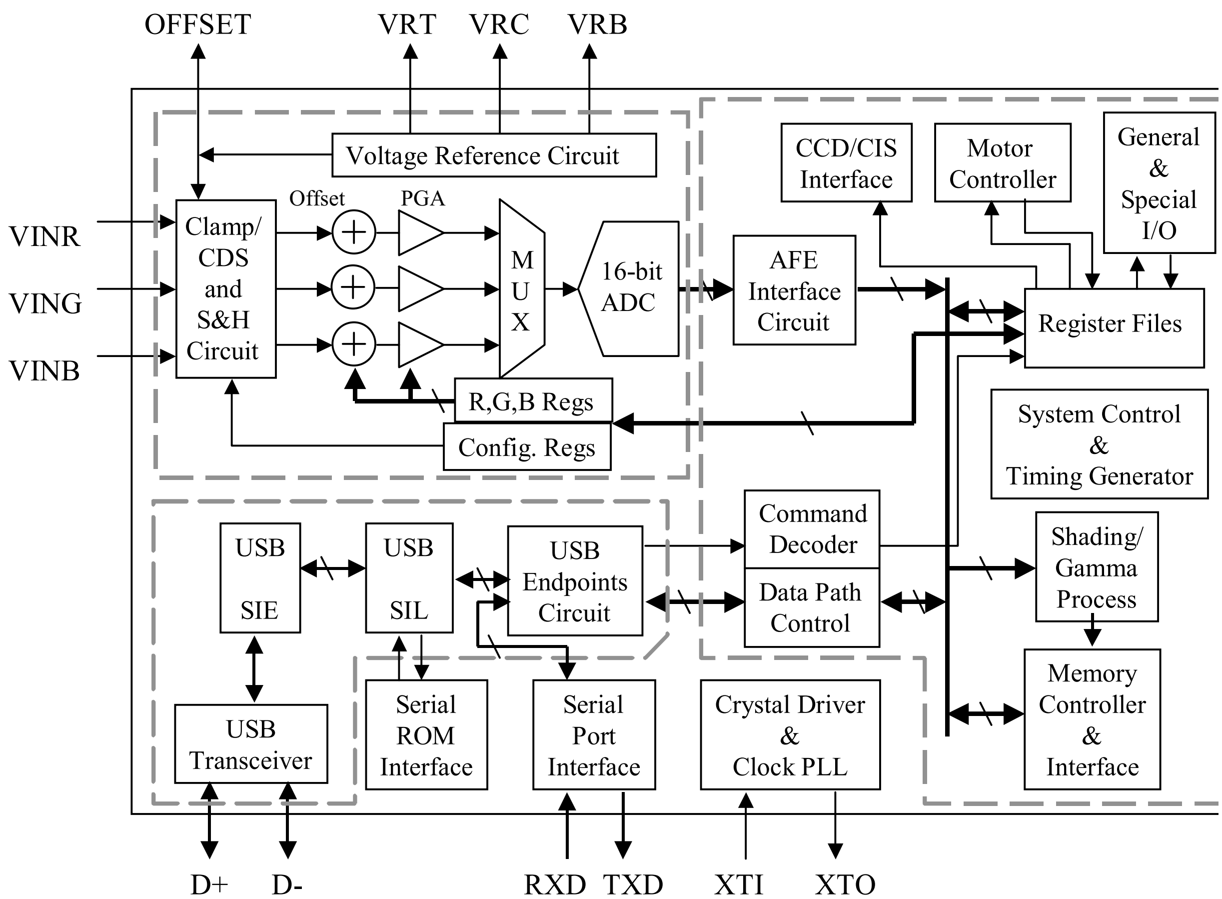
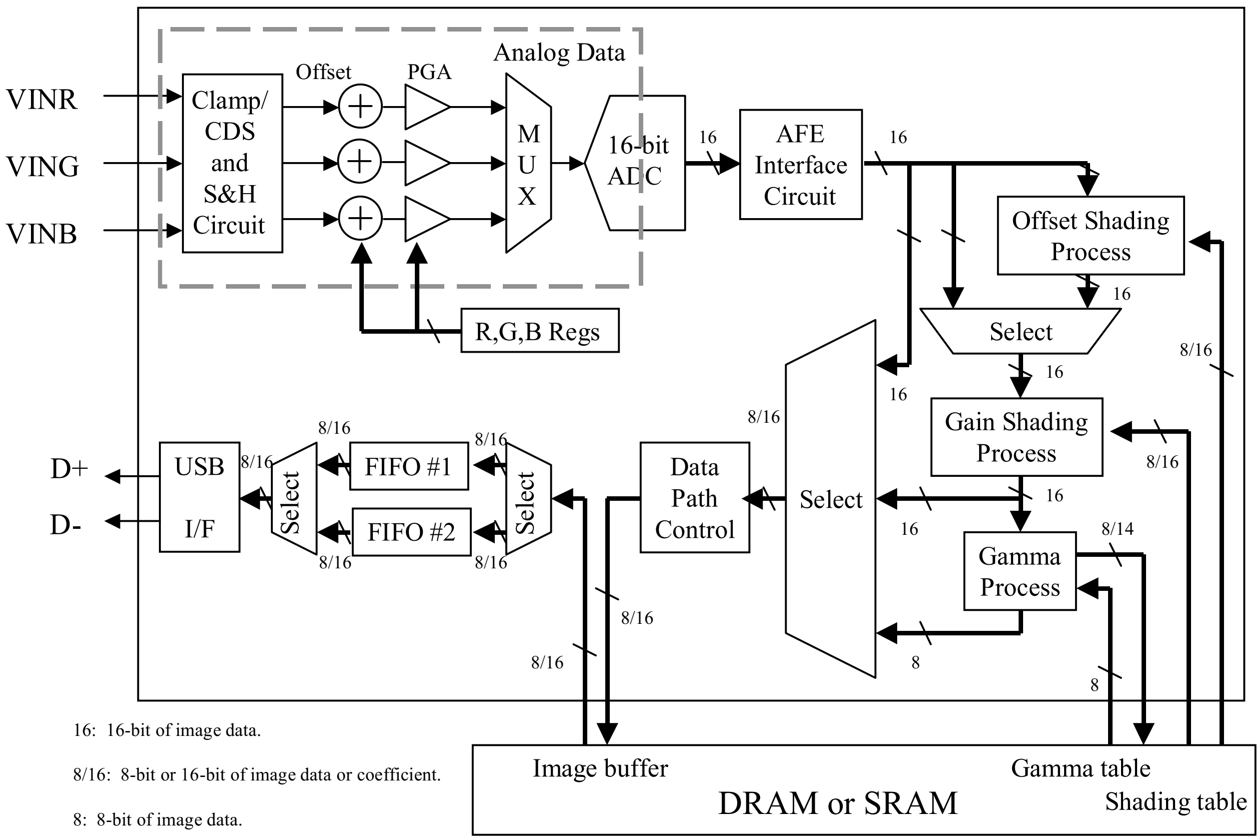


Fig. 5-1 Block Diagram of W6668 Device.

Note: Digital I/O pins are omitted on this figure.

There are three major parts consisted in W6668 device: the first part is analog front end circuit, at the left-top of the block diagram and is described in section 6; the second part is scanner ASIC circuit, at the right side of the block diagram and is described in section 7; the third part is USB interface circuit, at the left-bottom and is described in section 8. USB standard device requests is described in section 9. Figure 5-2 shows the image data processing flow from three channels analog input to USB bulk in to Host.



16: 16-bit of image data.

8/16: 8-bit or 16-bit of image data or coefficient.

8: 8-bit of image data.

Fig. 5-2 Image Data Process Flow of W6668 Device.

5.2 Register List Tables

Part 1: Analog Front End

Addr (dec)	Name	Default (hex)	Content							
			bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00H (0)	Config Reg.	F8	IP_ Span	Vref	3-ch	CDS	ICLB	AFE_ PD	0	0
01H (1)	AFE MUX Reg.	C0	1	Mon_R	Mon_G	Mon_B	0	0	0	0
02H (2)	PGA code (R-ch)	00	0	0	PGA_ R5	PGA_ R4	PGA_ R3	PGA_ R2	PGA_ R1	PGA_ R0
03H (3)	PGA code (G-ch)	00	0	0	PGA_ G5	PGA_ G4	PGA_ G3	PGA_ G2	PGA_ G1	PGA_ G0
4H (4)	PGA code (B-ch)	00	0	0	PGA_ B5	PGA_ B4	PGA_ B3	PGA_ B2	PGA_ B1	PGA_ B0
05H (5)	DAC code (R-ch)	00	DAC_ R7	DAC_ R6	DAC_ R5	DAC_ R4	DAC_ R3	DAC_ R2	DAC_ R1	DAC_ R0
06H (6)	DAC code (G-ch)	00	DAC_ G7	DAC_ G6	DAC_ G5	DAC_ G4	DAC_ G3	DAC_ G2	DAC_ G1	DAC_ G0
07H (7)	DAC code (B-ch)	00	DAC_ B7	DAC_ B6	DAC_ B5	DAC_ B4	DAC_ B3	DAC_ B2	DAC_ B1	DAC_ B0
08H (8)	DAC SIGN (R-ch)	00	0	0	0	0	0	0	0	DSIGN _R
09H (9)	DAC SIGN (G-ch)	00	0	0	0	0	0	0	0	DSIGN _G
0AH (10)	DAC SIGN (B-ch)	00	0	0	0	0	0	0	0	DSIGN _B

Part 2: CCD/CIS and AFE Interface

Addr (dec)	Name	Default (hex)	Content							
			bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10H (16)	Sensor Signal Polarity	70	0	LEDB_P	LEDG_P	LEDR_P	CLMP_P	PH1_P	RS_P	TG_P
11H (17)	Phase Behav Register	00	0	Diff_Exp_MD	Three_TG	NON_DUTY	ODD/EVEN_CCD	*PH_QBL*	*PH_DBL*	PH_EN_TG
12H (18)	Sensor Channel Select	39	0	0	S_Bsel 1	S_Bsel 0	S_Gsel 1	S_Gsel 0	S_Rsel 1	S_Rsel 0
13H (19)	TG shift (note 1)	00	0	0	0	TG_S4	TG_S3	TG_S2	TG_S1	TG_S0
14H (20)	TG width (note 2)	00	0	0	0	0	TG_W3	TG_W2	TG_W1	TG_W0
15H (21)	RSP shift (note 1)	00	0	0	0	RSP_S4	RSP_S3	RSP_S2	RSP_S1	RSP_S0
16H (22)	RSP width (note 1)	00	0	0	0	RSP_W4	RSP_W3	RSP_W2	RSP_W1	RSP_W0
17H (23)	PH shift (note 1)	00	0	0	0	PH_S4	PH_S3	PH_S2	PH_S1	PH_S0
18H (24)	CLMP shift (note 1)	00	0	0	0	CLMP_S4	CLMP_S3	CLMP_S2	CLMP_S1	CLMP_S0
19H (25)	CLMP width (note 1)	00	0	0	0	CLMP_W4	CLMP_W3	CLMP_W2	CLMP_W1	CLMP_W0
1AH (26)	CDSCK1 shift (note 1)	00	0	0	0	CDCK1_S4	CDCK1_S3	CDCK1_S2	CDCK1_S1	CDCK1_S0
1BH (27)	CDSCK width (note 1)	00	0	CDCK2_W2	CDCK2_W1	CDCK2_W0	0	CDCK1_W2	CDCK1_W1	CDCK1_W0

Part 2: CCD/CIS and AFE Interface, continued

Addr (dec)	Name	Default (hex)	Content							
			bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1CH (28)	CDSCK2 shift (note 1)	00	0	0	0	CDCK 2_S4	CDCK 2_S3	CDCK 2_S2	CDCK 2_S1	CDCK 2 _S0
1DH (29)	Add_Fun_ Reg1	00	0	0	0	Mtr_no _Mv	2_Ph_ PWM	Algo_ Mtr_IF	Dumy_ TG	RSP_ Dis_T G
1EH (30)	Exposure time reg * (low byte)	BC	EXP _T7	EXP _T6	EXP _T5	EXP _T4	EXP _T3	EXP _T2	EXP _T1	EXP _T0
1FH (31)	Exposure time reg * (high byte)	05	EXP _T15	EXP _T14	EXP _T13	EXP _T12	EXP _T11	EXP _T10	EXP _T9	EXP _T8
20H (32)	Start of LED R channel * (low byte)	00	STRT _R7	STRT _R6	STRT _R5	STRT _R4	STRT _R3	STRT _R2	STRT _R1	STRT _R0
21H (33)	Start of LED R channel * (high byte)	00	STRT _R15	STRT _R14	STRT _R13	STRT _R12	STRT _R11	STRT _R10	STRT _R9	STRT _R8
22H (34)	End of LED R channel * (low byte)	00	END _R7	END _R6	END _R5	END _R4	END _R3	END _R2	END _R1	END _R0
23H (35)	End of LED R channel * (high byte)	00	END _R15	END _R14	END _R13	END _R12	END _R11	END _R10	END _R9	END _R8
24H (36)	Start of LED G channel * (low byte)	00	STRT _G7	STRT _G6	STRT _G5	STRT _G4	STRT _G3	STRT _G2	STRT _G1	STRT _G0

Part 2: CCD/CIS and AFE Interface, continued

Addr (dec)	Name	Default (hex)	Content							
			bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
25H (37)	Start of LED G channel * (high byte)	00	STRT _G15	STRT _G14	STRT _G13	STRT _G12	STRT _G11	STRT _G10	STRT _G9	STRT _G8
26H (38)	End of LED G channel * (low byte)	00	END _G7	END _G6	END _G5	END _G4	END _G3	END _G2	END _G1	END _G0
27H (39)	End of LED G channel * (high byte)	00	END _G15	END _G14	END _G13	END _G12	END _G11	END _G10	END _G9	END _G8
28H (40)	Start of LED B channel * (low byte)	00	STRT _B7	STRT _B6	STRT _B5	STRT _B4	STRT _B3	STRT _B2	STRT _B1	STRT _B0
29H (41)	Start of LED B channel * (high byte)	00	STRT _B15	STRT _B14	STRT _B13	STRT _B12	STRT _B11	STRT _B10	STRT _B9	STRT _B8
2AH (42)	End of LED B channel * (low byte)	00	END _B7	END _B6	END _B5	END _B4	END _B3	END _B2	END _B1	END _B0
2BH (43)	End of LED B channel * (high byte)	00	END _B15	END _B14	END _B13	END _B12	END _B11	END _B10	END _B9	END _B8

Part 3: Shading Gamma

Addr (dec)	Name	Default (hex)	Content bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
2CH (44)	Shad/gamma set Register	00	0	0	16-bit_SHAD	14-bit_Gamma	0	0	SH_GM_EN1	SH_GM_EN0
2DH (45)	Start Shd_Gm_Address Reg	00	0	0	SSDG_AD_21	SSDG_AD_20	SSDG_AD_19	SSDG_AD_18	SSDG_AD_17	0
2EH (46)	Start G-ch Offset Reg (low byte)	00	STO_G11	STO_G10	STO_G9	STO_G8	0	0	0	0
2FH (47)	Start G-ch Offset Reg (high byte)	00	0	0	0	STO_G16	STO_G15	STO_G14	STO_G13	STO_G12
30H (48)	Start B-ch Offset Reg (low byte)	00	STO_B11	STO_B10	STO_B9	STO_B8	0	0	0	0
31H (49)	Start B-ch Offset Reg (high byte)	00	0	0	0	STO_B16	STO_B15	STO_B14	STO_B13	STO_B12
32H (50)	Start R-ch Gain Reg (low byte)	00	STG_R11	STG_R10	STG_R9	STG_R8	0	0	0	0
33H (51)	Start R-ch Gain Reg (high byte)	00	0	0	0	STG_R16	STG_R15	STG_R14	STG_R13	STG_R12
34H (52)	Start G-ch Gain Reg (low byte)	00	STG_G11	STG_G10	STG_G9	STG_G8	0	0	0	0
35H (53)	Start G-ch Gain Reg (high byte)	00	0	0	0	STG_G16	STG_G15	STG_G14	STG_G13	STG_G12
36H (54)	Start B-ch Gain Reg (low byte)	00	STG_B11	STG_B10	STG_B9	STG_B8	0	0	0	0

Part 3: Shading Gamma, continued

Addr (dec)	Name	Default (hex)	Content							
			bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
37H (55)	Start B-ch Gain Reg (high byte)	00	0	0	0	STG_ B16	STG_ B15	STG_ B14	STG_ B13	STG_ B12
38H (56)	Start_Img Reg (low byte)	00	STI_ AD11	STI_ AD10	STI_ AD9	STI_ AD8	0	0	0	0
39H (57)	Start_Img Reg (high byte)	00	0	0	0	STI_ AD16	STI_ AD15	STI_ AD14	STI_ AD13	STI_ AD12

Part 4: Motor Control

Addr (dec)	Name	Default (hex)	Content							
			bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
3AH (58)	Motor behav register	00	AUTO _PK	*MTR_ DRV_S*	*DUAL_ MTR*	Mtr_C_ Ctrl	Micro _step	M_Full _step	MTR _2PH	MTR _CDIR
3BH (59)	Motor speed register	00	0	MTPK _SP2	MTPK _SP1	MTPK _SP0	0	MTS _SP2	MTS _SP1	MTS _SP0
3CH (60)	Motor PWM_P register	00	PWM_ FC_7	PWM_ FC_6	PWM_ FC_5	PWM_ FC_4	PWM_ FC_3	PWM_ FC_2	PWM_ FC_1	PWM_ FC_0
3DH (61)	Motor PWM_D register	00	0	0	PWM_ DC_5	PWM_ DC_4	PWM_ DC_3	PWM_ DC_2	PWM_ DC_1	PWM_ DC_0
3EH (62)	Motor speed up register 1	00	1/4_ STP_3	1/4_ STP_2	1/4_ STP_1	1/4_ STP_0	½_ STP_3	½_ STP_2	½_ STP_1	½_ STP_0
3FH (63)	Motor speed up register 2	00	0	0	0	0	1/8_ STP_3	1/8_ STP_2	1/8_ STP_1	1/8_ STP_0
40H (64)	Motor pause step register	00	0	0	0	0	Mtr_ PS_3	Mtr_ PS _2	Mtr_ PS_1	Mtr_ PS _0
41H (65)	Back tracking reg.	00	BKTR 7	BKTR 6	BKTR 5	BKTR 4	BKTR 3	BKTR 2	BKTR 1	BKTR 0

Part 5: Image Buffer, Line Art and Shading Process and Scanning Area

Addr (dec)	Name	Default (hex)	Content bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
42H (66)	Memory type register	80	DRAM	0	0	MDS -16	0	ADDL _2	ADDL _1	ADDL _0
43H (67)	Line art Threshold register	00	LART_ TH7	LART_ TH6	LART_ TH5	LART_ TH4	LART_ TH3	LART_ TH2	LART_ TH1	LART_ TH0
44H (68)	Img LL Th register	00	Img_ LLT _7	Img_ LLT _6	Img_ LLT _5	Img_ LLT _4	Img_ LLT _3	Img_ LLT _2	Img_ LLT _1	Img_ LLT _0
45H (69)	Img FML register	00	Img_ FML _7	Img_ FML _6	Img_ FML _5	Img_ FML _4	Img_ FML _3	Img_ FML _2	Img_ FML _1	Img_ FML _0
46H (70)	Start point of shading reg (low byte)	00	STRT _SDN7	STRT _SDN6	STRT _SDN5	STRT _SDN4	STRT _SDN3	STRT _SDN2	STRT _SDN1	STRT _SDN0
47H (71)	Start point of shading reg (high byte)	00	0	0	0	0	STRT _SDN 11	STRT _SDN 10	STRT _SDN9	STRT _SDN8
48H (72)	Start point of x-axis reg (low byte)	00	STRT _X7	STRT _X6	STRT _X5	STRT _X4	STRT _X3	STRT _X2	STRT _X1	STRT _X0
49H (73)	Start point of x-axis reg (high byte)	00	0	0	STRT _X13	STRT _X12	STRT _X11	STRT _X10	STRT _X9	STRT _X8
4AH (74)	End point of x-axis reg (low byte)	00	END _X7	END _X6	END _X5	END _X4	END _X3	END _X2	END _X1	END _X0
4BH (75)	End point of x-axis reg (high byte)	00	0	0	END _X13	END _X12	END _X11	END _X10	END _X9	END _X8

Part 5: Image Buffer, Line Art and Shading Process and Scanning Area, continued

Addr (dec)	Name	Default (hex)	Content							
			bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
4CH (76)	Start point of y-axis reg (low byte)	00	STRT _Y7	STRT _Y6	STRT _Y5	STRT _Y4	STRT _Y3	STRT _Y2	STRT _Y1	STRT _Y0
4DH (77)	Start point of y-axis reg (high byte)	00	STRT _Y15	STRT _Y14	STRT _Y13	STRT _Y12	STRT _Y11	STRT _Y10	STRT _Y9	STRT _Y8
4EH (78)	End point of y-axis reg (low byte)	00	END _Y7	END _Y6	END _Y5	END _Y4	END _Y3	END _Y2	END _Y1	END _Y0
4FH (79)	End point of y-axis reg (high byte)	00	END _Y15	END _Y14	END _Y13	END _Y12	END _Y11	END _Y10	END _Y9	END _Y8

Part 6: System Control

Addr (hex)	Name	Default (hex)	Content							
			bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
50H (80)	Modes configure register	00	0	SHUT_ OVLP	COL_ TYP1	COL_ TYP0	0	L_ART	SPEE D_MD	PIX_ MD
51H (81)	X-resolution register	00	0	0	AFE_ DS1	AFE_ DS0	REXL _X3	REXL _X2	REXL _X1	REXL _X0
52H (82)	Y-resolution register	00	0	0	0	0	REXL _Y3	REXL _Y2	REXL _Y1	REXL _Y0
5CH (92)	Command register	00	ABRT_ SCN	RESE T	MCKS _1	MCKS _0	0	PARK	STRT_ NSCN	STRT_ SCN

Part 7: General I/O and Special Registers

Addr (dec)	Name	Default (hex)	Content							
			bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
5EH (94)	General IO direction register 1	0F	LTHP3	LTHP2	LTHP1	LTHP0	GDR3	GDR2	GDR1	GDR0
5FH (95)	General IO direction register 2	07	0	LTHP6	LTHP5	LTHP4	0	GDR6	GDR5	GDR4
60H (96)	General IO register 1	00	LTHI3	LTHI2	LTHI1	LTHI0	GIO3	GIO2	GIO1	GIO0
61H (97)	General IO register 2	00	0	LTHI6	LTHI5	LTHI4	0	GIO6	GIO5	GIO4
62H (98)	Special_IP register	00	0	0	0	0	0	HOME	LTH_M_PRES	M_PRES
63H (99)	LL_driver register	04	CCD_LPON	0	LEDI_ST1	LEDI_ST0	SIG_O_ON	HOME_P	0	0
64H (100)	Interrupt enable register	00	Buffer_FUL	EOS	HOME	LTH_M_PRES	LTHI3	LTHI2	LTHI1	LTHI0
65H (101)	Interrupt clear register	00	Buffer_FUL	EOS	HOME	LTH_M_PRES	LTHI3	LTHI2	LTHI1	LTHI0
66H (102)	Add_Fun_Reg2	00	LAMP_PWM	0	0	0	0	0	0	0

6. SCANNER ASIC CIRCUIT

Scanner ASIC circuit services USB command from USB interface circuit, decodes the commands, control the scanner system and generates timing for CCD/CIS interface, AFE circuit, image buffer memory, motor control and other I/O interface. The image data converted by 16-bit ADC in AFE circuit is buffered in AFE interface circuit, the data will write to image buffer memory and finally transfered to the double FIFO in the USB interface circuit. The reference clock of scanner ASIC circuit is MCLK and is derived from 24 MHz crystal clock and 48 MHz of internal PLL output clock.

6.1 Command Decoder and Interrupt

The USB interface will be enabled if the RXD/SPE pin is low. The detail of USB bulk out, bulk in and interrupt in transaction refer to section 9, the address and data definition are listed in each bit content and address mapping tables.

There are four bytes of Host command: command code, address/index_high, data/index_low and extend byte.

Command Code:

Bit [1:0], select which channel of table access.

Bit [1:0] = 00: R-channel.
01: G-channel.
10: B-channel.
11: reserved.

Bit [3:2], select which table to be accessed.

Bit [3:2] = 00: reserved.
01: Offset shading table.
10: Gain shading table.
11: gamma table.

Bit [5:4], reserved (must set to 00).

Bit 6 = 1: table access.
0: register access.

Bit 7, read/write action.

Bit 7 = 1: register or table read.
0: register/command write or table download.

Address/Index_high

Defines:

1. Register address.
2. Table index bit [15:8] of read table action.

Data/Index_low

Defines:

1. Data of register write.
2. Table index bit [7:0] of read table action. 00H is the start byte (or word) of the table, 01H is the next content byte (or word) the table.

Extend Byte:

Reserved.

Command Type

Software Reset

The software reset write from Host are via USB bulk out transaction at USB endpoint 1, this command will force to reset the USB command interface and scanner ASIC circuit, the system clock of scanner ASIC and enable/disable of internal 5V to 3.3V regulator also can be configured during software reset. This command must activated before any registers programmed.

1. Code byte = 00H.
2. Address byte, the address must be (5CH).
3. Data byte, the data must be any one of 40H, 48H, 50H, 58H, 60H or 68H.

   40H when system clock is 24M, 50H when system clock is 36M, 60H when system clock is 48M, internal 5V to 3.3V power regulator can be disabled by set bit 3 to high.

   4 Extend byte, reserved.

Table Download Command

The table may be offset/gain or gamma of R, G or B channel. The data length of shading table and gamma table is configured in shading/gamma set register. The following bulk out commands must be 8 bytes packet size to download the table, the bulk out command with zero length or less than 8 bytes must activated to end the table download.

1. Command code byte: 4XH, bit [3:0] select which channel of which table to be down-loaded.
2. Address, this byte is ignored.
3. Data byte, this byte is ignored.
4. Extend byte, reserved.

Table Read Command

The table may be offset/gain or gamma of R, G or B channel. The data length of shading table and gamma table is configured in shading/gamma set register. The following bulk in command has two byte to be read if the data length over 8 bits.

1. Command code byte: CXH, bit [3:0] select which channel of which table to be read.
2. Index high byte: high byte of the table index.
3. Index low byte: low byte of the table index.
4. Extend byte, reserved.

The USB bulk in transaction for data read in are listed as follows:

1. Data byte or data high byte.
2. Data low byte, when the data length of the read table is over 8 bits.

Register or Command Write

The register write or command write from Host are via USB bulk out transaction at USB endpoint 1. The USB bulk out transaction for register or command write are listed as follows:

1. Code byte = 00H.
2. Address byte:

   Bit [7:0], defines the register address map of the W6668.
3. Data byte:

   Bit [7:0], is the data to be write to the assigned register.
4. Extend byte, reserved.

Register Read

There are two stages for the register read access, the first stage is read command and register address activates from Host through USB bulk out transaction at USB endpoint 1 and the second stage is the data read in via USB bulk in transaction at USB endpoint 2. The start scan, start no scan and park command also can be read back to check the command is processing or finished. The USB bulk out transaction for register read are listed as follows:

1. Code byte = 80H.
2. Address byte:

   Bit [7:0], defines the register address map of the W6668.
3. Data byte:

   Bit [7:0], is ignored during read.
4. Extend byte, reserved.

The USB bulk in transaction for data read in are listed as follows:

1. Data byte, data content to be read

Scan Command and Image Data In

The image data in command from Host are via USB bulk out transaction at USB endpoint 1. The USB bulk out transaction for scan command and image data in are listed as follows:

1. Code byte = 00H.
2. Address byte:

   The address must be (5CH).
3. Data byte:

   The data must be 01H.
4. Extend byte, reserved.

   The image data in to Host are via USB bulk in transaction at USB endpoint 2.

Abort Scan Command Write

The abort scan command write from Host are via USB bulk out transaction at USB endpoint 1, this command will force to transmit the abort scan command from Host to scanner ASIC circuit even if the image data in transaction is going on.

1. Code byte = 00H.
2. Address byte:

   The address must be (5CH).
3. Data byte:

   The data must be 80H.
4. Extend byte, reserved.

Interrupt In

The data length of interrupt in is one byte, the USB interrupt transaction will be activated if any bit changing from low to high, the interrupt source can be masked (disabled) if write 0 to the related bit in the interrupt enable register. The content of the interrupt in is:

Bit [3:0]: Latched GIO[3:0] pin, when the signal of LTHI[3:0] bits in General IO register is set.

Bit 4: Latched M_PRES, when the signal of LTH_M_PRES bit in Special IP register is set.

Bit 5: HOME, active when the optical module has been back to home position.

Bit 6: End of Scan, this bit will issue interrupt if the scan command or start no scan command has been processed completely.

Bit 7: Image buffer full, the motor will stop scan forward and interrupt will be activated with this bit high.

7. USB INTERFACE CIRCUIT

USB interface circuit includes USB transceiver, USB serial interface engine (SIE), USB transaction control logic, USB endpoint control logic and endpoint circuit. The USB transaction control logic and USB endpoint control logic also called USB serial interface logic (SIL). Figure 7-1 shows the detail block diagram of USB interface circuit.

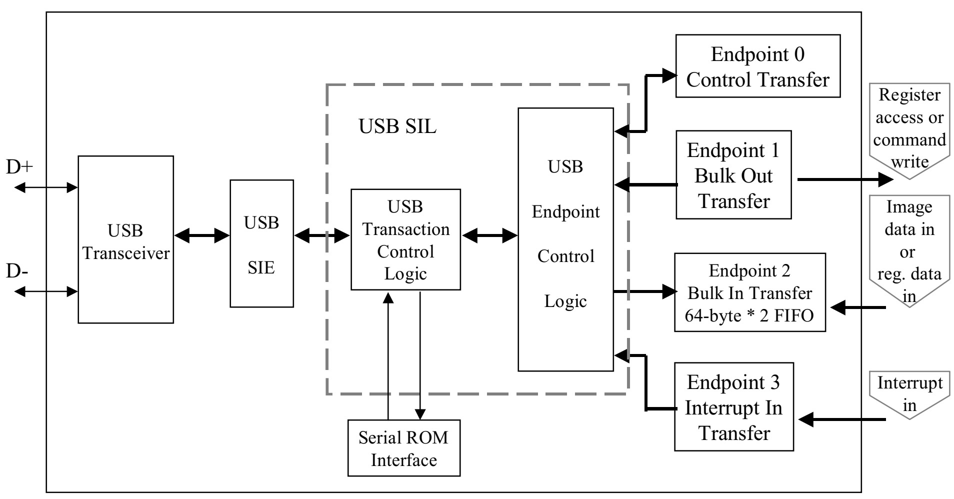


Fig. 7-1 Block Diagram of USB Interface Circuit.

USB transceiver accept analog USB D+ and D- signal from USB Host or USB Hub. The internal digital data stream is converted from the USB D+ and D- and the USB bus state of connect, disconnect, idle, resume and reset are also recognized by the USB transceiver. USB transceiver accept transmit data stream from SIE, convert to analog USB D+ and D- signal and transmit to USB Host or USB Hub. Figure 7-2and 7-3 show the analog eye pattern of USB D+ and D- waveform with 1M of USB cable and 5M of USB cable.

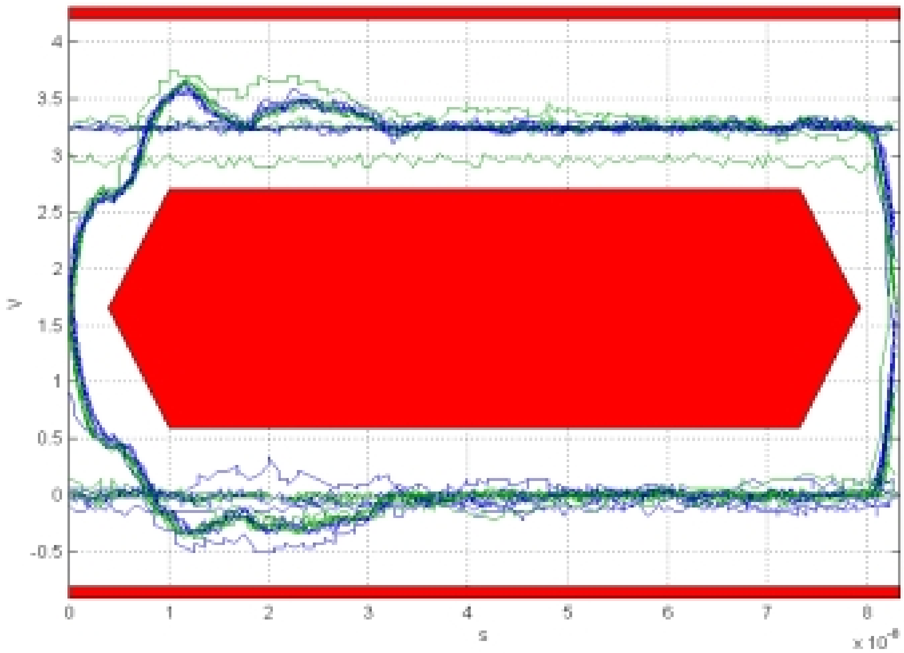


Figure 7-2 Eye Pattern of USB D+ and D- Signals with 1M of USB Cable.

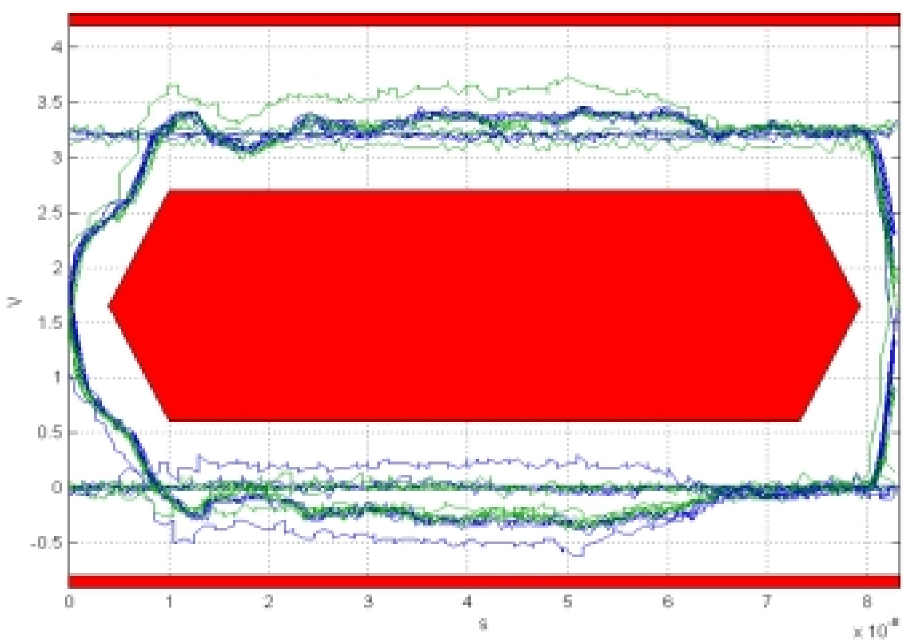


Figure 7-3 Eye Pattern of USB D+ and D- Signals with 5M of USB Cable.

Serial interface engine (SIE) accept the serial data stream from USB transceiver, recognize packet boundary, convert to parallel data and transfer to SIL circuit. The transmit data also converted to serial data stream, packeted and transfered to USB transceiver.

USB serial interface logic (SIL) is consisted of USB transaction control logic and USB endpoint control logic. There are four endpoints consisted in USB interface circuit. Endpoint 0 is control transfer, the transaction is 8 bytes packet size of bi-direction data transfer for device setup and configuration. Endpoint 1 is bulk out transfer, the transaction is 4 bytes packet size of unidirection data transfer for scanner control command from Host to scanner, another transaction is 8 bytes packet size of unidirection data transfer for shading and gamma table download from Host to scanner. Endpoint 2 is bulk in transfer, the main transaction is 64 bytes packet size double buffer of unidirection data transfer for scanner image data to Host, another transaction is one byte of unidirection data transfer for register data read back to Host or one or two bytes of unidirection data transfer for shading and gamma table data read back to Host. There are two 64-byte FIFO in the endpoint 2 circuit and are used to buffered the image data between image buffer memory and USB bulk in transaction. Endpoint 3 is interrupt transfer, the transaction is 1 bytes packet size of unidirection data transfer for interrupt information to Host.

7.2 Serial ROM Access

The serial ROM interface is used to access the serial EEPROM as 93C46 type. The vender ID, product ID are pre-stored in and can be read back after the system is power on or after reset action. Figure 7-4 is the read timing of serial ROM interface. The following table is the content description of the serial EEPROM.

Address*	Content	Description
0	iVender / Device Desc, Low-byte.	Vender ID.
1	iVender / Device Desc, High-byte.	Vender ID.
2	iProduct / Device Desc, Low-byte.	Product ID.
3	iProduct / Device Desc, High-byte.	Product ID.
4	bcdDevice / Device Desc, Low-byte.	Device releaseNo. in bcd code.
5	bcdDevice / Device Desc, High-byte.	Device releaseNo. in bcd code.
6	bmAttribute / Configuration Desc.	Bit7: Bus Powered. Bit6: Self Powered. Bit[5:0]: Reserved.
7	MaxPower / Configuration Desc.	Maximum Power consumption = n x 2 mA.

*: The address is the byte address not the write address of the EEPROM except address 0.

Table 7-1: Content description of EEPROM.

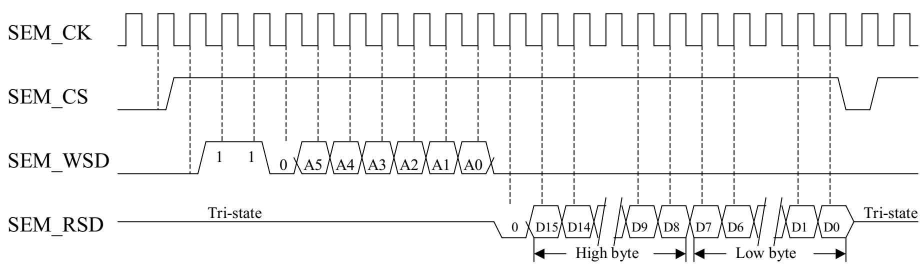


Fig. 7-4 Serial EEPROM Read Timing.

If no serial ROM is used, the SEM_CS, SEM_SK, SEM_WSD and SEM_RSD pins also can be used to select the default vender ID and product ID codes during hardware reset action by connecting these four pins to high, the un-connected pin will be recognized as low state. Any of these four pins driven high will disable serial ROM read action and default vender ID and product ID code will be configured. The following table listed the default vendor/product ID can be selected.

Item	DFT_PDS[3:0]	Vendor/Product ID Code	Description
0	0000		Serial ROM read access.
1	0001	0416/6481	Winbond Vendor/Product ID Code.
2	0010		Vendor/Product ID Code 1.
3	0011		Vendor/Product ID Code 2.
4	0100		Vendor/Product ID Code 3.
5	0101		Vendor/Product ID Code 4.
6	0110		Vendor/Product ID Code 5.
7	0111		Vendor/Product ID Code 6.
8	1000		Vendor/Product ID Code 7.
9	1001		Vendor/Product ID Code 8.
10	1010		Vendor/Product ID Code 9.
11	1011		Vendor/Product ID Code 10.
12	1100		Vendor/Product ID Code 11.
13	1101		Vendor/Product ID Code 12.
14	1110		Vendor/Product ID Code 13.
15	1111		Vendor/Product ID Code 14.

Table 7-2: Default vendor ID and product ID select table.

8. ELECTRICAL CHARACTERISTICS

8.1. Maximum Ratings*

	Parameter	Symbol	Rating	Units
1	Supply Voltage with respect to V_{AVSS} (at AVDD pin)	V_{AVDD}	-0.3 to 6	V
2	Supply Voltage with respect to V_{DVSS} (at DVDD pin)	V_{DVDD}	-0.3 to 6	V
3	Supply Voltage with respect to V_{DIVSS} (at DIVDD pin)	V_{DIVDD}	-0.3 to 6	V
4	Supply Voltage with respect to V_{UVSS} (at UVDD pin)	V_{UVDD}	-0.3 to 6	V
5	Voltage on any pin other than V_{DVSS} supplies		-0.3 to V_{dd5} + 0.3	V
6	Current at any pin other than supplies		0 to 10	mA
7	Storage Temperature	T_{st}	-65 to 150	℃

* Exceeding these values may cause permanent damage.

8.2. Recommended Operating Conditions

	Characteristics	Symbol	Rating	Unit
1	Operation Voltage (referenced to AVSS pin).	V_{AVDD}	4.75 to 5.25	V
2	Operation Voltage (referenced to DVSS pin).	V_{DVDD}	4.75 to 5.25	V
3	Operation Voltage (referenced to DIVSS pin).	V_{DIVDD}	3.0 to 3.6	V
4	Operation Voltage (referenced to UVSS pin).	V_{UVDD}	3.0 to 3.6	V
5	Clock Frequency	f_{XTL}	24	MHz
6	Clock Frequency Tolerance	Δf_C	100	PPM
7	Operation Temperature	T_{op}	0 to 70	℃

8.3. Power Supply Characteristics

	Parameter	Condition	Symbol	Min	Typ‡	Max	Units	Test
1	Standby Supply Current	Power Supply	I_{QAVDD}			0.08	mA	Test 1
2	Operating Supply Current	(V_{AVDD} = 5.0V)	I_{AVDD}		40	TBD	mA	Test 2

‡: Typical figure are at V_{AVDD} = 5.0V and temperature = 25 ℃ and are for design aid only, not guaranteed and not subject to production testing.

Test 1: Configure as power down mode, no analog input.

Test 2: 24 MHz system clock configured.

	Parameter	Condition	Symbol	Min	Typ‡	Max	Units	Test
1	Standby Supply Current	Power Supply	I_{QDVDD}			0.01	mA	Test 1
2	Operating Supply Current	(V_{DVDD} = 5.0V)	I_{DVDD}		5	TBD	mA	Test 2

‡: Typical figure are at V_{DVDD} = 5V and temperature = 25 ℃ and are for design aid only, not guaranteed and not subject to production testing.

Test 1: All input pins are V_{DVDD} or V_{DVSS}, configure as power down mode, output without loading.

Test 2: 24 MHz system clock configured.

	Parameter	Condition	Symbol	Min	Typ‡	Max	Units	Test
1	Standby Supply Current	Power Supply	$I_{Q3.3V}$			0.05	mA	Test 1
2	Operating Supply Current	(V_{DIVDD} = 3.3V)	$I_{D3.3V}$		40	TBD	mA	Test 2

‡: Typical figure are at V_{DIVDD} = 3.3V and temperature = 25 ℃ and are for design aid only, not guaranteed and not subject to production testing.

Test 1: All input pins are V_{DVDD} or V_{DVSS}, configure as power down mode, output without loading.

Test 2: 24 MHz system clcok configured.

8.4. Digital Characteristics

	Parameter	Condition	Symbol	Min	Typ‡	Max	Units	Notes
1	Output High Voltage	(VDVDD = 5V)	V_{OH}	4.5			V	1
2	Output Low Voltage	(VDVDD = 5V)	V_{OL}			0.5	V	2
3	High Level Input Voltage	(VDVDD = 5V)	V_{IH}	2.5			V	
4	Low Level Input Voltage	(VDVDD = 5V)	V_{IL}			1.4	V	
5	Input Current		Iin			1	uA	
6	Input Capacitance		Cin		10		pF	

‡: Typical figure are at V_{DVDD} = 5V and temperature = 25 ℃ and are for design aid only, not guaranteed and not subject to production testing.

Notes:

1: The current must below or equal to the maximum source current as listed in pin descriptions section.

2: The current must below or equal to the maximum sink current as listed in pin descriptions section.

8.5. Analog Characteristics (measures from analog input to ADC output)

	Parameter	Symbol	Min	Typ‡	Max	Units	Test Conditions
Analog to Digital Converter							
1	Maximum Conversion Rate	SPS		6		MHz	
2	Resolution			16		Bits	
3	Integral Nonlinearity	INL			+/- 8	LSB	
4	Differential Nonlinearity	DNL			+/- 1.5	LSB	

8.5. Analog Characteristics (measures from analog input to ADC output), continued

	Parameter	Symbol	Min	Typ‡	Max	Units	Test Conditions
PGA & Offset DAC							
1	PGA Gain Range	G	1.0		6.0	V/V	
2	PGA Gain Resolution	G_{RES}		6		bits	Note 1
3	Offset Range	OFS	-350		+350	mV	V_{AVDD} = 5.0V
4	DAC bit number			8+sign		bits	Note 1
5	Offset Resolution	OFS_{RES}		1.36		mV	
Analog Input and Output							
1	Full Scale of Analog Input	Vin		2.0		V	Note 2
2	Input Capacitance	Cin		10		pF	
3	Signal to Noise Ratio from analog I/P to ADC O/P	SNR		70		dB	Note 3

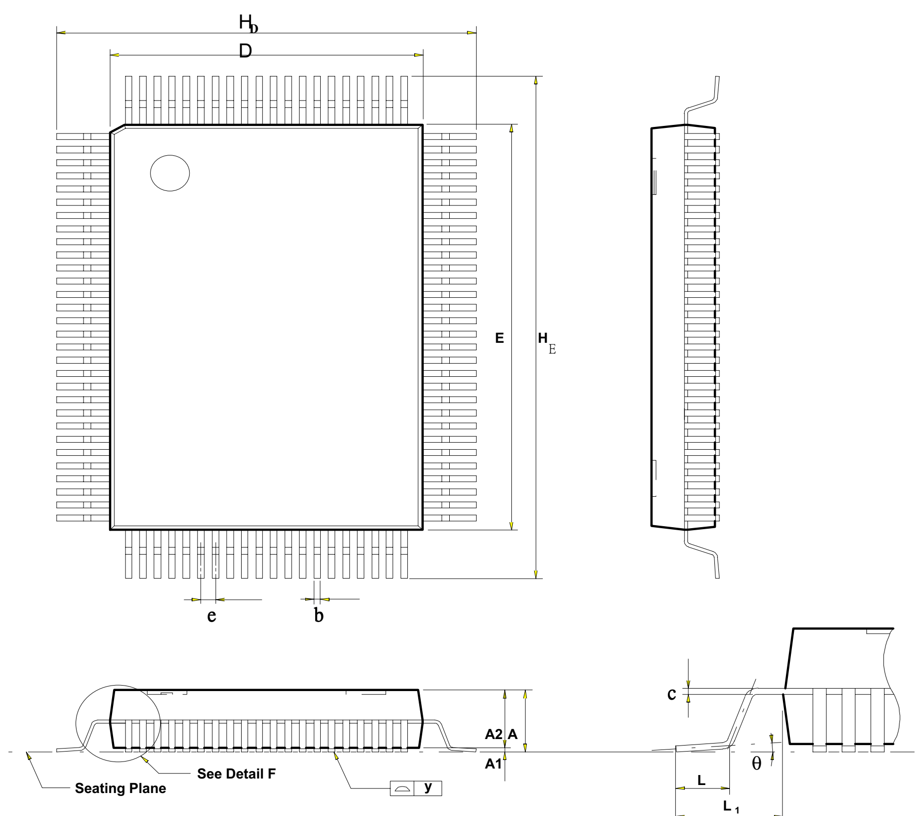
‡: Typical figure are at V_{AVDD} = 5V and temperature = 25 ℃ and are for design aid only, not guaranteed and not subject to production testing.

Note:

1. All steps of PGA gain and offset are monotonic.
2. PGA gain = 1 and offset = 0.
3. Analog signal full scale input.

9. PACKAGE INFORMATION (W6668F)

100L QFP(14x20x2.75mm footprint 4.8mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.010	0.014	0.018	0.25	0.35	0.45
A_2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.008	0.012	0.016	0.20	0.30	0.40
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
$\boxed{e}$	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.746	0.740	0.756	18.40	18.80	19.20
H_E	0.960	0.976	0.992	24.40	24.80	25.20
L	0.039	0.047	0.055	1.00	1.20	1.40
L_1	—	0.064	—	—	2.40	—
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

10. HOW TO READ THE TOP MARKING

Example: The top marking of W6668F

Winbond

W6668F

032GB2024923B-91SA

1st line: Winbond logo

2nd line: The type number W6668F

3rd line: the tracking code: 032 G B **2**024923B-91 SA

- 032: packages made in '00, week 32
- G: assembly house ID; 0 means OSE, G means GR
- B: IC version
- **2**024923B-91: wafer production series lot number
- SA: Internal use code

11. ORDERING INFORMATION

Part Number	Package Type	Production Flow
W6668F	100PQFP	Commercial, 0°C to 70°C

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III
Science-Based Industrial Park
Hsinchu, Taiwan
TEL: 886-35-770066
FAX: 886-35-789467
www: http://www.winbond.com.tw/

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502
TLX: 16485 WINTPE

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II
123 Hoi Bun Rd., Kwun Tong
Kowloon, Hong Kong
TEL: 852-27516023-7
FAX: 852-27552064

Winbond Electronics (North America) Corp.
2730 Orchard Parkway
San Jose, CA 95134 U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668