

**MOS FIELD EFFECT TRANSISTOR**  
**2SK2139**

**SWITCHING**  
**N-CHANNEL POWER MOS FET**  
**INDUSTRIAL USE**

**DESCRIPTION**

The 2SK2139 is N-Channel Power MOS Field Effect Transistor designed for high voltage switching applications.

**FEATURES**

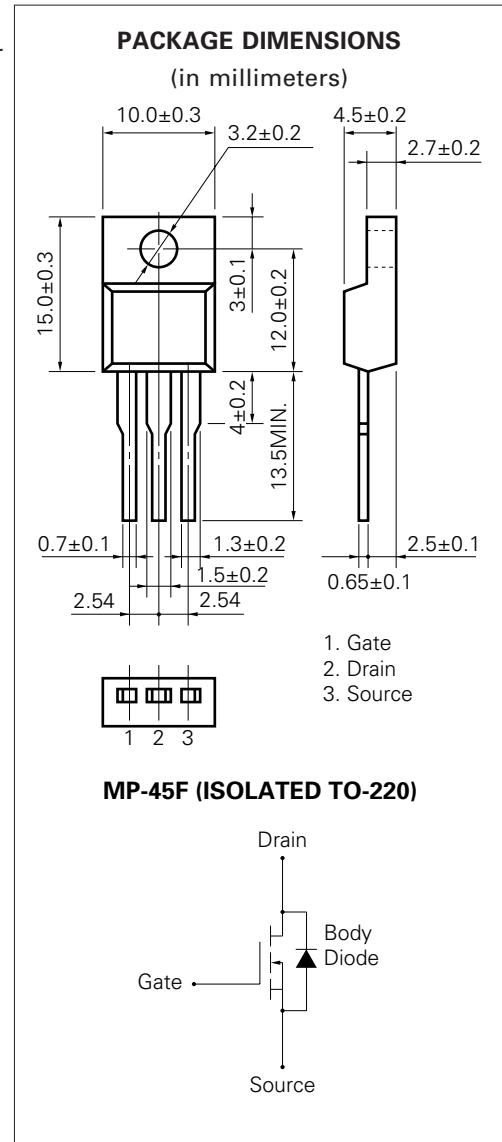
- Low On-Resistance  
 $R_{DS(on)} = 1.5 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 2.5 \text{ A)}$
- Low  $C_{iss}$   $C_{iss} = 930 \text{ pF TYP.}$
- High Avalanche Capability Ratings
- Isolate TO-220 (MP-45F) Package

**ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)**

Drain to Source Voltage	$V_{BSS}$	600	V
Gate to Source Voltage	$V_{GSS}$	$\pm 30$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 5.0$	A
Drain Current (pulse)*	$I_{D(pulse)}$	$\pm 20$	A
Total Power Dissipation ( $T_c = 25 \text{ °C}$ )	$P_{T1}$	35	W
Total Power Dissipation ( $T_A = 25 \text{ °C}$ )	$P_{T2}$	2.0	W
Channel Temperature	$T_{ch}$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C
Single Avalanche Current**	$I_{AS}$	5.0	A
Single Avalanche Energy**	$E_{AS}$	8.3	mJ

\*  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1 \%$

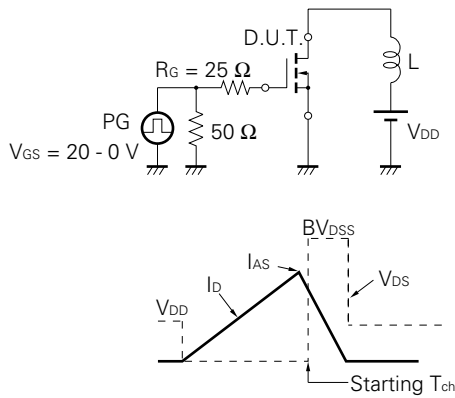
\*\* Starting  $T_{ch} = 25 \text{ °C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0$



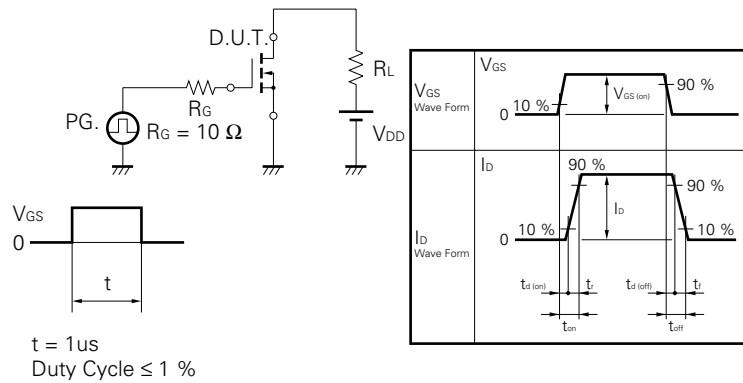
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		1.1	1.5	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.5 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	2.5		3.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	1.5			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2.5 A
Drain Leakage Current	I <sub>DSS</sub>			100	μA	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±100	nA	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		930		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		200		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		40		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		20		ns	V <sub>GS</sub> = 10 V
Rise Time	t <sub>r</sub>		10		ns	V <sub>DD</sub> = 150 V
Turn-Off Delay Time	t <sub>d(off)</sub>		60		ns	I <sub>D</sub> = 2.5 A, R <sub>G</sub> = 10 Ω
Fall Time	t <sub>f</sub>		12		ns	R <sub>L</sub> = 60 Ω
Total Gate Charge	Q <sub>G</sub>		30		nC	V <sub>GS</sub> = 10 V
Gate to Source Charge	Q <sub>GS</sub>		6.0		nC	I <sub>D</sub> = 5.0 V
Gate to Drain Charge	Q <sub>GD</sub>		15		nC	V <sub>DD</sub> = 450 V
Diode Forward Voltage	V <sub>F(S-D)</sub>		1.0		V	I <sub>F</sub> = 5.0 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		320		ns	I <sub>F</sub> = 5.0 A
Reverse Recovery Charge	Q <sub>rr</sub>		1.4		μC	di/dt = 50 A/μs

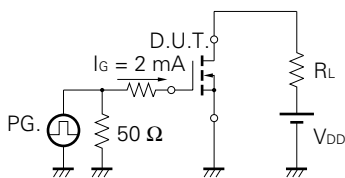
**Test Circuit 1 Avalanche Capability**



**Test Circuit 2 Switching Time**

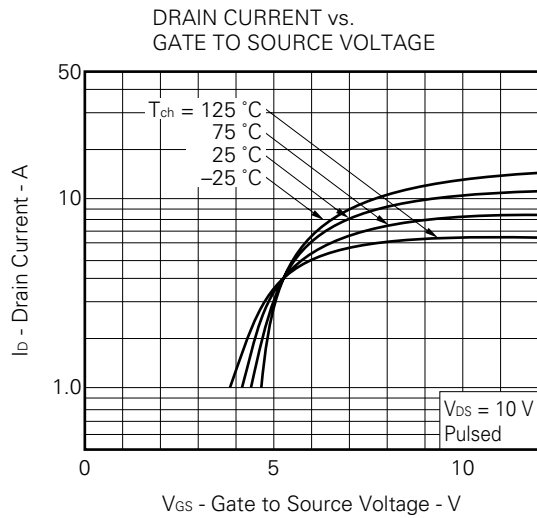
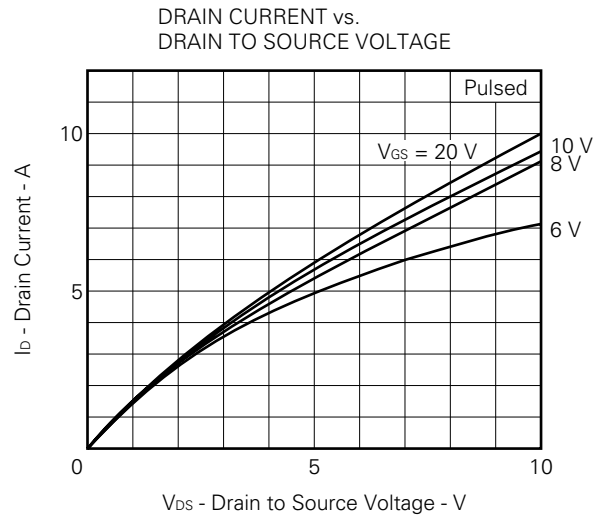
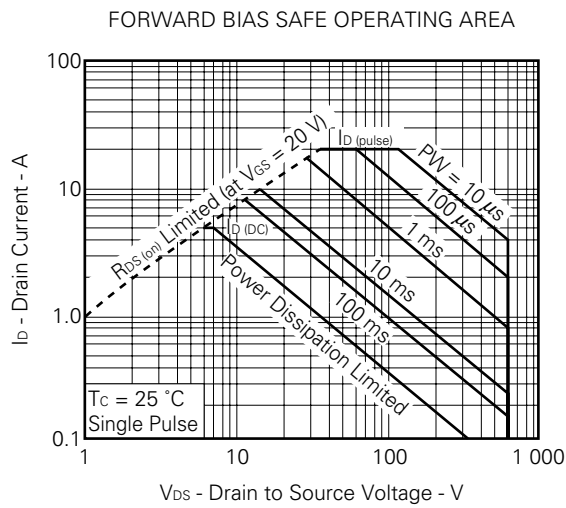
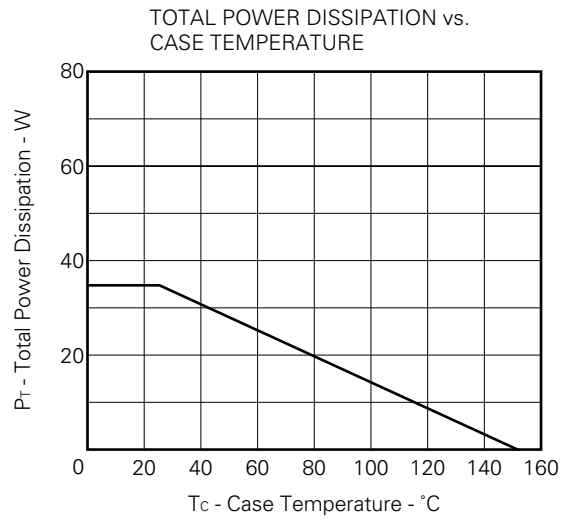
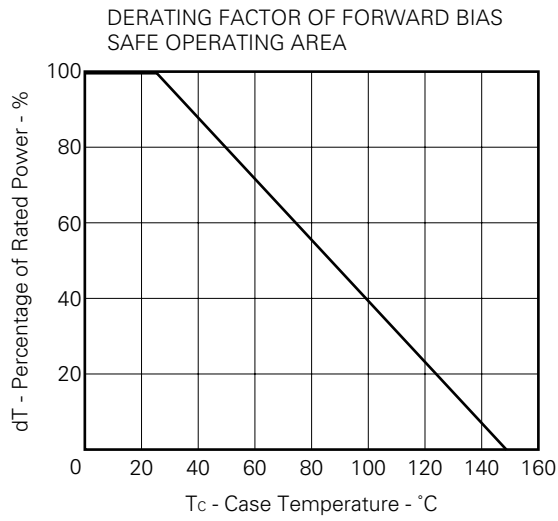


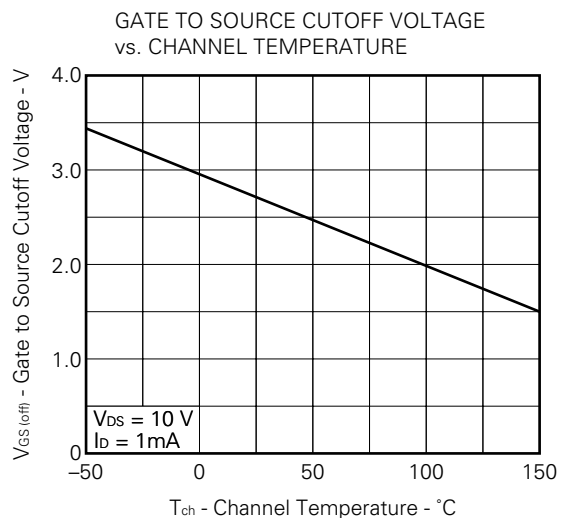
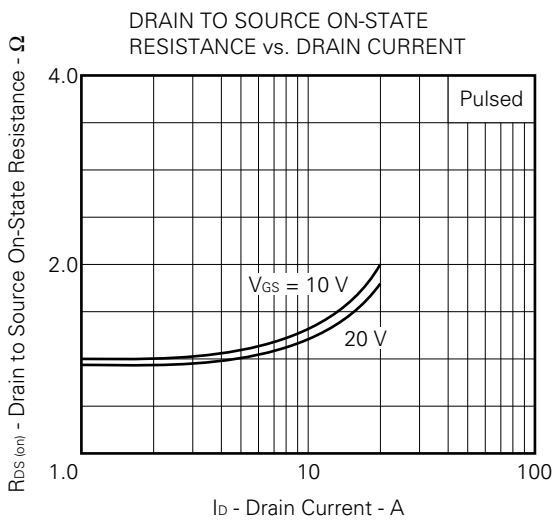
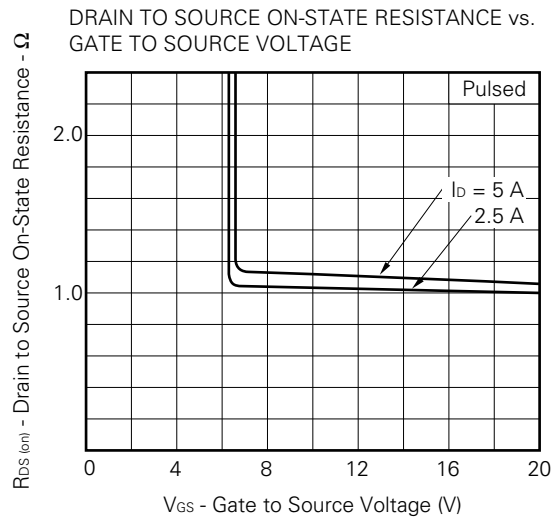
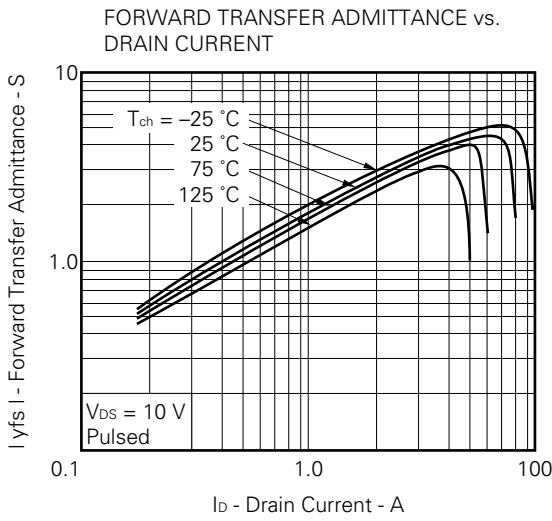
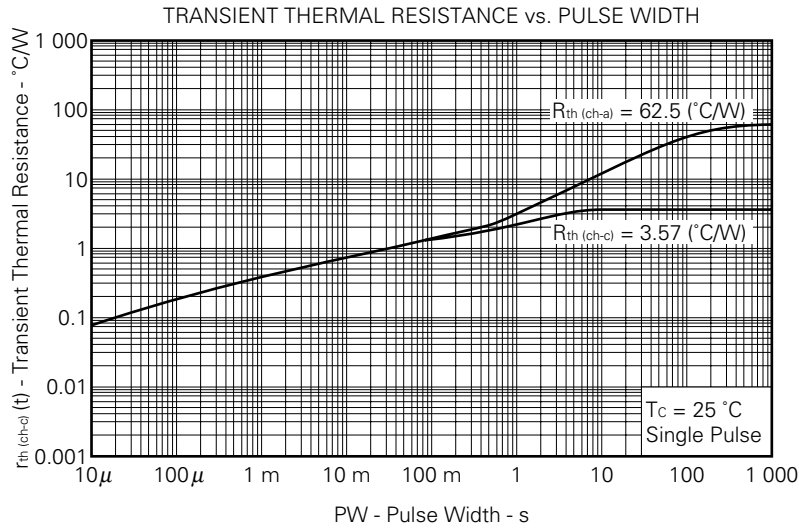
**Test Circuit 3 Gate Charge**

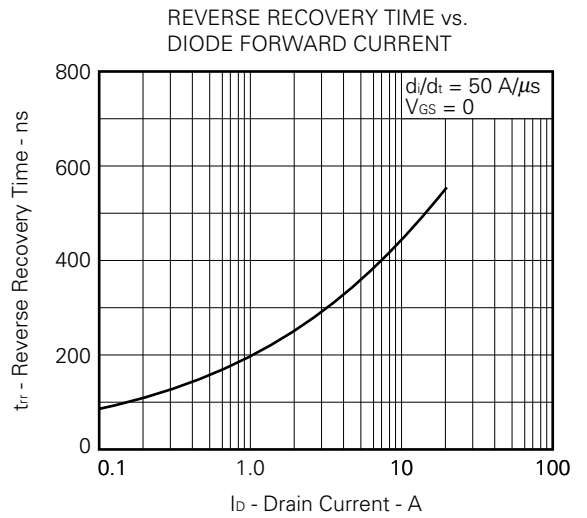
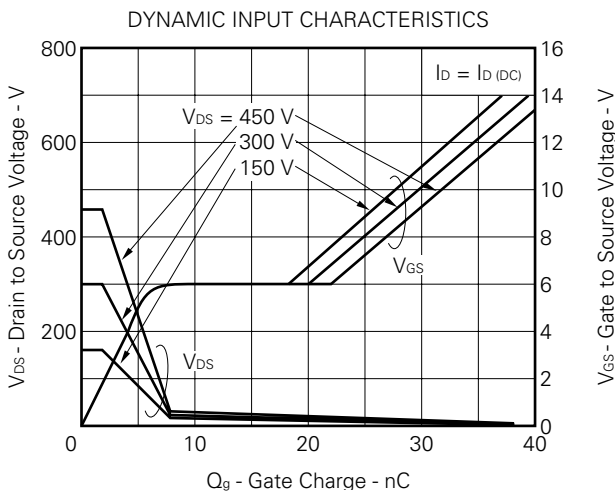
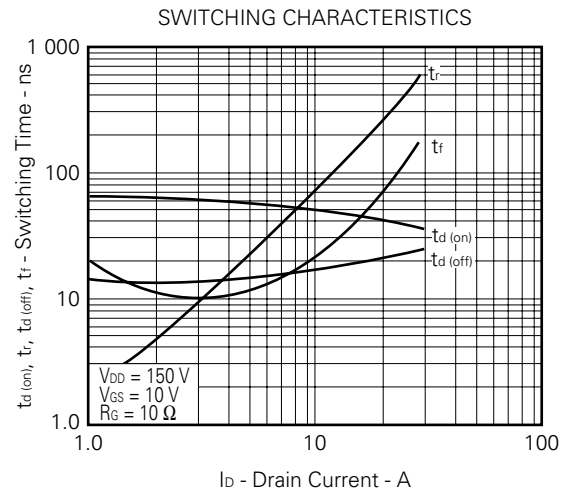
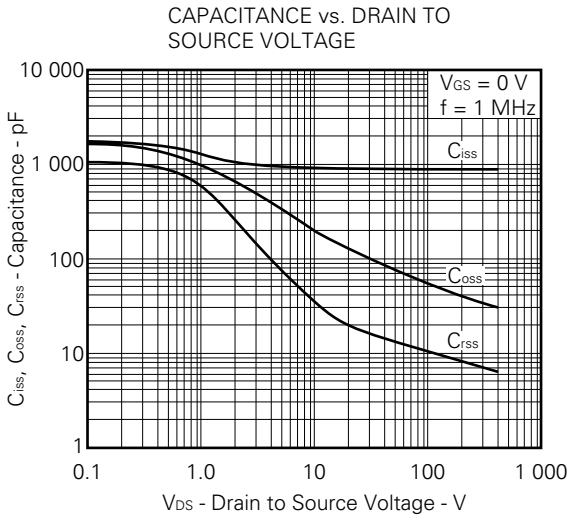
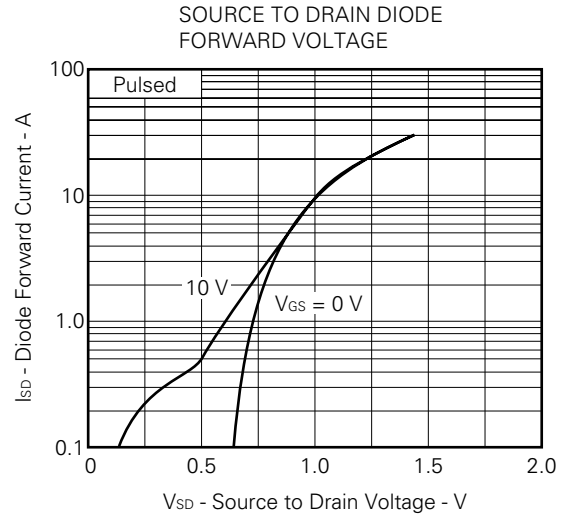
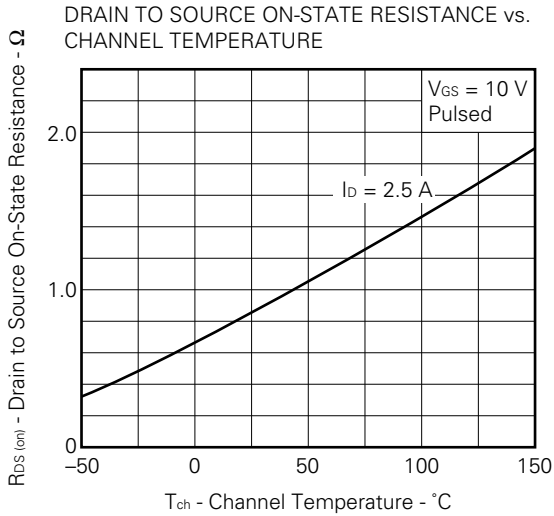


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

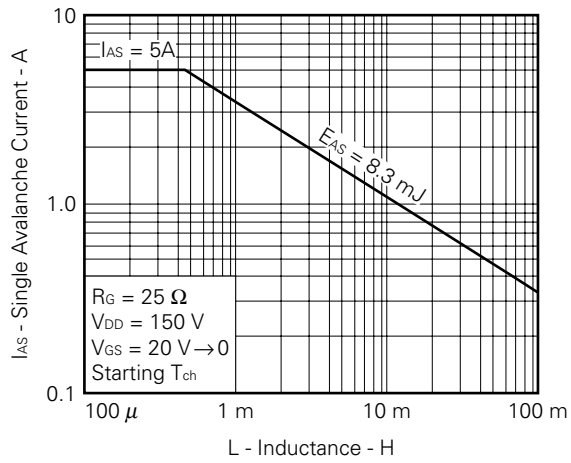
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)



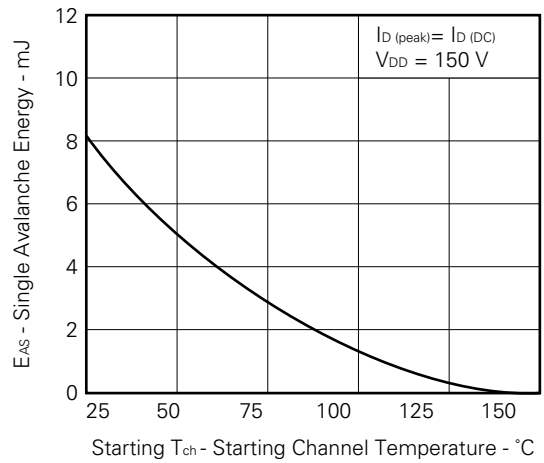




SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



**REFERENCE**

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Anti-radioactive design is not implemented in this product.