

MOS FIELD EFFECT TRANSISTOR
2SK2140, 2SK2140-Z

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK2140, 2SK2140-Z is N-channel Power MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 1.5 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 3.5 \text{ A)}$
- Low C_{iss} $C_{iss} = 930 \text{ pF TYP.}$
- High Avalanche Capability Ratings

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

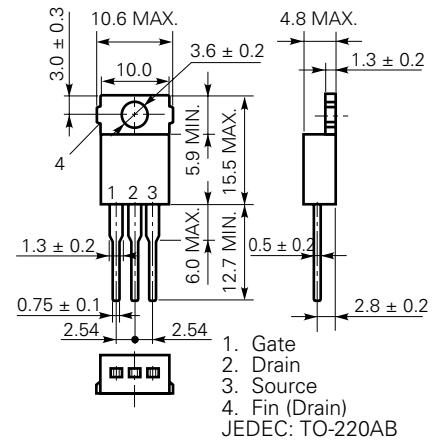
Drain to Source Voltage	V _{DSS}	600	V
Gate to Source Voltage	V _{GSS}	±30	V
Drain Current (DC)	I _{D(DC)}	±7.0	A
Drain Current (pulse)*	I _{D(pulse)}	±28	A
Total Power Dissipation (T _c = 25 °C)	P _{T1}	75	W
Total Power Dissipation (T _A = 25 °C)	P _{T2}	1.5	W
Storage Temperature	T _{stg}	-55 to +150	°C
Channel Temperature	T _{ch}	150	°C
Single Avalanche Current**	I _{AS}	7.0	A
Single Avalanche Energy**	E _{AS}	16.3	mJ

* PW ≤ 10 μs, Duty Cycle ≤ 1 %

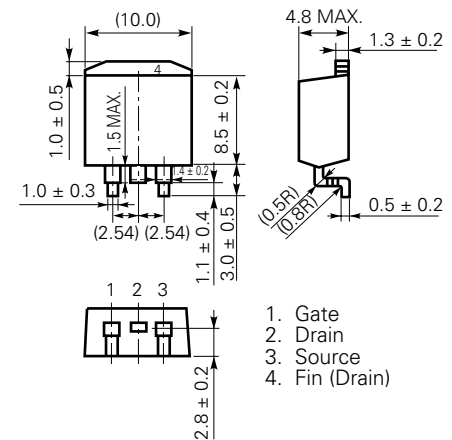
** Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0

PACKAGE DIMENSIONS

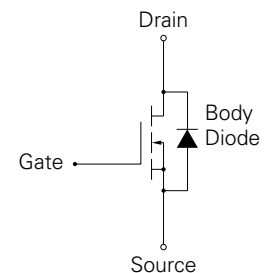
(in millimeters)



MP-25 (TO-220)



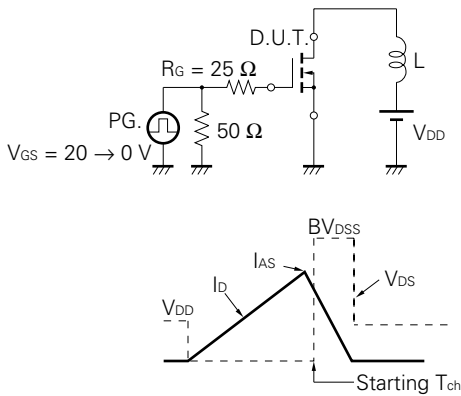
MP-25Z (SURFACE MOUNT TYPE)



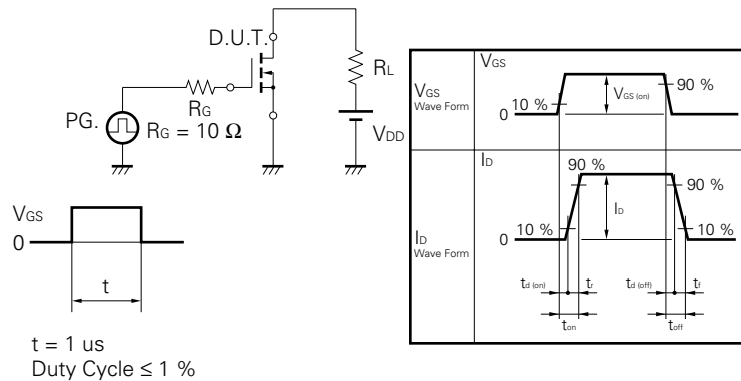
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		1.1	1.5	Ω	V _{GS} = 10 V, I _D = 3.5 A
Gate to Source Cutoff Voltage	V _{GS(off)}	2.5		3.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	1.5			S	V _{DS} = 10 V, I _D = 3.5 A
Drain Leakage Current	I _{DSS}			100	μA	V _{DS} = 600 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±100	nA	V _{GS} = ±30 V, V _{DS} = 0
Input Capacitance	C _{iss}		930		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		200		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		40		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		20		ns	V _{GS} = 10 V
Rise Time	t _r		12		ns	V _{DD} = 150 V
Turn-Off Delay Time	t _{d(off)}		60		ns	I _D = 3.5 A, R _G = 10 Ω
Fall Time	t _f		12		ns	R _L = 42.9 Ω
Total Gate Charge	Q _G		30		nC	V _{GS} = 10 V
Gate to Source Charge	Q _{GS}		6.0		nC	I _D = 7.0 V
Gate to Drain Charge	Q _{GD}		15		nC	V _{DD} = 450 V
Diode Forward Voltage	V _{F(S-D)}		1.0		V	I _F = 7.0 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		400		ns	I _F = 7.0 A
Reverse Recovery Charge	Q _{rr}		2.0		μC	di/dt = 50 A/μs

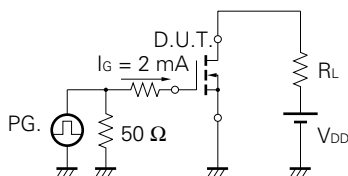
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time

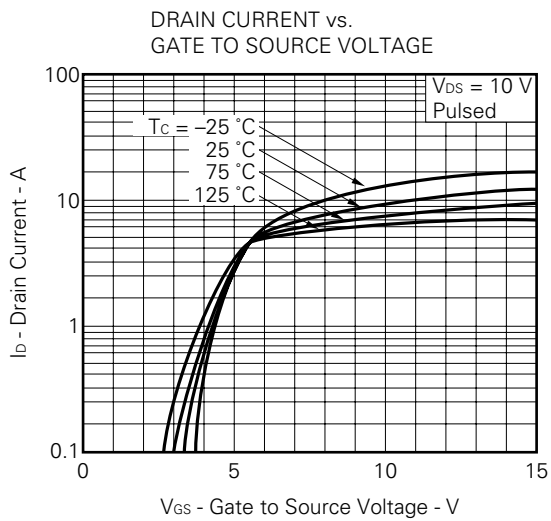
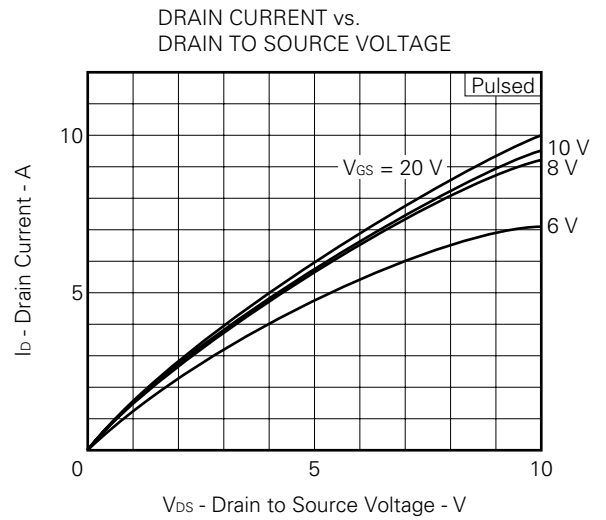
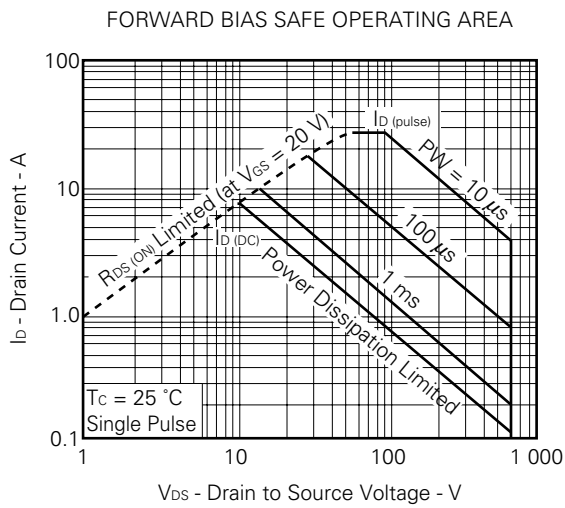
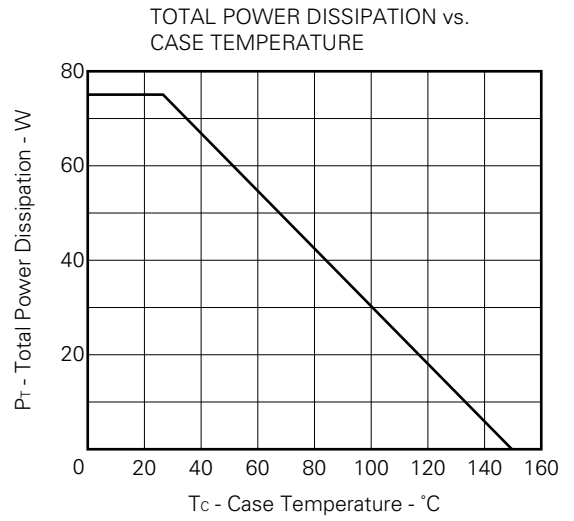
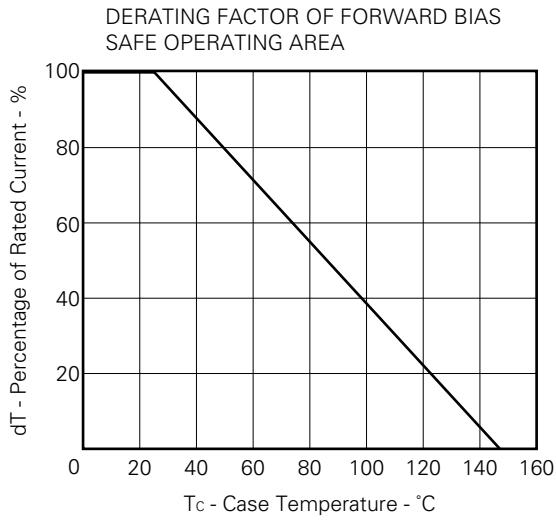


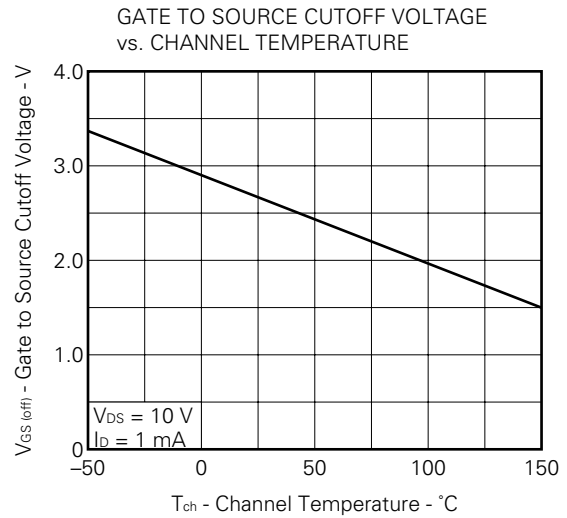
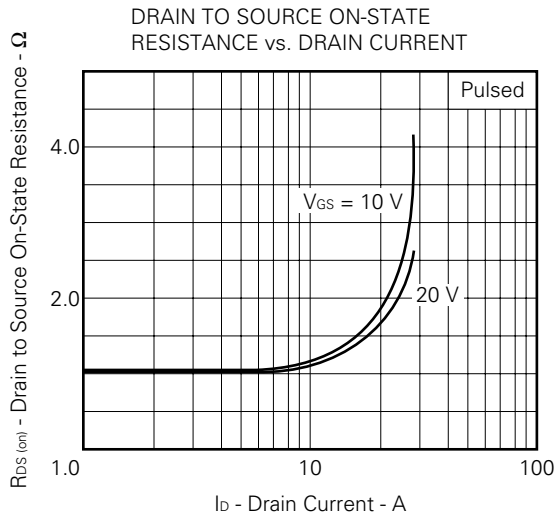
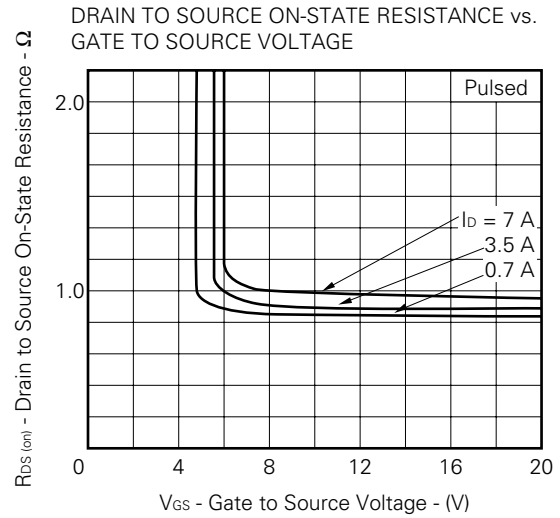
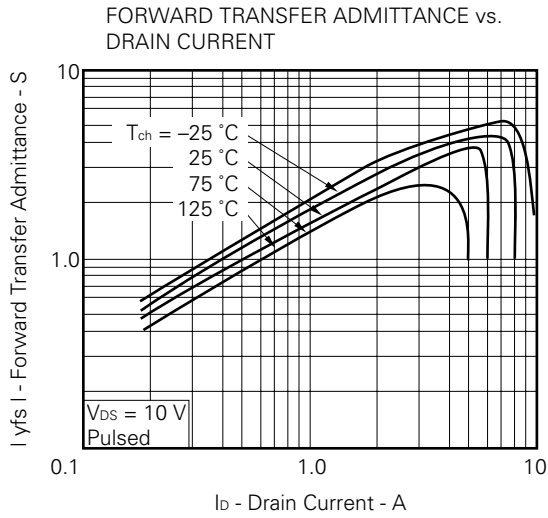
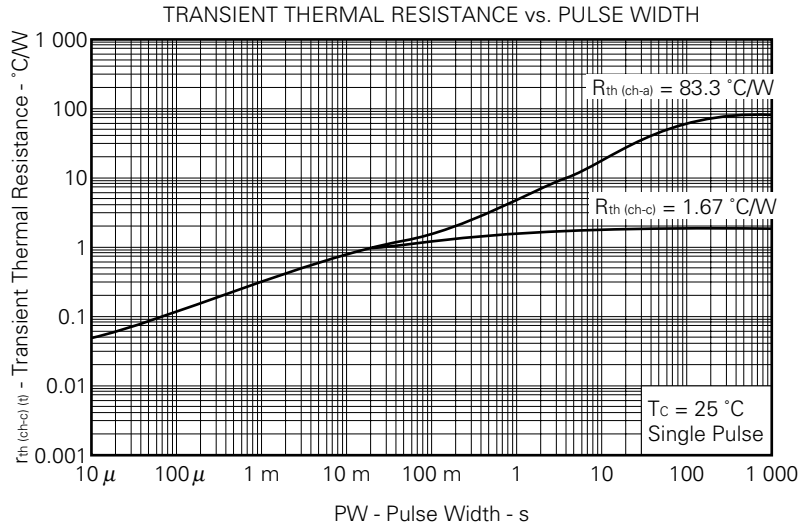
Test Circuit 3 Gate Charge

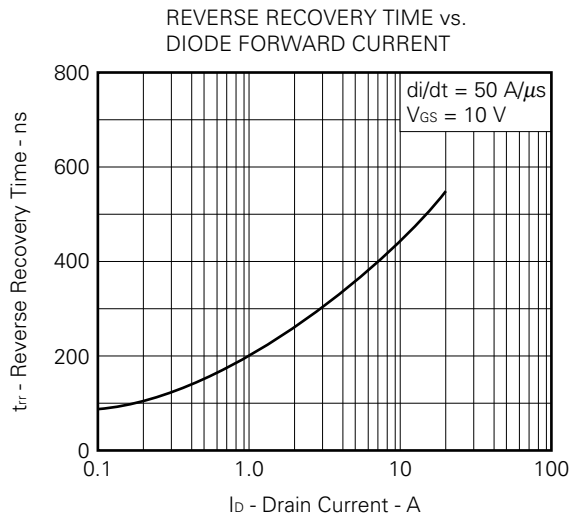
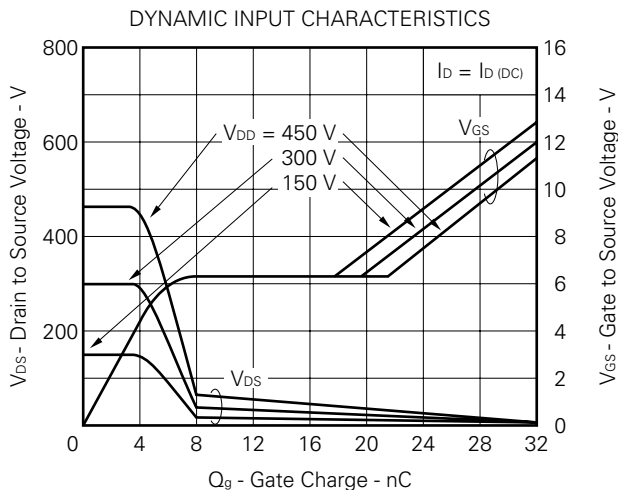
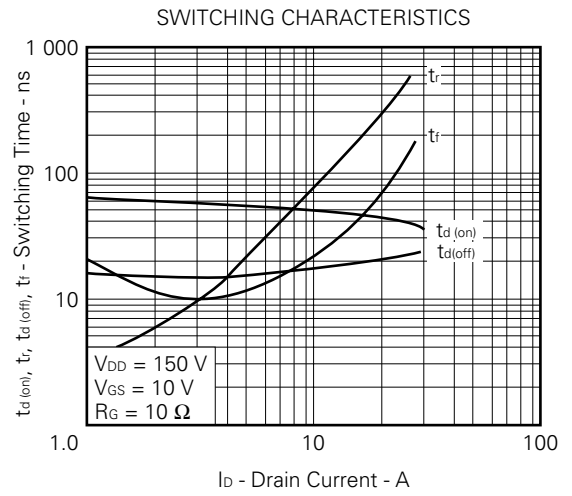
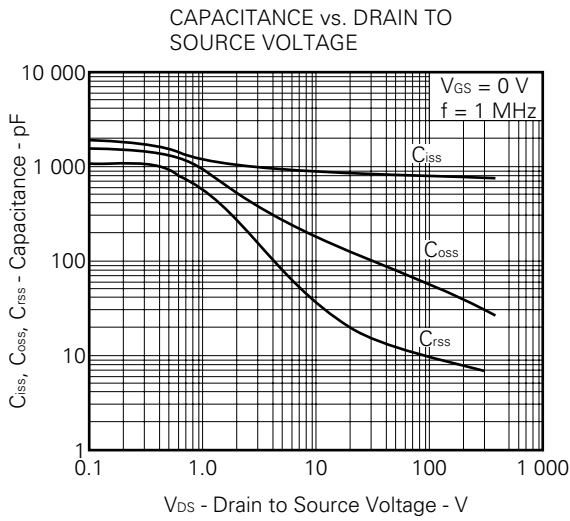
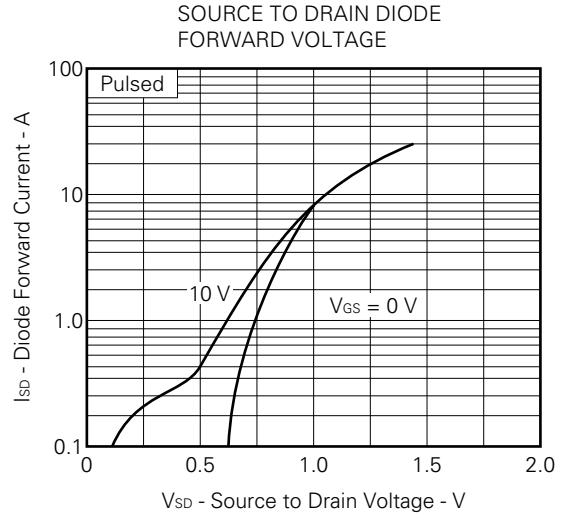
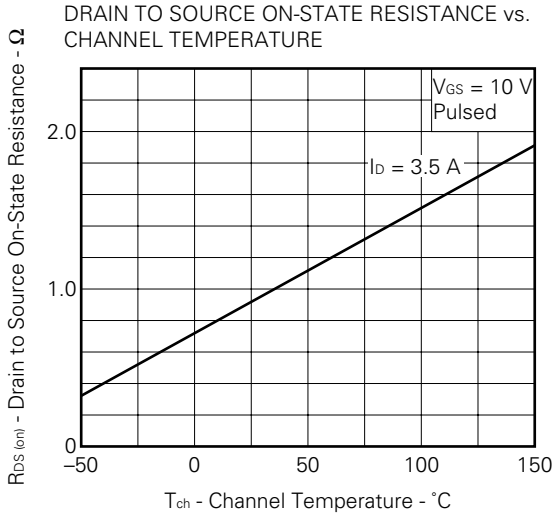


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

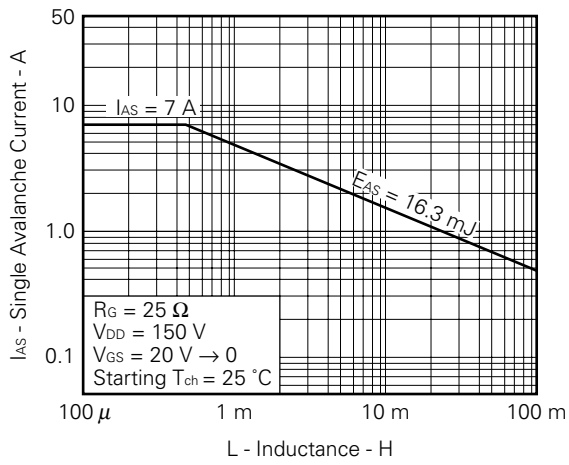
TYPICAL CHARACTERISTICS (T_A = 25 °C)



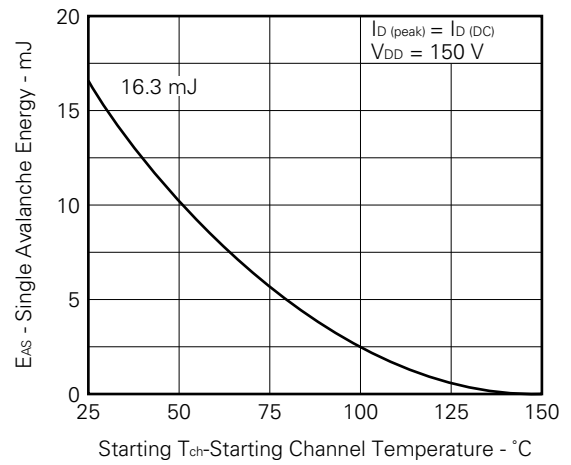




SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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Anti-radioactive design is not implemented in this product.