Preliminary W9321

Winbond Electronics Corp.

ADPCM CODEC

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1. GENERAL DESCRIPTION

The Winbond ADPCM Codec is a single channel chip incorporating a ΣΔ PCM codec filter with a 32K, 24K, 16K ADPCM encoder/decoder complying with the CCITT G.721 and G.726 standards. In addition, this chip also meets the PCM conformance specification of the CCITT G.714 recommendation.

This chip allows full-duplex operation over a wide voltage range from 2.7 to 5.25 volts; it's low power consumption makes it ideal for battery or AC powered applications. The chip includes a serial setup port (SSP) interface with a 16 byte setup and status registers. A microcontroller can access many built-in features through the SSP interface. In addition, this chip also consists of some OP amplifiers integrated with a ΣΔ PCM codec-filter to allow for easy control of the analog interface.

This chip can be used on two key applications. One application is for wireless telephone systems such as CT2, DECT. Another application is for public switch telephone network (PSTN) applications such as pair gain. See the section on application information for more details.

2. FEATURES

- Single 2.7 to 5.25 volt power supply
- Master clock rate: 10.24 MHz oscillator typically for Winbond cordless system
- Typical power consumption of 85 mW for 3 volt; power down of 0.2 mW
- Full-duplex single channel speech codec
- Linear 14 bit ΣΔ PCM codec-filter for A/D and D/A converter
- Complete Mu-Law and A-Law companding
- ADPCM transcoder for 64, 32, 24, and 16 Kbps bit rates
- Serial PCM/ADPCM transfer data rate from 128 to 2048 Kbps
- Universal programmable dual tone generator such as DTMF application
- Noise burst detection algorithm for ADPCM receive path
- Analog input: differential OP amplifier with external gain adjustment for microphone interface
- Programmable transmit gain, receive attenuation, and sidetone gain
- Analog output:
  - Differential power driver with 300 Ω load and external gain adjustment
  - Differential auxiliary driver with 300 Ω load for ringer interface
- 3 Volt regulator for digital circuit
- 5 Volt charge pump for analog circuit low voltage applications
- 16 Setup and status registers with 8 bits for monitoring microcontroller applications
- Packaged in 28-pin DIP/SOP

3. PIN CONFIGURATION

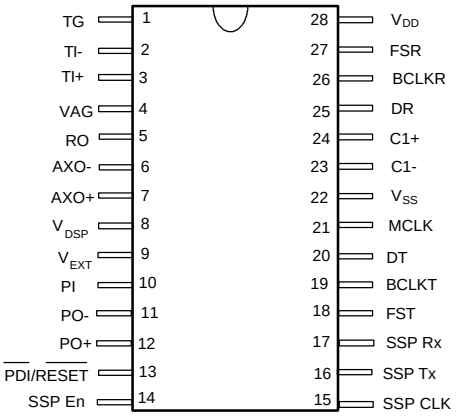

Figure 3-1

4. PIN DESCRIPTIONS

4.1. Power Control Interface

PIN NAME	PIN NO.	I/O	FUNCTION
VEXT	9	I	This pin is the external power supply between 2.7 and 5.25 volt. This pin should be decoupled to VSS with a 0.1 µF capacitor.
VDSP	8	O	This is the output of the on-chip 3 volt regulator which supplies the digital circuit of the chip. This pin should be decoupled to VSS with a 0.1 µF ceramic capacitor. This pin cannot be used for powering external loads.
VDD	28	I/O	This is the output of the on-chip 5 volt charge pump which supplies the analog circuit. When VEXT = +5V ±5%, VDD is an input and should be connected to VEXT externally. Charge pump capacitor C1+ and C1- should not be used and BR0[b2] must be written into logic "1". In this case VEXT and VDD can share the same 0.1 µF decoupling capacitor to VSS. When VEXT = 2.7 to 5.25 volt, VDD is a 5 volt charge pump output and should not be connected to VEXT. VDD should be decoupled to VSS with a 0.1 µF capacitor. This pin cannot be used for powering external loads.
VSS	22	I	This pin connects the analog and digital ground and is typically connected to 0 volt.

4.1. Power Control Interface, continued

PIN NAME	PIN NO.	I/O	FUNCTION
VAG	4	O	This is the analog ground output pin which supplies a 2.5 volt reference voltage for all analog signal processing. This pin should be decoupled to VSS with 0.1 µF capacitor. This pin becomes high impedance when the chip enters an analog power down mode.
C1+, C1-	23, 24	I	The charge pump capacitor pins. When VEXT = +5V ±5%, these capacitors C1+ and C1- should not be used and BR0[b2] must be written into logic "1". When VEXT = 2.7 to 5.25 volt, a 0.1 µF capacitor should be placed between C1+ and C1-.
PDI/RESET	13	I	The power down/reset input pin. When at logic 0, the chip enters a power down mode. When it switches from logic 0 to logic 1, this chip is active and resets the ADPCM transcoder and all circuits.

4.2. Analog Interface

PIN NAME	PIN NO.	I/O	FUNCTION
TG	1	O	This pin is the analog output of the transmit input amplifier. It can be used to set the gain by external resistors. When the chip is in analog power down mode, this pin is high impedance.
TI-	2	I	This pin is the inverting input of the transmit input amplifier. Connecting this pin and TI+ (pin-3) to VDD will force TG into a high impedance state.
TI+	3	I	The non-inverting input of the transmit input amplifier. Connecting this pin and TI- (pin-2) to VDD will force TG to be high impedance. Note this pin may be connected to the VAG pin for an inverting configuration if the input signal is referenced to the VAG pin.
RO	5	O	This pin is the non-inverting analog output of the receive smoothing filter. This pin can typically drive a 2 KΩ load to 1.13 volt peak referenced to the VAG pin. This pin may be dc referenced to either the VAG pin or VEXT/2 determined by BR2 (b7). When the chip is in analog power down mode, this pin is high impedance.
AXO-	6	O	This pin is the auxiliary inverting analog output. This pin can drive a 300 Ω load differentially. Its output can swing between 0.5 volt and VEXT. This pin may be dc referenced to either the VAG pin or VEXT/2 by BR2 (b7). When the chip is in analog power down mode, this pin is high impedance.
AXO+	7	O	This pin is the auxiliary non-inverting analog output. This pin can drive a 300 Ω load differentially. Its output can swing between 0.5 volt and VEXT. This pin may be dc referenced to either the VAG pin or VEXT/2 by BR2 (b7). When the chip is in analog power down mode, this pin is high impedance.

4.2. Analog Interface, continued

PIN NAME	PIN NO.	I/O	FUNCTION
PI	10	I	This pin is the inverting input to the PO- (pin-11) power amplifier. It may be dc referenced to either the VAG pin or VEXT/2 by BR2 (b7). This pin and PO- are used to set the gain by using external resistors. Connecting this pin to VDD will power down the chip and the PO+ and PO- outputs will be high impedance.
PO-	11	O	This pin is the inverting power amplifier output. Its operation is same as the AXO- (pin-6). In the application, this pin can drive the speaker on the receiver.
PO+	12	O	This pin is the non-inverting power amplifier output. Its operation is the same as the AXO+ (pin-7). In the application, this pin can drive the speaker of the receiver.

4.3. ADPCM/PCM Serial Interface

PIN NAME	PIN NO.	I/O	FUNCTION
MCLK	21	I	This pin is the system master clock input pin. It typically accepts 10.24 MHz for Winbond cordless applications. This pin is the oscillator input.
FST	18	I	This pin is an 8 KHz pulse train for transmission of frame syncs. This pin synchronizes the output of the DT pin (pin-20).
BCLKT	19	I	The bit clock for transmission. It shifts out the data on the DT pin on the rising edge. The frequency may vary from 128K to 2048 KHz.
DT	20	O	This pin is tri-state output data for transmission controlled by FST and BCLKT pin.
FSR	27	I	This pin is an 8K Hz pulse train to receive frame syncs. This pin synchronizes the input of the DR pin (pin-25).
BCLKR	26	I	This pin is the receive bit clock. It shifts data on the DR pin into the chip on the falling edge. The frequency varies from 128K to 2048 KHz.
DR	25	I	This pin is the receive input data controlled by the FSR and BCLKR pins.

4.4. Serial Setup Port(SSP) Interface

PIN NAME	PIN NO.	I/O	FUNCTION
SSP EN	14	I	This pin is the enable signal for SSP setup. This pin is held low to select the16 control and status registers. There are two timing controls. One is for double 8 bit transfer mode; the other control is for the single 16 bit transfer mode. See the timing diagram, Figure 7-6 to 7-9, in Section 7.4.

4.4 Serial Setup Port(SSP) Interface, continued

PIN NAME	PIN NO.	I/O	FUNCTION
SSP CLK	15	I	This pin is the clock for SSP setup. Note that data is shifted out of the SSP on the falling edge of this pin, and shifted into the SSP on the rising edge. The SSP CLK can be any frequency from 0 to 2048 KHz.
SSP TX	16	O	This pin is the tri-state output data for SSP transmission controlled by the SSP CLK pin (pin-15).
SSP RX	17	I	This pin is the receive input data for the SSP controlled by the SSP CLK pin (pin-15).

5. SYSTEM DIAGRAM

5.1 Pair Gain System

Applications for this device include the public switching telephone system. One such application is the pair gain system shown in Figure 5-1. The figure illustrates how the chip is used in a pair gain system to connect the telephone system between end users and the central office terminal These chips are used on devices installed in both the central office terminal (COT) and in the remote office terminal (ROT). If the chip is operating in 32 Kbps ADPCM mode, the COT and ROT must use four chips for 4-channel communication because the U interface chip can support 2B channel, i.e., 128K bps.

In the transmission path, the telephone system first sends the analog signal to the ADPCM chip in the ROT to compress it into a 32 Kbps digital signal. The U interface can then build a 2B+D channel, 128 Kbps, with four ADPCM chip channels, and send the 128 Kbps digital signal to the COT. After receiving the digital signal, the U interface in the COT separates the 128 Kbps data into four ADPCM channels (32 Kbps) and sends this data to the chip to execute the ADPCM decoder and for reconstruction into an analog signal. The analog signal is then sent to the central office (CO) to complete the transmission operation.

For the receive path it is the reverse operation of the transmission path mentioned above.

In a pair gain system, the analog signal (voice signal, or modem signal) is digitized and compressed to a ADPCM signal e.g. 32 Kbps ADPCM. The subscriber loop, the connection between the end user and the central office, is digitized by the U interface transceiver. This provides two B-channels (2×64 Kbps) for data and one D channel for signaling. In short, data can be transmitted and received on the subscriber loop via the U interface transceiver. One B-channel can carry 64 Kbps data, i.e. two 32 Kbps ADPCM channels. Therefore the pair gain system can supply four telephones.

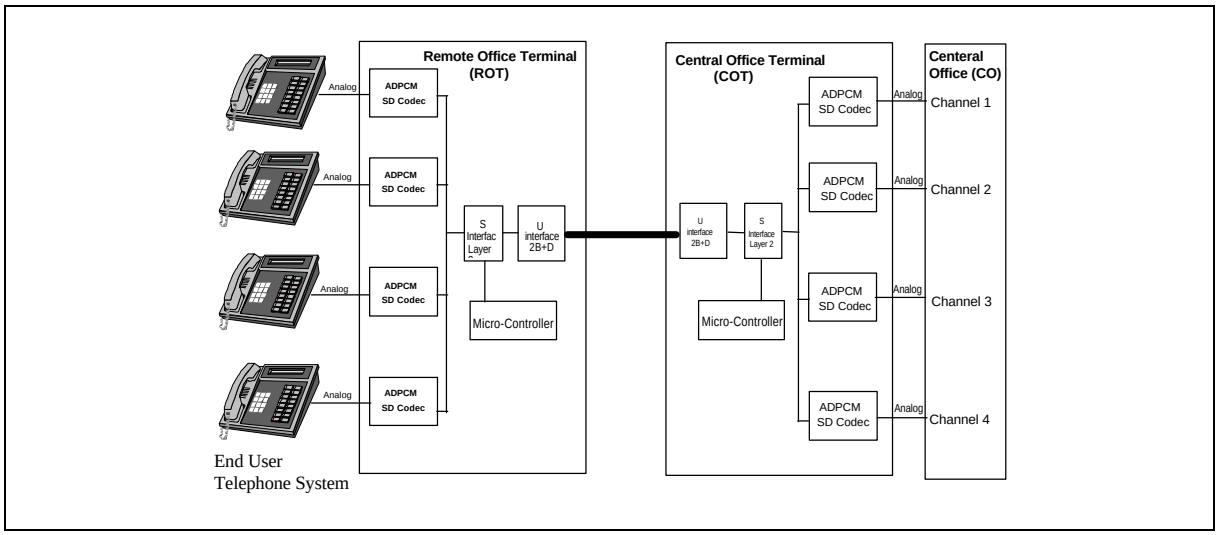

Figure 5-1 System Diagram for Pair Gain Application

5.2. Cordless Phone System

Figure 5-2 shows a cordless phone system block diagram. On the transmission side, the voice is sent to the W9321 ADPCM Codec from the external microphone. First, the analog speech signal is digitized into a 14-bit linear signal and compressed into 32 Kbps ADPCM data. The compressed signal is then sent to the W9330F SST which provides all the baseband functions required for an FCC Part 15 compliant cordless phone. The SST W9330 will generate the spread spectrum binary sequence for output to an RF modulator. The microprocessor manages the other functions of the cordless phone such as the keypad and display control. On the receive side, the WHT9362 RF Module converts the received signal to baseband. The W9330 SST then performs the de-correlation and demoulation and sends the 32K bps speech signal into the W9321 ADPCM. The W9321 then reconstructs the digital speech signal into an analog signal using the 32K ADPCM decoder before sending this analog signal to the speaker.

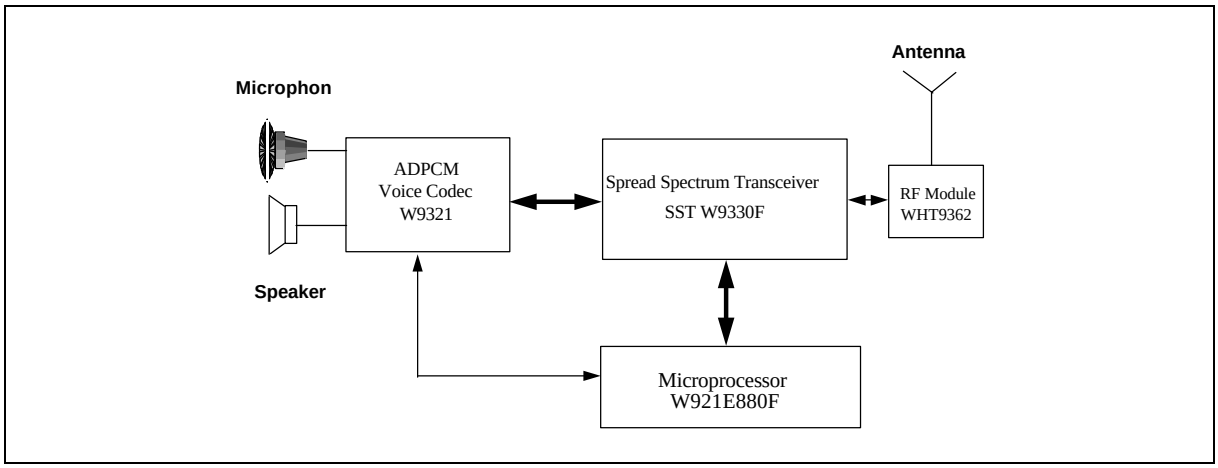

Figure 5-2 System Diagram for Cordless Phone Application

6. BLOCK DIAGRAM

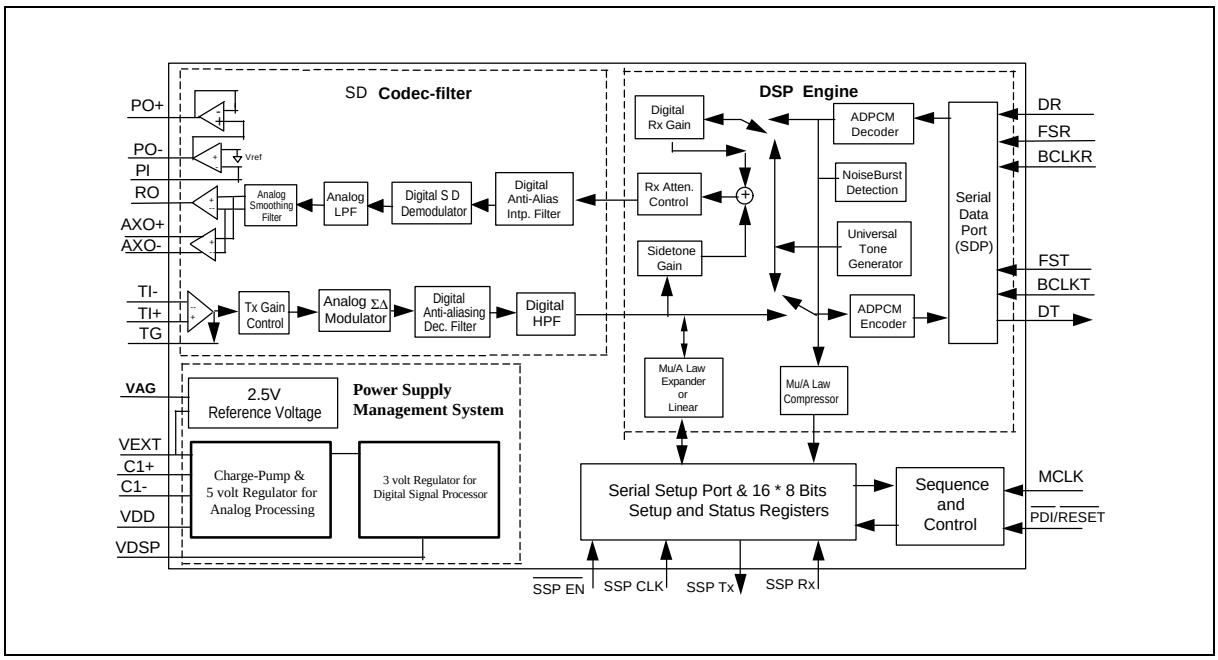

Figure 6-1 Winbond ADPCM ΣΔ Codec Block Diagram

7. FUNCTIONAL DESCRIPTIONS

Figure 6-1 illustrates the functional blocks of the Winbond ADPCM ΣΔ codec. The chip can be divided into four subsystems which are described in the following subsections.

7.1. Power Supply Management System

In this block two groups comprise the power supply management system. One group is a 5-volt power supply system for all analog signal processing. The second group is a 3-volt power supply system for all digital signal processing.

7.1.1. Power Supply for All Analog Signals Processing

All analog circuits except for output power amplifiers AXO and PO are supplied with 5-volt power. This voltage may be applied directly to the V_{DD} pin or by the 5 volt charge pump circuit. Note that the power drivers AXO and PO are powered by the V_{EXT} pin which is the main positive power supply pin.

When V_{EXT} = +5V ±5% (e.g. base station applications) V_{DD} is an input pin and should be connected externally to the V_{EXT} pin. The charge pump capacitor C1+ and C1- should not be used and the BR0[b2] must be set as a logic "1" to disable the charge pump circuit. In this case VEXT and V_{DD} can share the same 0.1 uF decoupling capacitor to V_{SS}.

When V_{EXT} = 2.7 to 5.25 volts (e.g. battery applications) V_{DD} is a 5 volt charge pump circuit output and should not be connected to V_{EXT}. V_{DD} should be decoupled to Vss with a 0.1 µF capacitor. This pin cannot be used for powering external loads.

7.1.2. Power Supply for All Digital Signals Processing

All digital circuits are supplied by the V_{DSP} pin from a 3-volt regulator circuit. This reduces the chip power consumption. Whatever the value on the power supply pin V_{EXT}, range from 2.7 to 5 volts, the digital circuits will always be powered by a 3 volt voltage supply. Note that the V_{DSP} pin should be decoupled to Vss with a 0.1 μF capacitor and that this pin cannot be used for powering external loads.

7.1.3. Reference Voltage Control System

All analog reference voltages such as power amplifier RO, AXO, PO is 2.5 volt or $V_{EXT}/2$ determined by BR2(b7).

7.2. SD Codec-Filter

This device has a built in linear 14-bit PCM codec-filter using ΣΔ technology. There are two paths in the block, a transmit path and a receive path.

7.2.1. Transmit Path in SD Codec-Filter

An analog signal input, from a microphone interface, is passed to three terminal operational amplifiers (TI+, TI-, TG) driving a typical 2 KΩ load externally to amplify the input analog signal. The analog signal can then be set to have further transmission gain from 0 to +7 dB, in 1 dB steps by the transmit gain control block. The gain is programmed through the SSP port in BR1(b2:b0). The ΣΔ modulator block oversamples the analog signal at 1.024 MHz with one bit resolution. The next anti-aliasing decimation filter reduces the sampling frequency from 1.024 MHz (1 bit) to 32 KHz (15 bit). Digital biquad filters perform the decimation from 32K to 8 KHz and CCITT low-pass filtering at 3400 Hz. The digital HPF block performs the high-pass filtering at 300 Hz. In the final step, the 14 bit A/D conversed data is sent by the transmit path to the DSP engine for further signal processing (e.g. by the ADPCM encoder).

7.2.2. Receive Path in SD Codec-Filter

A 14-bit linear digital signal from the Rx Attenuation control block in the DSP engine is first passed to the digital anti-aliasing interpolation filter block. The interpolation block performs the reverse operation of the decimation filter (described above in the transmit path) and the sampling rate will be increased from 8 KHz (14 bits) to 1.024 MHz (14 bits). The digital ΣΔ demodulator will then reduce the 14-bit samples (1.024 MHz) to 1 bit (1.024 MHz). The digital output signal will be passed to a 3400 Hz switched capacitor low-pass filter with sin(x)/x correction and an analog smoothing filter to reduce the spectral components of the switched capacitor filter. Finally, the analog output signal is sent to the power amplifier, RO, which is capable of driving a 2 KΩ load connected to to the VAG pin, and high current analog output driver AXO simultaneously with a 300 Ω differential load.

Note the device provides another power amplifier, PO, connected in a push-pull configuration. The AXO and PO have different circuit configurations for different applications. The AXO is for handset ringer applications, but the PO driver can accommodate large gain ranges by adjusting two external resistors for applications such as driving a telephone line or a handset receiver.

7.3. DSP Engine

This block is the kernel of the ADPCM transcoder and tone generator. There are two paths in this block, a transmit path and a receive path.

7.3.1. Transmit Path in the DSP Engine

A linear 14 bit sample input from the transmit path of the ΣΔ Codec-filter block is sent in three processing directions: sidetone gain process, Mu/A law compressor/Linear, and ADPCM encoder/ tone encoder. In the sidetone gain block, the input sample is fedback to the receive path and is summed with the output of the digital receive gain. The value is kept in the -70 dB to -8.5 dB range by the SSP port in BR1(b6:b4).The A/D output is then saved linearly into BR9(b7:b0) & BR10(b7:b2). The ADPCM encoder/tone encoder provides 16 Kbps, 24 Kbps, or 32 Kbps ADPCM, or 64 Kbps PCM respectively, as determined by the length of the transmit frame sync (pin 18). The length of the frame sync is calculated by the number of falling edges at the BCLKT pin when the transmit frame sync FST pin is high. Because the frame sync clock is 8 KHz, the encode interrupt is performed once every 125 μS.

As a default value the transmit ADPCM will be delayed by two frames after being requested, i.e. if the current frame request is for ADPCM operation, it will be computed in the next frame and the ADPCM result is transmitted in the next two frames. For applications such as the signaling channel of T1 frame structure the delay status can be configured to a total of 6 frames by the SSP port in BR7(b5). The ADPCM output result will be sent to the serial data port (SDP) on the DT pin and the output data rate from 128 KHz to 2048 KHz will be controlled by the serial data port on the BCLKT pin.

In the universal tone generator mode, the input of the ADPCM encoder comes from the output of the universal tone generator, not from the transmit path in the ΣΔ codec-filter. The ADPCM encoder outputs the tone ADPCM signal through pin DT.

7.3.2. Receive Path in DSP Engine

The device receives data from the DR pin via the serial data port (SDP) under the control of the BCLKR and FSR pins. The clock of the receive frame sync FSR is 8 KHz. The ADPCM decoder receives one decode interrupt every 125 μS. The serial data rate in the BCLKR is in the 128 KHz to 2048 KHz range. The input parameter data is sent to the ADPCM decoder which also provides 16 Kbps, 24 Kbps, or 32 Kbps ADPCM or 64 Kbps PCM, is determined by the length of the receive frame sync FSR pin. The length of the frame sync is calculated by the number of falling edges at the BCLKR pin when the receive frame sync FSR pin is high. The ADPCM decoder consists of a sync adjustment operation for the correction of sync. tandem application, except when the receive digital gain is used for a handset application. The digital receive gain is programmed from -12 dB to +12 dB through the SSP port in BR3(b6:b0). In order to prevent noise from influencing the result of the ADPCM decoder, the noise burst detection algorithm can be enabled by setting the BR7(b6) register to detect interfering sounds and to mute the receive path.

The reconstructed linear PCM will be compressed by the Mu/A law compressor block and sent to BR11 (b7:b0) on the SSP port after sync. adjustment in G.726 for CCITT test mode. After the control of digital receive gain, the synthesized PCM data will be added to the feedback signal of the transmit path in the sidetone gain block. The sum value is then passed to the Rx attenuation control block to protect the output driver, RO, from distortion when the amplitude of the synthesis data is too large (e.g. battery applications). The gain of the Rx. attenuation block is programmed through the BR2 (b2:b0) register in the SSP port. A receive attenuation range of from 0 to -7 dB can be programmed in 1 dB steps.

If the device enables the universal tone generator, the function of the ADPCM decoder will be disabled. Different tone types (i.e. tone 1 and tone 2) can be programmed through the BR7, BR4, and BR5 registers in the SSP port. The tone generator can be used to generate DTMF tones, different ringing tones, and call progress tones for handset applications. In telephone line applications, this tone generator can be used for signaling on the line.

7.3.3. Frame Sync. Types

The frame sync operation uses two industrial control types for the transfer of the ADPCM or PCM data words. These two types are the long frame sync and short frame sync.

7.3.3.1. Long Frame Sync

The long frame sync types for various data rates are shown in Figure 7-1 to 7-4. The bit rate for the ADPCM or PCM encoder and decoder is determined by the length of the frame sync pin (FST or FSR). The length of the frame sync is calculated by the number of falling edges at the BCLKT or BCLKR pin when the frame sync FST or FSR pin is high. For example, if the number of the falling edges on the BCLKT or BCLKR pin is equal to 2 when the frame sync is high, this corresponds to the 16 Kbps bit rate for the encoder and decoder of the ADPCM operation. If the number is 8, the device becomes 64 Kbps PCM operation. The device shifts out the data on the DT pin at the BCLKT rising edge and shifts in the data on the DR pin at the BCLKR falling edge. The length of the frame sync may be changed on a frame by frame basis.

7.3.3.2. Short Frame Sync

The short frame sync types for 32 Kbps ADPCM timing is shown in Figure 7-5. The bit rate for this type of frame performs only 32 Kbps ADPCM encoding and decoding. The length of the frame sync is equal to 1. The device shifts out data on the DT pin at the BCLKT rising edge and shifts in data on the DR pin at the BCLKR falling edge. Switching between long frame sync and short frame sync without going through a power down operation is not recommended.

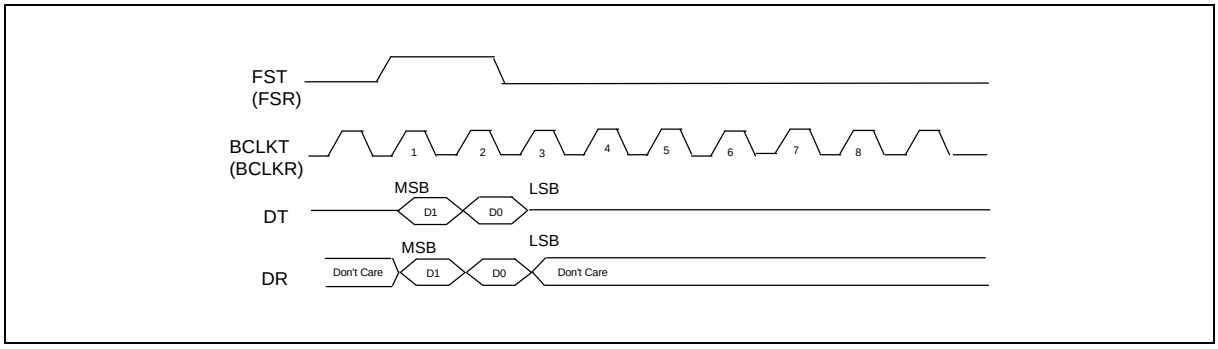

Figure 7-1 Long Frame Sync for 16 Kbps ADPCM Timing

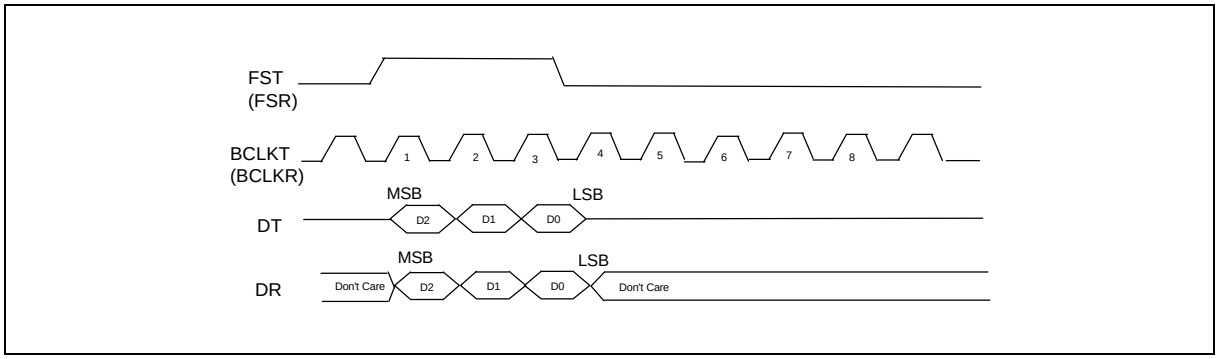

Figure 7-2 Long Frame Sync for 24 Kbps ADPCM Timing

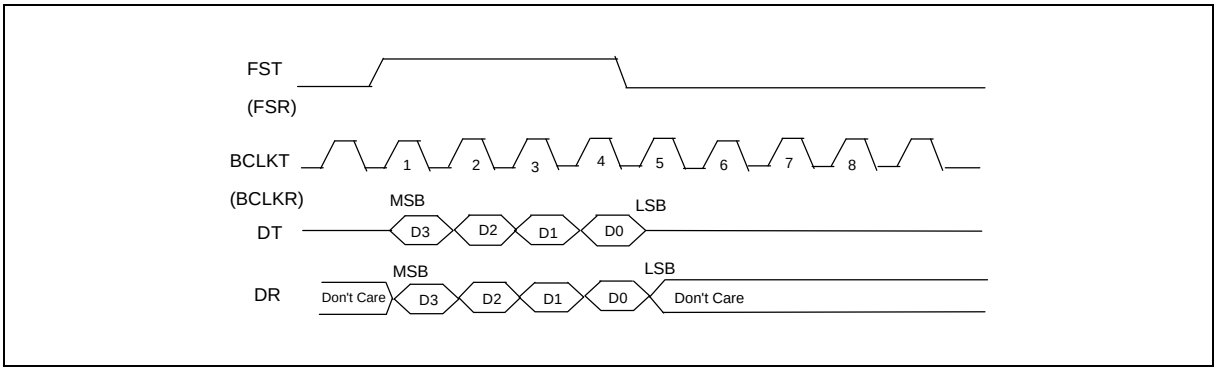

Figure 7-3 Long Frame Sync for 32 Kbps ADPCM Timing

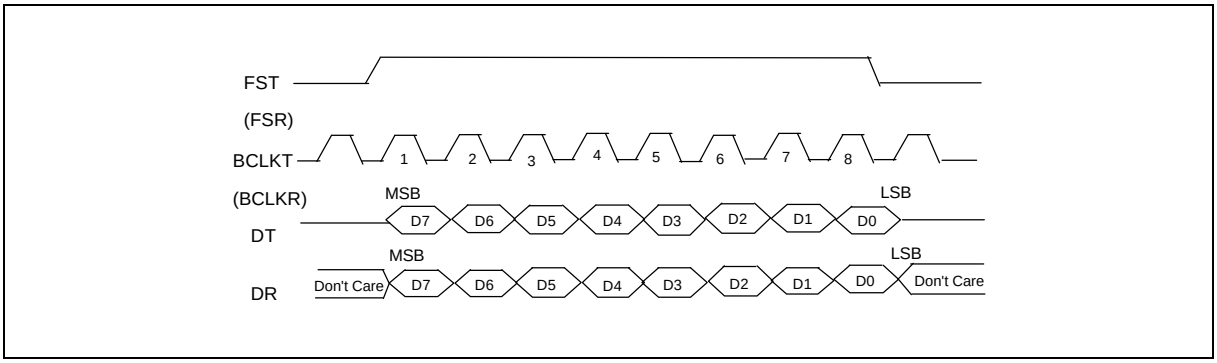

Figure 7-4 Long Frame Sync for 64 Kbps ADPCM Timing

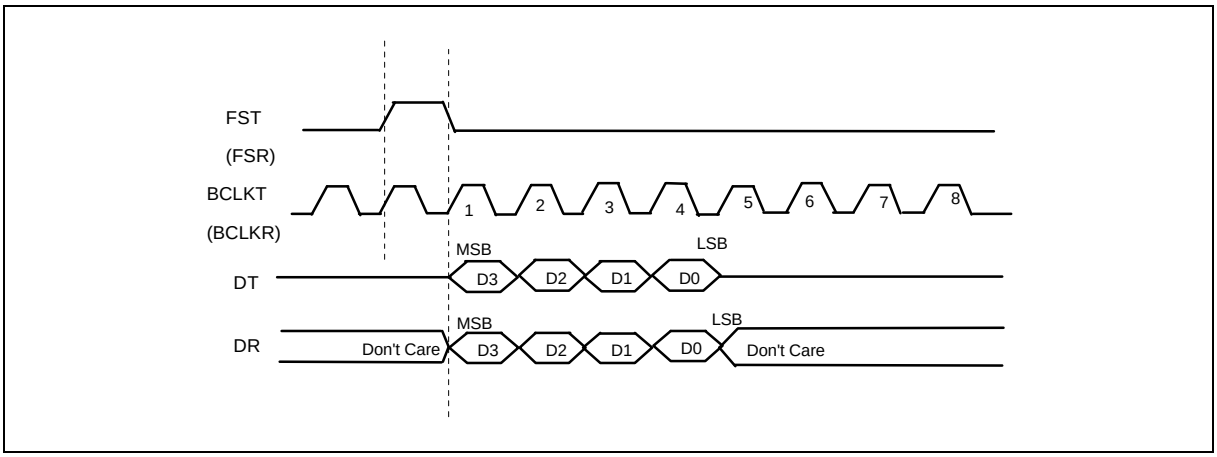

Figure 7-5 Short Frame Sync for 32 Kbps ADPCM Timing

7.4. Serial Setup Port (SSP)

The W9321 has sixteen 8-bit wide setup and status registers, BR0--BR15, for controlling and monitoring functions via the serial setup port (SSP). The SSP may be used by an external microcontroller such as the Winbond W921E880F. The SSP has a full-duplex four wire interface (marked as SSP Tx, SSP Rx, SSP CLK, and SSP EN) for communicating with an external micro-

controller. Two timing controls, a double 8-bit transfer mode and a single 16-bit transfer mode, are available when SSP EN is held low to select the setup registers. The data rate for the SSP CLK ranges from 0 to 2048 KHz. The data is shifted out of the SSP port on the falling edge of SSP CLK, and shifted into the SSP port on the rising edge of the SSP CLK. This latch operation is the reverse of the serial data port in the DSP engine.

The 16 byte registers are selected by bits 3 to 0 in the first byte from the SSP Rx pin as shown in Figure 7-6 to 7-9. Bit 7 of the first byte indicates whether the status is read (logic 1) or write (logic 0). The second byte is the data word (D7:D0). The description of setup and status registers, BR0--BR15 is described in greater detail in the next section 8. (Control and Status Registers).

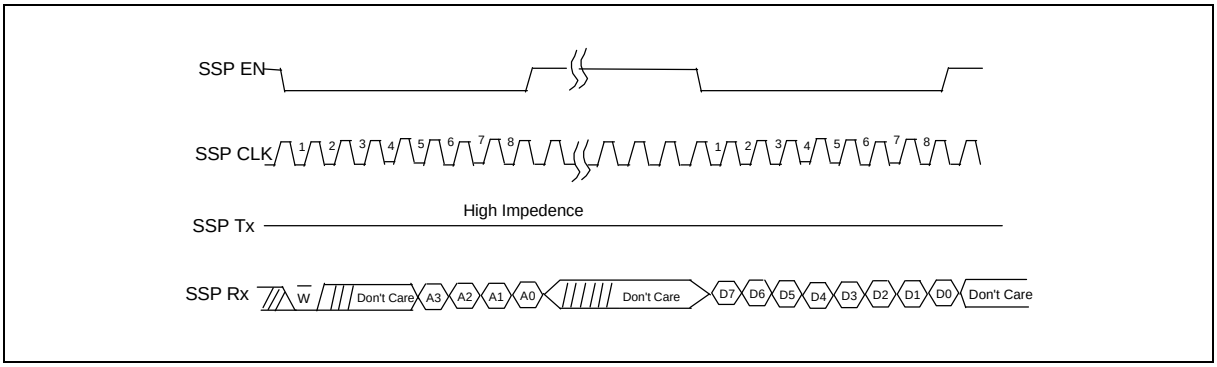

Figure 7-6 Double 8 bit for Write Operation of SSP Register

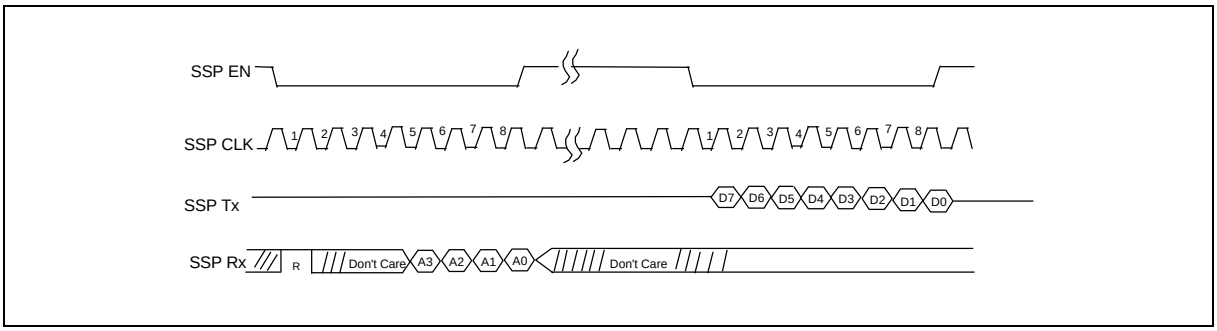

Figure 7-7 Double 8 bit for Read Operation of SSP Register

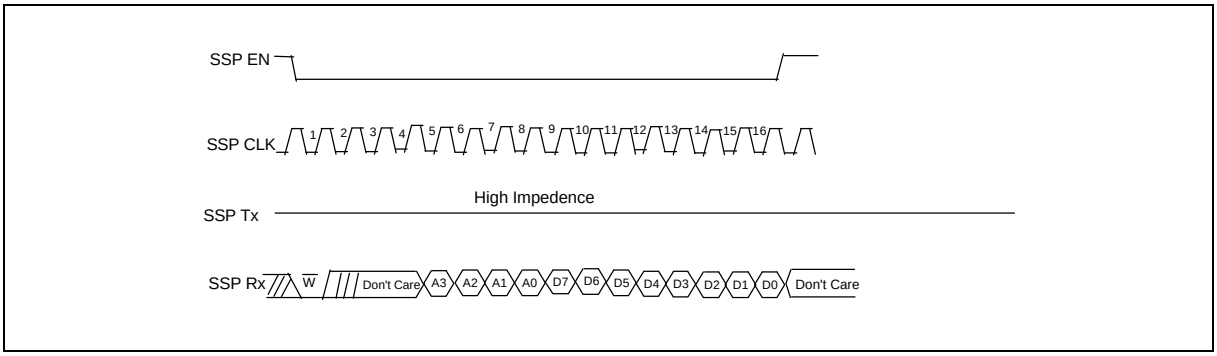

Figure 7-8 Single 16 bit for Write Operation of SSP Register

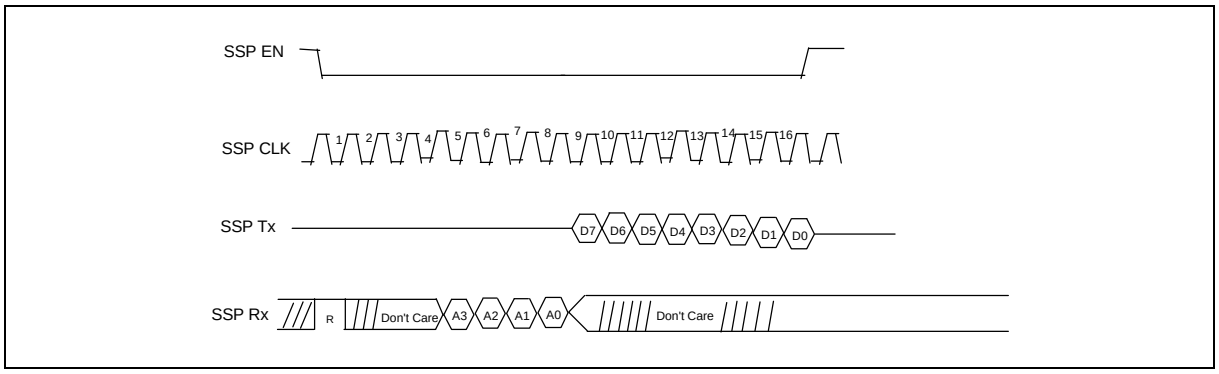

Figure 7-9 Single 16 bit for Read Operation of SSP Register

7.5. Sequence and Control

This block generates some internal clocks, providing clocks such as 1.024 MHz and 8 KHz for ΣΔ codec-filter operation. The master clock MCLK, which supports the clock of the DSP engine, may be asynchronous to all other blocks. Its frequency is typically 10.24 MHz for cordless applications using Winbond chips.

The ΣΔ codec-filter may use the BCLKR pin as a direct 1.024 MHz input. The rising edge of this input clock must be approximately aligned with the rising edge of the FST. This mode requires that the ADPCM transmit and receive be controlled by the BCLKT pin. This is configured by the SSP port through the BR0(b7) register.

There are two ways of forcing the device into a low power consumption condition in power down mode. One way is the hardware power down mode where the PDI/RESET pin is held to logic 0. The other way is the software power down mode where the register BR0(b1:b0) is set through the SSP. When the BR0(b1) setting initiates an analog power down, all clocks for analog signal processing will be halted. To initiate a digital power down, the BR0(b0) register can be programmed to logic 1 to halt all clocks for all digital signal processing. When the chip is powered down, the VAG, TG, RO, PO, AXO, DT and SSP Tx outputs are all high impedance. When the power is reactivated from the power down mode, the ADPCM algorithm is reset to the CCITT initiate state.

7.6. I/O Level

Digital I/O for the device can be programmed in either Mu-law or A-law. Full scale and zero words for these two log-PCM forms are shown in Table 7-1. For analog signal processing, the maximum transmit level is 3.17 dBm0 for Mu-Law or 3.14 dBm0 for A-Law. These values meet the CCITT G.711specifications.

	MU-LAW			A-LAW		
Level	Sign	Segment Bits	Step Bits	Sign	Segment Bits	Step Bits
+ max. scale	1	000	0000	1	010	1010
+Zero	1	111	1111	1	101	0101
- Zero	0	111	1111	0	101	0101
- max. scale	0	000	0000	0	010	1010

Table 7-1 Full Scale and Zero Word for Mu/A-Law

8. CONTROL AND STATUS REGISTERS

8.1. Introduction

There are 16 available byte setup and status registers for the SSP port. The functional description and read/write status of each bit are illustrated in the sections that follow. The read or write status described in Table 8-1 is indicated by the symbol r, w, ro.

SYMBOL	TYPE	MEANING
r/w	Read/Write	Data may be read from the SSP port or written into the SSP port by micro-processor
ro	Read Only	Data may only be read from the SSP port. Writing to this port has no effect.
ro/wo	Read Only/Write Only	Data may be read or written by an external micro-processor and internal chip simultaneously. The value is written into the bit and read back by the external micro-controller

Table 8-1 Read/Write Status Description in SSP Byte Register

8.2. Byte Register Description

There are 16 byte registers for controlling and monitoring the status of the chip. These registers are labeled BR0 to BR15. The descriptions are as follows. Note that "setting" is corresponding to logic "1" and "clearing" is corresponding to logic "0".″.

8.2.1. Byte Register 0 (BR0)

This is a control register. All bits are cleared when the PDI/RESET pin is set to logic zero.

	B7	B6	B5	B4	B3	B2	B1	B0
BR0	Ext 1024 KHz Clock	Mu/A Law Select	Analog Loopback	Function Mode Select[1]	Function Mode Select[0]	Charge Pump Disable	Analog Power Down	Digital Power Down
	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

External 1024 KHz Clock (b7):

This bit controls a mux. When this bit is cleared, the mux selects the 1024 KHz clock from the internal clock generator. When this bit is set, the BCLKR pin is used to provide an external 1024 KHz clock and the internal BCLKR is connected to BCLKT; the BR0[b1] must be set to "1" for reset codec.

Mu/A Law (b6):

When this bit is set to logic zero, the device selects Mu-Law companding of the Log-PCM. Setting this bit selects the A-Law companding of the Log-PCM.

Analog Loopback (b5):

Setting this bit causes an analog loopback from the receive path to the transmit path. Internally the RO output in the receive path is routed to the transmit gain control in the transmit path; the op-amp TG is bypassed.

Mode Select[1:0] (b4:b3):

The function modes are shown in Table 8-2. The ADPCM Codec mode performs a combination of PCM codec and ADPCM transcoder in full duplex. The PCM codec mode is a subset of the ADPCM codec mode, where only the PCM codec is executed. The CCITT test mode uses the CCITT ADPCM test vectors to do conformance testing. Enabling this mode will remove the ΣΔ codec-filter operation. The test vectors go through the SSP port in BR9[b7:b0] and BR10[b7:b0]. See the BR9 and BR10 descriptions for more details. The battery test mode allows testing of the voltage present at the VEXT pin. In this mode, the HPF output in register BR8[b4] must be disabled. Note that the steady linear code for the VEXT pin will be delayed by about 60 samples. The output result of linear 14 bits is stored in registers BR9 and BR10.

FUNCTION MODE SELECT[1:0] (B4:B3)	TYPE
00	ADPCM Codec
01	PCM Codec
10	CCITT Test
11	Battery Test

Table 8-2 Function Mode Selection

Charge Pump Disable (b2):

Setting this bit disables the 5 volt charge pump. In this mode, the charge pump capacitor C1+ and C1- should not be used and the VDD pin should be connected externally to the VEXT pin.

Analog Power Down (b1):

Setting this bit causes an analog power down. In this mode, all clocks for analog processing (e.g. the ΣΔ codec) will be halted to reduce power consumption. The analog circuit will not operate normally until this bit is cleared.

Digital Power Down (b0):

Setting this bit causes a digital power down. In this mode, all clocks for digital processing (e.g. the DSP engine) will be halted to reduce power consumption. The digital circuit and the ADPCM initialization will not operate until this bit is cleared.

8.2.2. Byte Register 1 (BR1)

This register controls the sidetone gain value and transmit gain. This register can also mute the transmit signal. All bits are cleared when the PDI/RESET pin is set to logic zero.

	B7	B6	B5	B4	B3	B2	B1	B0
BR1	Reserved	Sidetone Gain[2]	Sidetone Gain[1]	Sidetone Gain[0]	Transmit Mute	Transmit Gain[2]	Transmit Gain[1]	Transmit Gain[0]
		r/w	r/w	r/w	r/w	r/w	r/w	r/w

Reserved (b7):

This bit is reserved.

Sidetone[2:0] (b6:b4):

These three bits control the sidetone attenuation. The sidetone attenuation can range from -¡Û to -8.5 dB as shown in Table 8-3.

Transmit Mute (b3):

Setting this bit will mute the transmit path in the ΣΔ codec-filter block. A send zero is sent to the DSP engine for further processing.

Transmit Gain (b2:b0):

These three bits control the transmit gain control as shown in Table 8-4. The gain range can be set in the 0 to 6.8 dB range in +1 dB steps.

SIDETONE[2] (B6)	SIDETONE[1] (B5)	SIDETONE[0] (B4)	SIDETONE ATTEN. (DB)
0	0	0	-¡Û
0	0	1	-21.5
0	1	0	-18.0
0	1	1	-15.0
1	0	0	-13.5
1	0	1	-11.5
1	1	0	-10.5
1	1	1	-8.0

Table 8-3 Sidetone Attenuation

TRANSMIT GAIN[2] (B2)	TRANSMIT GAIN[1] (B1)	TRANSMIT GAIN[0] (B0)	TRANSMIT GAIN CONTROL(DB)
0	0	0	0
0	0	1	+1.5
0	1	0	+2
0	1	1	+3
1	0	0	+4
1	0	1	+5
1	1	0	+6
1	1	1	+6.8

Table 8-4 Transmit Gain Control

8.2.3. Byte Register 2 (BR2)

This register controls the operations of the receive path in the ΣΔ code-filter block. All bits are cleared when the PDI/RESET pin is set to logic zero.

	B7	B6	B5	B4	B3	B2	B1	B0
BR2	Reference Point Select r/w	AXO Enable r/w	PO Disable r/w	Reserved	RO Mute r/w	Receive Atten.[2] r/w	Receive Atten.[1] r/w	Receive Atten.[0] r/w

Reference Point Select (b7):

This bit determines the reference voltage for power amplifiers such as RO, AXO, and PO. The output of the VAG pin is the reference voltage. Setting this bit sets the reference voltage to 2.5 volts. When this bit is cleared, the reference voltage is the default value of VEXT/2.

AXO Enable (b6):

This bit determines the status of the power amplifier AXO. Setting the bit will enable the operation of the AXO amplifier. When this bit is cleared, the amplifier AXO will be disabled by default. In power down mode, the output pins of AXO are high impedance.

PO Disable (b5):

This bit determines the status of power amplifier PO. Setting the bit will disable the operation of PO amplifier. When this bit is cleared, the amplifier PO is enabled by default. In the power down mode, the output pins of PO are high impedance.

Reserved (b4):

This bit is reserved.

RO Mute (b3):

Setting this bit will force the input of the RO amplifier to ground. The RO remains offset in order to avoid audible " pops" when turning the block on and off.

Receive Attenuation[2:0] (b2:b0):

These three bits control the receive attenuation as shown in Table 8-5. The attenuation range can be set from 0 to -7 dB in -1 dB steps.

RECEIVE ATTEN.[2] (B2)	RECEIVE ATTEN.[1] B1)	RECEIVE ATTEN.[0] (B0)	RECEIVE ATTENUATION (DB)
0	0	0	0
0	0	1	-1
0	1	0	-2
0	1	1	-3

Continued

RECEIVE ATTEN.[2] (B2)	RECEIVE ATTEN.[1] B1)	RECEIVE ATTEN.[0] (B0)	RECEIVE ATTENUATION (DB)
1	0	0	-4
1	0	1	-5
1	1	0	-6
1	1	1	-7

Table 8-5 Receive Attenuation Control

8.2.4. Byte Register 3 (BR3)

	B7	B6	B5	B4	B3	B2	B1	B0
BR3	Digital Rx Gain Enable r/w	Dig. Rx Gain[6] r/w	Dig. Rx Gain[5] r/w	Dig. Rx Gain[4] r/w	Dig. Rx Gain[3] r/w	Dig. Rx Gain[2] r/w	Dig. Rx Gain[1] r/w	Dig. Rx Gain[0] r/w

This register contains information on the digital receive gain. All bits are cleared when the PDI/RESET pin is set to logic zero.

Digital Rx Gain Enable (b7):

Setting this bit will enable the digital receive gain routine in the DSP engine. The receive gain can be programmed by setting the gain factors defined in this register BR3[B6:B0]. When this bit is cleared, the digital receive gain routine is disabled.

Digital Rx Gain[6:0](b6:b0):

These seven bits show the value of the digital receive gain factor. The gain value is calculated as follows:

2 * b6 + b5+ 1/2 *b4 + 1/4 * b3 + 1/8 *b2 +1/16 *b1 +1/32 * b0

The first two bits (b6:b5) are integers and the last five bits are fractions. The decimal point is placed after bit 5. The gain range can be up to +12 dB.

8.2.5. Byte Register 4 (BR4)

	B7	B6	B5	B4	B3	B2	B1	B0
BR4	TonePar[7] r/w	TonePar[6] r/w	TonePar[5] r/w	TonePar[4] r/w	TonePar[3] r/w	TonePar[2] r/w	TonePar[1] r/w	TonePar[0] r/w

This register holds the parameters for the tone generator. All bits are cleared when the PDI/RESET pin is set to logic zero.

Tone Generator Parameters[7:0](b7:b0):

These seven bits contain the eight LSB frequencies or tone generator attenuation coefficients. The tone generator is enabled when the BR7[b3] register is set to 1. The four MSB tone parameters are placed in BR5[b3:b0]. Switching between the frequency and attenuation factor is determined by the BR5[b7:b6] register.

8.2.6. Byte Register 5 (BR5)

This register holds the parameters for noise burst detection and the tone generator. The noise burst detection and tone generator modes are enabled through the BR7(b3) register. All bits are cleared when the PDI/RESET pin is set to logic zero.

	B7	B6	B5	B4	B3	B2	B1	B0
BR5	NB Thd[7]/ ToneAddr[1] r/w	NB Thd[6]/ ToneAddr[0] r/w	NB Thd[5]/ Don't Care r/w	NB Thd[4]/ Don't Care r/w	NB Thd[3]/ TonePar[11] r/w	NB Thd[2]/ TonePar[10] r/w	NB Thd[1]/ TonePar[9] r/w	NBThd[0]/ TonePar[8] r/w

Noise Burst Detect Threshold[7:0] (b7:b0):

When the device is in the noise burst detection mode (i.e. BR7[b3] = 0 and BR7[b6] = 1) these eight bits contain the threshold for noise burst detection. The detected algorithm use the frequency value to decide whether the noise is present or not. We suggest a threshold value greater than 80 (to be written in decimal format, i.e. 4 KHz above).

Tone Generator Address[1:0](b7:b6):

When the tone generator is enabled, (i.e. BR7[b3] = 1), these two bits can be programmed to select the frequency or attenuation factor as shown in Table 8-6.

Tone Generator Parameters[11:8](b3:b0):

These four bits contain the four MSB frequencies or tone generator attenuation coefficients. The tone generator is enabled when the BR7 (b3) register is set to 1. The last eight LSBs are placed in the BR4[b7:b0] register. Switching between the frequency and attenuation factor is determined by bit 7 and bit 6.

TONE ADDRESS[1] (B7)	TONE ADDRESS[0] (B6)	TONE PARAMETER SELECTION
0	0	Frequency of Tone 1
0	1	Attenuation of Tone 1
1	0	Frequency of Tone 2
1	1	Attenuation of Tone 2

Table 8-6 Tone generator Address Parameters

8.2.7 Byte Register 6 (BR6)

	B7	B6	B5	B4	B3	B2	B1	B0
BR6	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register is reserved. The user should not read or write to this register.

8.2.8. Byte Register 7 (BR7)

This register is used to enable noise burst detection and the tone generator. Additional options include 2/6 frame delay and writing ready status for the BR4 and BR5 registers. All bits are cleared when the PDI/RESET pin is set to logic zero.

	B7	B6	B5	B4	B3	B2	B1	B0
BR7	Ready for BR4 & BR5 ro	NB Detect Enable ro/wo	2/6 Delay r/w	Don't Care	Tone Gen. Enable r/w	Reserved	Tone1 Enable r/w	Tone 2 Enable r/w

Ready for Writing BR4 and BR5 (b7):

This read-only bit indicates whether parameters have been written into the BR4 and BR5 register. This bit is set after writing to BR5. This bit is cleared when the internal DSP Engine reads from the BR4 and BR5 registers.

Noise Burst Detect Enable (b6):

This is a read-only/write-only bit. Setting this bit and bit 3 to 0 enables the noise burst detection routine. If noise is detected, this bit is cleared and can be polled by an external micro-controller. This mutes the receive path.

2/6 Delay (b5):

This bit controls the frame delay status. Setting this bit inserts a 6-frame delay between frame control changes. Clearing this bit inserts a 2-frame delay between frame control changes.

Don't Care (b4):

No effect whenever the bit is read or written to by an external micro-controller.

Tone Generator Enable (b3):

Setting this bit performs the tone generator routine instead of the ADPCM decoder. In addition, the noise burst detection will be disabled. The result of the tone generator will be passed to the ADPCM encoder to compress the tone and transmit the encoded result to the DT pin.

Reserved (b2):

This bit is reserved.

Tone 1 Enable (b1):

Setting this bit enables the tone 1 routine for the tone generator. When this bit is cleared, the tone1 routine is disabled.

Tone 2 Enable (b0):

Setting this bit enables the tone 2 routine for the tone generator. When this bit is cleared, the tone 2 routine is disabled. If DTMF is enabled, the user must set tone 1 and tone 2 to enable.

8.2.9. Byte Register 8 (BR8)

This register contains miscellaneous control bits. All bits are cleared when the PDI/RESET pin is set to logic zero.

	B7	B6	B5	B4	B3	B2	B1	B0
BR8	S/W Encoder Reset r/w	S/W Decoder Reset r/w	Linear Codec Mode r/w	HPF Disable r/w	Reserved	Reserved	Reserved	Reserved

Software Encoder Reset (b7):

Setting this bit forces the device to execute the ADPCM encoder initialization every time the encoder receives an interrupt.

Software Decoder Reset (b6):

Setting this bit forces the device to execute the ADPCM decoder initialization every time the decoder receives an interrupt.

Linear Codec Mode (b5):

Setting this bit forces the device to perform as an 8 bit linear codec. The 6 LSB linear A/D converted output from the ΣΔ codec-filter will be truncated in this mode.

HPF Disable (b4):

Setting this bit will disable the high pass filter (HPF) in the transmit path for applications such as battery test mode in BR0[b4:b3] = "11"″.

Reserved (b3:b0):

These bits are reserved and should not be used by the user.

CAUTION: Reserved bits (b3:b0) must be set to zero at all times for normal operation.

8.2.10. Byte Register 9 (BR9)

	B7	B6	B5	B4	B3	B2	B1	B0
BR9	Tx Log PCM[7]/ Linear PCM[13] ro/wo	Tx Log PCM[6]/ Linear PCM[12] ro/wo	Tx Log PCM[5]/ Linear PCM[11] ro/wo	Tx Log PCM[4]/ Linear PCM[10] ro/wo	Tx Log PCM[3]/ Linear PCM[9] ro/wo	Tx Log PCM[2]/ Linear PCM[8] ro/wo	Tx Log PCM[1]/ Linear PCM[7] ro/wo	Tx Log PCM[0]/ Linear PCM[6] ro/wo

This register contains the PCM value of the transmit path. If the PCM value comes from the transmit path of the ΣΔ codec-filter, then BR9 may be internally written into the most siginificant bits of the 14 bit linear PCM (b13:b6). If the device is for applications such as CCITT test mode i.e. BR0[b4:b3] = "10" then BR9 may read the companding Log-PCM from an external micro-controller to be used for the ADPCM encoder. In the 14 bit linear mode, the 8 MSB are stored into this register and the left 6 LSB will be placed in BR10[b7:b2]. See the description of BR10 for more details. Note that this register is read-only/write-only.

8.2.11. Byte Register 10 (BR10)

	B7	B6	B5	B4	B3	B2	B1	B0
BR10	Encoder Linear PCM[5] ro	Encoder Linear PCM[4] ro	Encoder Linear PCM[3] ro	Encoder Linear PCM[2] ro	Encoder Linear PCM[1] ro	Encoder Linear PCM[0] ro	Reserved	Reserved

This register contains the 6 LSB of the linear PCM value for the transmit path. The PCM value must come from the transmit path of the ΣΔ codec-filter and not from an external micro-controller. The left 8 MSB are stored into BR9[b7:b0]. See the description of BR9 for more details. Note that this register is read-only.

8.2.12. Byte Register 11 (BR11)

	B7	B6	B5	B4	B3	B2	B1	B0
BR11	Rx Log-PCM[7]/ DAC PCM[13] ro	Rx Log-PCM[6]/ DAC PCM[12] ro	Rx Log-PCM[5]/ DAC PCM[11] ro	Rx Log-PCM[4]/ DAC PCM[10] ro	Rx Log-PCM[3]/ DAC PCM[9] ro	Rx Log-PCM[2]/ DAC PCM[8] ro	Rx Log-PCM[1]/ DAC PCM[7] ro	Rx Log-PCM[0]/ DAC PCM[6] ro

This register contains the PCM value of the receive path. The PCM value comes from the companding Log-PCM generated by the sync adjustment block of the decoder in CCITT test mode, i.e. BR0 (b4:b3) is set to logic "10". Note that, this register is read-only. The combined BR11 (b7:b0) and BR12 (b7:b2) value is the same as sending the D/A converter .

8.2.13. Byte Register 12 (BR12)

	B7	B6	B5	B4	B3	B2	B1	B0
BR12	DAC PCM[5] ro	DAC PCM[4] ro	DAC PCM[3] ro	DAC PCM[2] ro	DAC PCM[1] ro	DAC PCM[0] ro	Reserved	Reserved

This register contains the 6 LSB of the linear PCM value for the D/A converter. The PCM value cannot be entered by an external microcontroller. The left 8 MSB are stored into BR11[b7:b0]. See the description of BR11 for more details. Note that this register is read-only.

8.2.14. Byte Register 13 (BR13)

	B7	B6	B5	B4	B3	B2	B1	B0
BR13	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register is reserved and should not be used by the user.

8.2.15. Byte Register 14 (BR14)

	B7	B6	B5	B4	B3	B2	B1	B0
BR14	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register is reserved and should not be used by the user.

8.2.16. Byte Register 15 (BR15)

This register shows the version number of this device.

	B7	B6	B5	B4	B3	B2	B1	B0
BR15	Reserved	Reserved	Reserved	Reserved	Vers.[3] ro	Vers.[2] ro	Vers.[1] ro	Vers.[0] ro

Version[3:0] (b3:b0):

These four bits determine the manufacturing version number of this chip.

9. ELECTRICAL CHARACTERISTICS

9.1. Absolute Maximum Ratings

(Voltage Referenced to VSS pin)

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	VEXT, VDD	-0.3 to 6	V
Analog Input/Output Voltage	---	-0.3 to VDD + 0.3	V
Digital Input/Output Voltage	---	-0.3 to VEXT + 0.3	V
Operating Temperature	TOP	-25 to +85	¢J
Storage Temperature	TSTG	-85 to +85	¢J

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9.2. DC Characteristics

(VSS = 0 volt TOP = -25 to +85° C)

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	VEXT	-----	2.7	3.0	5.25	V
Operating Current	IEXT	MCLK = 10.24 MHz, Charge Pump "N" no load	---	---	20	mA
Power Down Current	IPWDN	MCLK Off	---	---	0.5	mA
Input High Voltage	VIH	All digital input pins	VEXT -0.5	---	-----	V
Input Low Voltage	VIL	All digital input pins	0	----	0.5	V

9.2. DC Characteristics, continued

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Output High Voltage	VOH	DT, SSP Tx	VEXT -0.5	----	-----	V
Output Low Voltage	VOL	DT, SSP Tx	0	---	0.4	V
Input High Current	IIL	VSS ≤ Vin ≤ VEXT	-10	---	+10	uA
Input Low Current	IIH	VSS ≤ Vin ≤ VEXT	-10	---	+10	uA
Input Capacitance	CIN	All digital input pins to VSS	---	---	10	pF

9.3. Analog Transmission Characteristics

(VDD = +5V ±5%, VSS = 0 volt , Top = -25 to +85° C; all analog signal referenced to VAG; 64 Kbps PCM; FST = FSR = 8 KHz; BCLKT = BCLKR = 2.048 MHz; MCLK = 10.24 MHz ; Unless otherwise noted)

9.3.1. Amplitude Response for Analog Transmission Performance

PARAMETER	SYM.	CONDITION	TYP.	TRANSMIT		RECEIVE		UNIT
				MIN.	MAX.	MIN.	MAX.	
Absolute Level	LABS	0 dBm0 = 0 dBm @ 600 Ω	0.776	---	---	---	---	Vrms
Max. Transmit Level	TXMAX	------	1.579	---	---	---	---	Vpk
Frequency Response, Relative to 0 dbm0 @ 1020 Hz	GRTV	15 Hz	----	----	-40	-0.5	0	dB
		50 Hz	----	---	-30	-0.5	0	
		60 Hz	---	---	-26	-0.5	0	
		200 Hz	---	-1.0	-04	-0.5	0	
		300 to 3000 Hz	---	-0.20	+0.15	-0.20	+0.15	
		3300 Hz	---	-0.35	+0.15	-0.35	+0.15	
		3400 Hz	---	-0.8	0	-0.8	0	
		4000 Hz	---	---	-14	---	-14	
		4600 to 100, 000 Hz	---	---	-32	---	-30	
Gain Variation vs. Level Tone (1020 Hz relative to -10 dBm0)	GLT	+3 to -40 dBm0	---	-0.3	+0.3	-0.2	+0.2	dB
		-40 to -50 dBm0	---	-1.0	+1.0	-0.4	+0.4	
		-50 to -55 dBm0	---	-1.6	+1.6	-0.8	+0.8	

9.3.2. Distortion Characteristics for Analog Transmission Performance

PARAMETER	SYM.	CONDITION	TYP.	TRANSMIT		RECEIVE		UNIT
				MIN.	MAX.	MIN.	MAX.	
Absolute Group Delay	DABS	1600 Hz	---	---	440	---	---	µS

9.3.2. Distortion Characteristics for Analog Transmission Performance, continued

PARAMETER	SYM.	CONDITION	TYP.	TRANSMIT		RECEIVE		UNIT
				MIN.	MAX.	MIN.	MAX.	
Group Delay Referenced to 1600 Hz	DRTV	500 to 600 Hz	---	---	210	---	---	µS
		600 to 800 Hz	---	---	130	---	---	
		800 to 1000 Hz	---	---	70	---	---	
		1000 to 1600 Hz	---	---	35	---	---	
		1600 to 2600 Hz	---	---	70	---	---	
		2600 to 2800 Hz	---	---	95	---	---	
		2800 to 3000 Hz	---	---	145	---	---	
Total Distortion vs. Level Tone (1020 Hz, Mu-Law, C-Message)	DLT	+3 dBm0	---	36	---	34	---	dBC
		0 to -30 dBm0	---	36	---	36	---	
		-40 dBm0	---	29	---	30	---	
		-45 dBm0	---	25	---	25	---	

9.3.3. Noise Characteristic for Analog Transmission Performance

PARAMETER	SYM.	CONDITION	TYP.	TRANSMIT		RECEIVE		UNIT
				MIN.	MAX.	MIN.	MAX.	
Idle Channel with Equipment Noise	NIDE	Mu-Law, C-Message	**---**	**---**	19	**---**	+11	dBrn
Spurious Out-of-Band at SPKO (300 to 3400 Hz @ 0 dBm0)	NSPO	4600 to 7600 Hz	---	---	---	---	-30	dB
		7600 to 8400 Hz	---	---	---	---	-40	
		8400 to 100,000 Hz	---	---	---	---	-30	
In-Band Spurious (1020 Hz @ 0 dBm0)	NIBS	300 to 3000 Hz	---	---	-48	---	-48	dB
Crosstalk (1020 Hz @ 0 dBm0)	NCTK	300 to 3000 Hz	---	---	-70	---	-70	dB

9.4. Analog Electrical Characteristics

(OP Amplifer TG, RO; Power Amplifer AXO, PO; V_{DD} = +5V ±5%, Vss = 0V; Top = -25 to +85° C)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset voltage of TG	VOFIN	TI+, TI-	---	---	±25	mV
Input Common Mode Voltage	VCMV	TI+, TI-	1.0	---	V_{DD} -2.0	V
Load Capacitance for RO	CLRO	RO	---	---	100	pF
Load Resistance to VAG for TG, RO	RLD	TG, RO	2	---	---	KΩ
VAG Output Voltage	VAG	to Vss	2.4	2.5	2.6	V

9.4. Analog Electrical Characteristics, continued

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Supply Rejection Ratio (0 to 100 KHz @ 100m Vrms to V_{DD} with C-Message)	PSRRdd	TG	---	40	---	dBC
Load Capacitance for AXO, PO	Clap	AXO- to AXO+; PO- to PO+	---	----	300	pF
Load Resistance differentially for AXO, PO	Rldap	AXO- to AXO+; PO- to PO+	300	---	----	Ω
Input Offset Voltage for PI	Vofpi	ref to VAG	---	----	±25	mV

9.5. Digital Switching Characteristics

9.5.1. Characteristic of Serial Data Port for Long Frame and Short Frame

(V_{EXT} = +2.7 to 5.25V ; V_{SS} = 0V; all digital circuits referenced to V_{SS}; Top = -25 to +85° C, C_L = 150 pF)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Master Clock Frequency	T_{MAST}	MCLK	10.232	10.240	10.247	MHz
Bit Clock Frequency	T_{BCLK}	BCLKT, BCLKR	128	---	2048	KHz
Frame Sync. Frequency	T_{SYNC}	FST, FSR	---	8	- -	KHz
Clock Duty Cycle	D_C	MCLK, BCLKT, BCLKR	45	50	55	%
Rise Time	T_{IR}	All digital input pins	---	---	50	nS
Fall Time	T_{IF}	All digital input pins	---	---	50	nS
Frame Sync. Pulse Width	T_{FSP}	FST, FSR	100	---	---	nS
Transmit Sync. Timing	T_{XS} T_{SX}	BCLKT to FST FST to BCLKT	20 80	--- ---	--- ---	nS
Receive Sync. Timing	T_{RS} T_{SR}	BCLKR to FSR FSR to BCLKR	20 80	--- ---	--- ---	nS
Setup Time for DR Valid	T_{STDR}	-	20	---	---	nS
Hold Time for DR Valid	T_{HDDR}	-	50	---	---	nS
Output Delay Time for DT Valid	T_{DV}	BCLKT to DT	10	---	140	nS
Output Delay Time for DT High Impedance	T_{DHI}	BCLKT to DT	10	---	140	nS

Note: these parameters are shown in Figure 9-1 and 9-2.

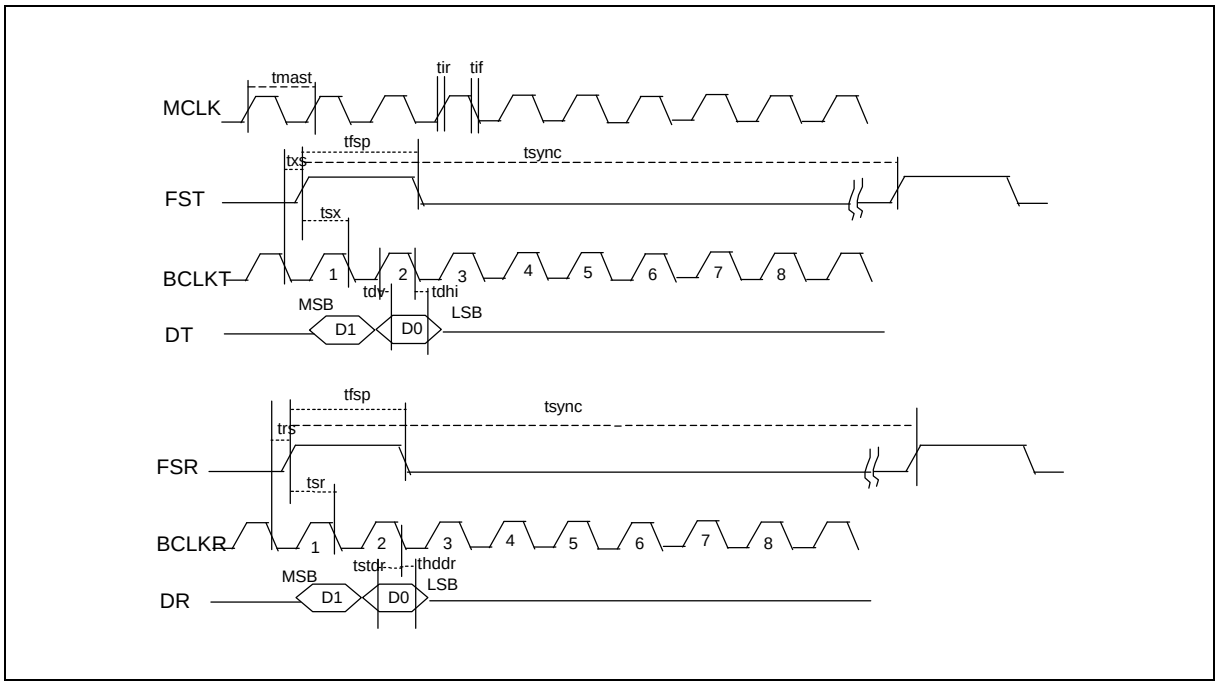

Figure 9-1 Long Frame Sync, Timing

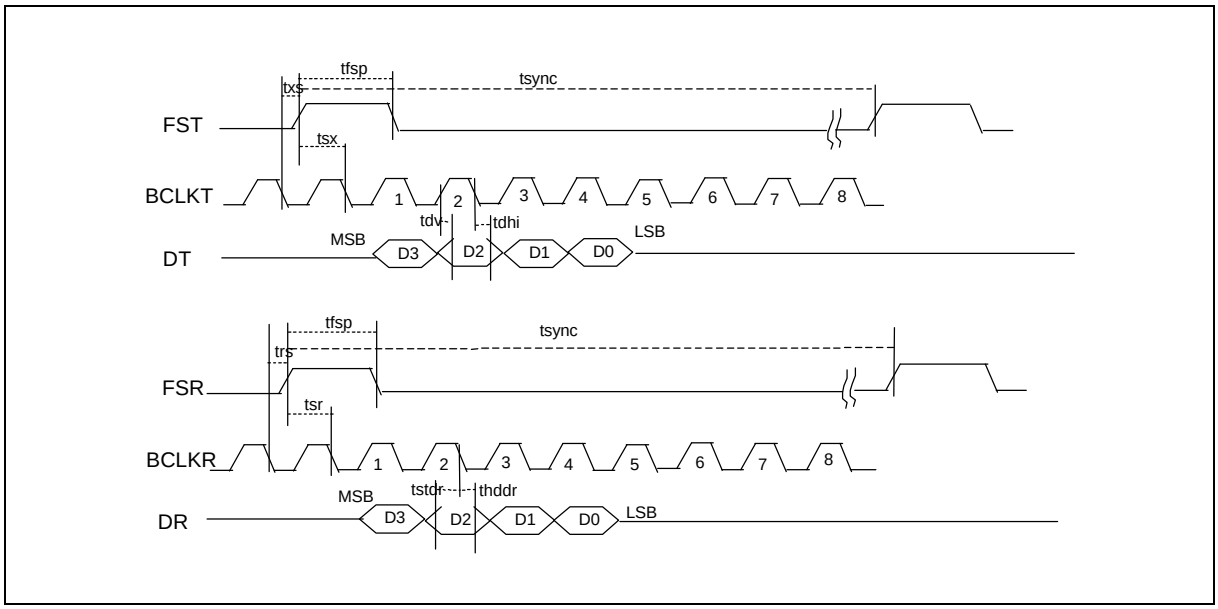

Figure 9-2 Short Frame Sync, Timing

9.5.2. Characteristic of Serial Setup Port (SSP)

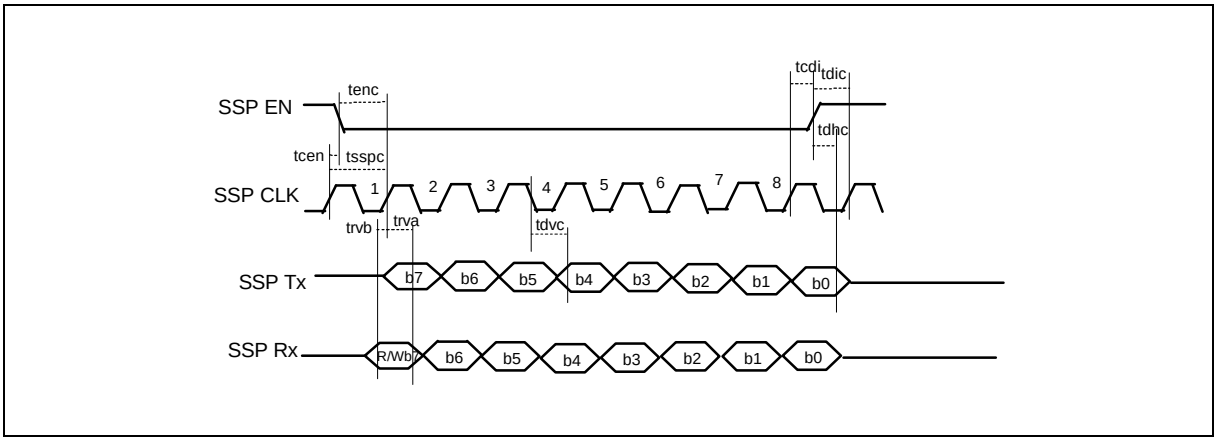

Figure 9-3 Serial Setup Port (SSP) Timing

(V_{EXT} = +2.7 to 5.25V ; Vss = 0V; all Digital Circuit Referenced to V_{SS} ; T_{OP} = -25 to +85° C, C_L = 150 pF)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SSP Clock Frequency	T_{SSPC}	SSP CLK	---	——	2.048	MHz
Clock Duty Cycle of SSP	D_{SSP}	SSP CLK	40	50	60	%
SSP Enable Timing	T_{ENC}	SSPEN to SSP CLK	50	---	---	nS
	T_{CEN}	SSP CLK to SSP EN	50	---	---	
SSP Rx Valid Timing	T_{RVB}	Setup Time	50	---	---	nS
	T_{RVA}	Hold Time	50	---	---	
Output Delay Time for SSP Tx Valid	T_{DVC}	SSP CLK to SSP Tx	---	---	140	nS
Output Delay Time for SSP Tx High Impedance	T_{DHC}	SSP En Rising to SSP Tx	---	---	140	nS
SSP Disable Timing	T_{CDI}	SSP CLK to SSP EN	50	---	---	nS
	T_{DIC}	SSP EN to SSP CLK	50	---	---	

Note: The parameters are shown in Figure 9-3.

10. APPLICATION INFORMATION

10.1. Handset Application for Wireless Communication

For wireless handset applications, V_{EXT} is supplied from a 2.7 to 5.25 volt battery power supply. Meanwhile the V_{DD} pin, connected with a 1.0 µF capacitor to ground, is a 5 volt output and should not be connected to V_{EXT}. The V_{DSP} pin, connected with a 0.1 µF capacitor to ground, is a 3 volt output. The V_{DD} and V_{DSP} pins should not be used to supply any external systems. The chip must also enable the charge pump by clearing the BR0[b2] of SSP port.

The output power amplifier pins PO- and PO+ drive the receiver speaker. A ringer is driven by the differential power amplifier outputs AXO- and AXO+. The input to the transmitter amplifier is from a microphone output.

The application circuit, Figure 10-1 is as follows.

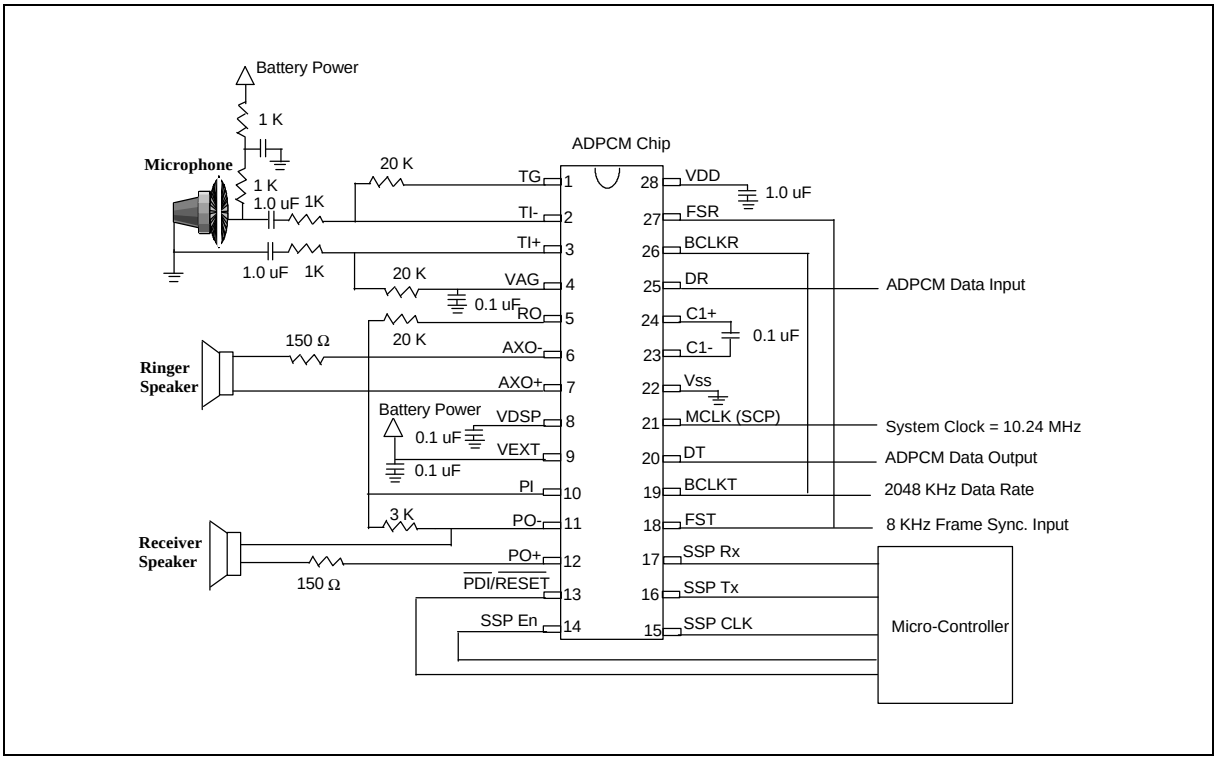

Figure 10-1 Typical Handset Application

10.2. Transformer Application for Public Switching Telephone Network (PSTN)

For this application, V_{EXT} = +5V ±5%, V_{DD} is an input and should be connected to V_{EXT} externally. The charge pump capacitor C1+ and C1- should not be used and the device must disable the charge pump circuit by setting BR0[b2]. Here V_{EXT} and V_{DD} can share the same 0.1 µF capacitor.

The transmitter TI-, TI+ and the receiver PO-, PO+ are connected to the secondary terminal of the telephone line transformer.

The application circuit, Figure 10-2 is as follows.

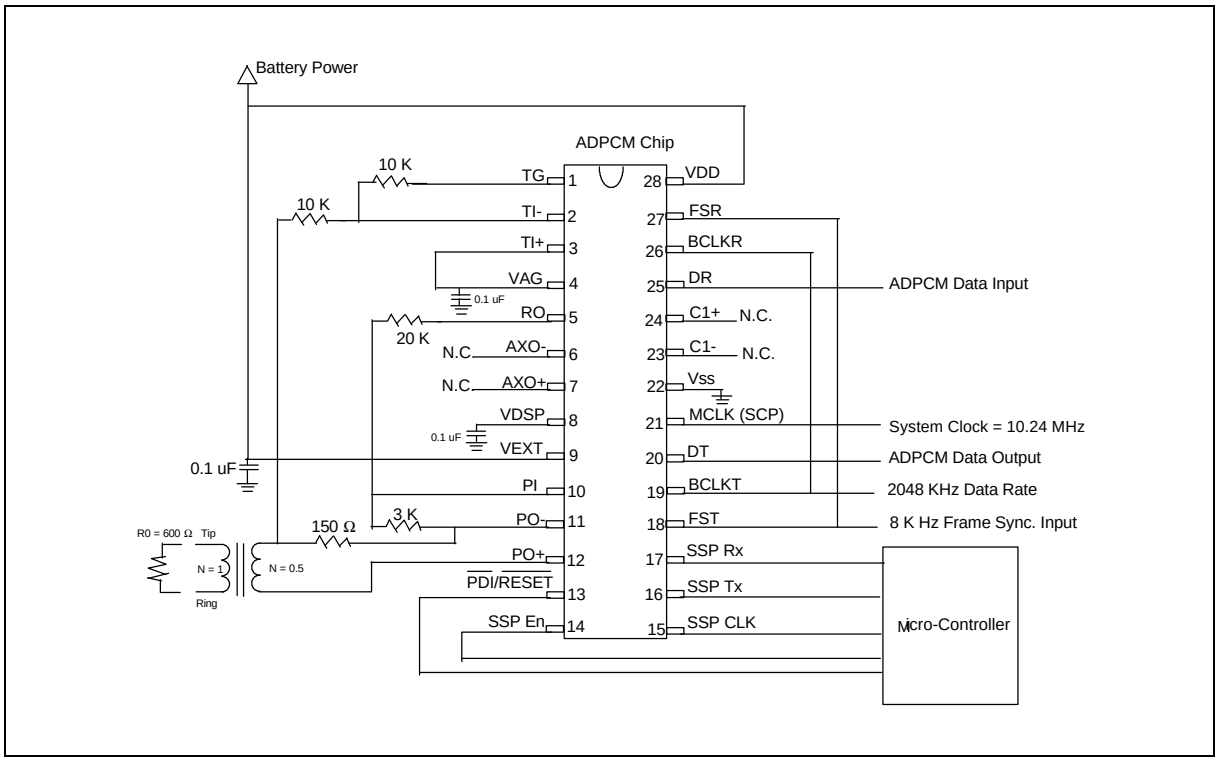

Figure 10-2 Typical Transformer Application

11. HOW TO PROGRAM THE TONE GENERATOR

11.1. Introduction

The chip can enable the tone generator by setting BR7(b3) to logic "1". Under this operation, the ADPCM decoder will be disabled. The tone generator is implemented by the DSP engine based on the function "c" os(nx)″.

The procedure for programming the W9321 tone generator is as follows.

Setting BR7(b3) to logic "1" turns on the tone generator. In addition, BR7(b1:b0) must be set to logic "0" to avoid turning on tone1 or tone2, without first programming the coefficients for freqency and attenuation.

Setup the 12-bit coefficients for freqency and attenuation once every FSR cycle(125 μs). First the 8 least significant bits(LSB) of 12-bit coefficients must be written into BR4(b7:b0); then the 4 most significant bits(MSB) of 12-bit coefficients and address parameter will be written into BR5(b3:b0) and BR5(b7:b6) simultaneously in the same cycle.

Poll BR7(b7) until BR7(b7) becomes a logic "0" before writing another 12-bit coefficent for BR4 and BR5.

Set BR7(b1:b0) to logic "1" selects the tone 1 or tone2 generator.

11.2. Tone Frequency Coefficient Calculation

The tone frequency coefficient is calculated by the function "cos(2*PI*f/8000 radian)" where PI = 3.14159, and f is frequency (Hz). The number will then be converted into a 12-bit coefficient whose MSB is the sign and whose remaining 11 bits are the fractional part found by multiplying by 2048 and rounding off the number. For example, if the frequency is 1209 Hz, the frequency number is as followed.

Cos (2*3.14159*1209/8000) = 0.582053

The converted binary number is 010010101000 and the hex number 4A8, where BR4 = 4 and BR5 = A8.

11.3. Tone Attenuation Coefficient Calculation

The tone attenuation coefficient is calculated by the function "x/1.579 Vp" where x is the amplitude (Vp). The number will be converted into a 12-bit coefficient whose MSB is the sign and whose remaining 11 bits are the fractional part, found by multiplying by 2048 and rounding off the number. For example, if the attenuation is -14 dBm (600 Ω) Hz, first change the dBm units into Vp format as follows.

sqrt[10*exp(-14/10)*600*0.001] * sqrt(2) = 0.218570 Vp

The attenuation is "0.218570/1.579 = 0.138423" the binary number is 000100011011 and the hex number is 11B where BR4 = 1 and BR5 = 1B.

11.4. Frequency Coefficients for the DTMF Signal

Table 11-1 shows the 12-bit frequency coefficients for the DTMF signal. The 8 least significant bits are stored in BR4(b7:b0), the 4 most significant bits are stored in BR5(b3:b0). Table 11-2 illustrates the 12-bit attenuation coefficients for the DTMF signal such as -9 dBm (600 Ω) or -6 dBm (600 Ω) for column tone and -11 dBm (600 Ω) or -8 dBm (600 Ω) for row tone.

FREQENCY (HZ)	BR5 (HEX)	BR4 (HEX)
697	6	D5
770	6	95
852	6	46
941	5	EA
1209	4	A8
1336	3	FC
1477	3	32
1633	2	46

Table 11-1 Frequency Coefficients for the DTMF Signal

ATTENUATION (DBM@600 W)	PEAK VALUE (VP)	BR5 (HEX)	BR4 (HEX)
-11	0.308738	1	90
-9	0.388679	1	F8
-8	0.436105	2	35
-6	0.549023	2	C8

Table 11-2 Attenuation Coefficients for the DTMF Signal

12. PACKAGE DIMENSIONS

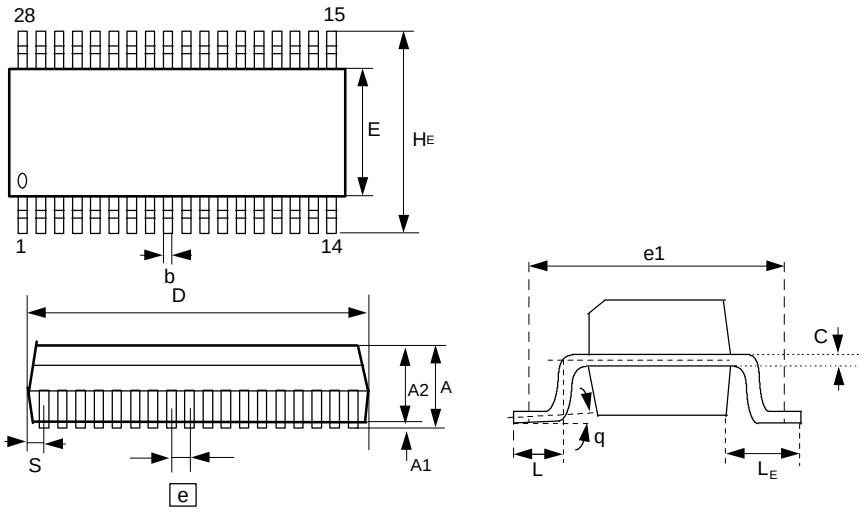

Figure12-1 28-Lead Plastic SOP Package

There are two packages for the W9321. One is a 28-lead plastic SOP shown in Figure 12-1, the other is a 28-lead plastic DIP shown in 12-2.

SYMBOL	DIMENSION IN INCH	DIMENSION IN MM
A	0.110 Max.	2.794 Max.
A1	0.004 Min.	0.102 Min.
A2	0.093 ±0.005	2.362 ±0.127
b	0.016 +0.004 -0.002	0.406 +0.102 -0.051
c	0.010 +0.004 -0.002	0.254 +0.102 -0.051
D	0.705 TYP. (0.725 Max.)	17.90 TYP. (18.415 Max.)
E	0.295 ±0.005	7.493 ±0.127
e	0.050 ±0.006	1.270 ±0.152
e1	0.370 Nom.	9.396 Nom.
HE	0.406 ±0.012	10.312 ±0.305
L	0.036 ±0.006	0.914 ±0.203
LE	0.055 ±0.006	1.397 ±0.203
S	0.043 Max.	0.102 Max.
θ	0–10 degree	0–10 degree

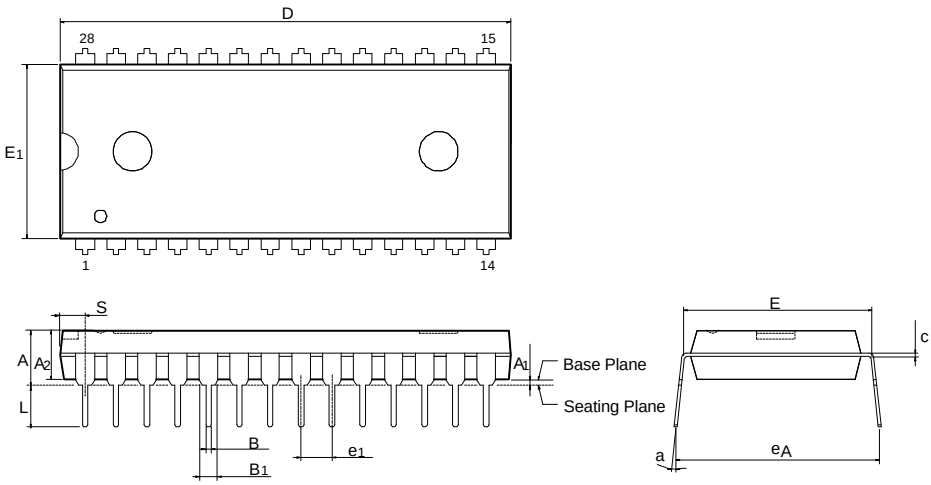

Figure12-2 28-Lead Plastic DIP Package

SYMBOL	DIMENSION IN INCH	DIMENSION IN MM
A	0.210 Max.	5.334 Max.
A1	0.010 Min.	0.254 Min.
A2	0.155 ±0.005	3.937 ±0.127
B	0.018 +0.004 -0.002	0.457 + 0.102 - 0.051
B1	0.06 + 0.004 - 0.002	1.524 +0.102 -0.051
C	0.01 + 0.004 - 0.002	0.254 +0.102 -0.051
D	1.46 TYP. (1.47 Max.)	37.084 TYP. (37.33 Max.)
E	0.6 ±0.01	15.24 ±0.254
E1	0.545 ±0.005	13.843 ±0.127
e1	0.100 ±0.01	2.540 ±0.254
L	0.130 ±0.01	3.302 ±0.254
eA	0.650 ±0.02	16.51 ±0.508
S	0.09 Max.	2.286 Max.
a	0–15 degree	0–15 degree

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