

**SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE**

**DESCRIPTION**

The 2SK2141 is N-channel Power MOS Field Effect Transistor designed for high voltage switching applications.

**FEATURES**

- Low On-state Resistance  
 $R_{DS(on)} = 1.1 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 3.0 \text{ A)}$
- Low  $C_{iss}$   $C_{iss} = 1150 \text{ pF TYP.}$
- High Avalanche Capability Ratings
- Isolated TO-220 (MP-45F) Package

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C)**

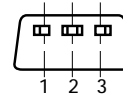
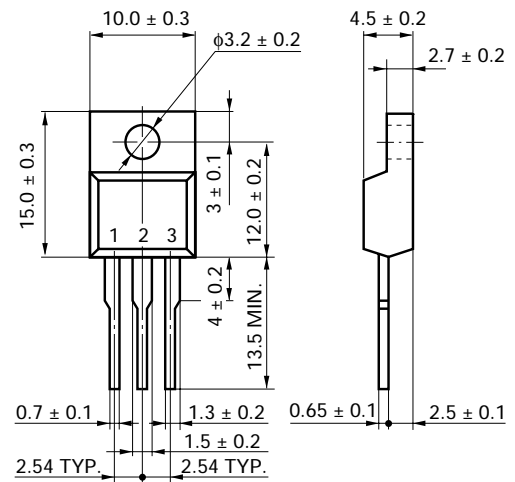
Drain to Source Voltage	$V_{DSS}$	600	V
Gate to Source Voltage	$V_{GS}$	±30	V
Drain Current (DC)	$I_D \text{ (DC)}$	±6.0	A
Drain Current (pulse)	$I_D \text{ (pulse)}^*$	±24	A
Total Power Dissipation (T <sub>c</sub> = 25 °C)	$P_{T1}$	35	W
Total Power Dissipation (T <sub>a</sub> = 25 °C)	$P_{T2}$	2.0	W
Storage Temperature	$T_{stg}$	-55 to +150	°C
Channel Temperature	$T_{ch}$	150	°C
Single Avalanche Current	$I_{AS}^{**}$	6.0	A
Single Avalanche Energy	$E_{AS}^{**}$	12	mJ

\*PW ≤ 10 μs, Duty Cycle ≤ 1%

\*\*Starting T<sub>ch</sub> = 25 °C, R<sub>G</sub> = 25 Ω, V<sub>GS</sub> = 20 V → 0

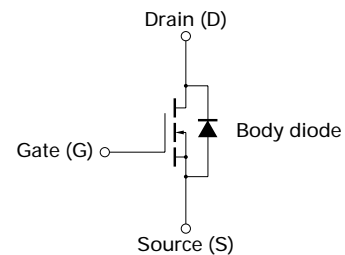
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

**PACKAGE DIMENSIONS  
(in millimeters)**



- 1. Gate
- 2. Drain
- 3. Source

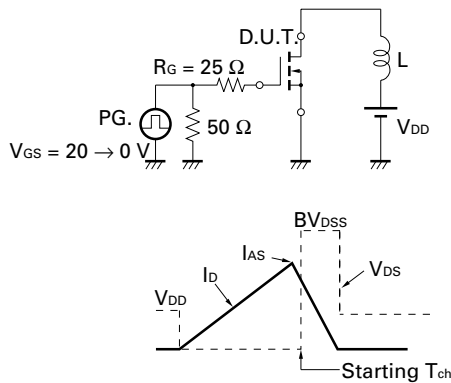
**ISOLATED TO-220 (MP-45F)**



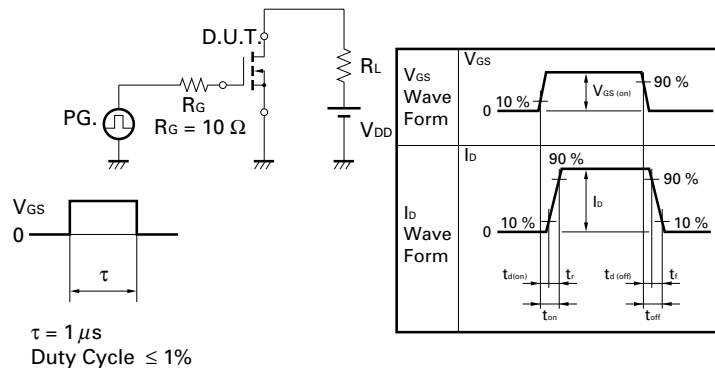
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.8	1.1	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.0 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	2.5		3.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	2.0			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.0 A
Drain Leakage Current	I <sub>DSS</sub>			100	μA	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±100	nA	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		1150		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		260		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		60		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		15		ns	V <sub>GS</sub> = 10 V
Rise Time	t <sub>r</sub>		15		ns	V <sub>DD</sub> = 150 V
Turn-Off Delay Time	t <sub>d(off)</sub>		75		ns	I <sub>D</sub> = 3.0 A, R <sub>G</sub> = 10 Ω
Fall Time	t <sub>f</sub>		13		ns	R <sub>L</sub> = 37.5 Ω
Total Gate Charge	Q <sub>G</sub>		40		nC	V <sub>GS</sub> = 10 V
Gate to Source Charge	Q <sub>GS</sub>		6.0		nC	I <sub>D</sub> = 6.0 A
Gate to Drain Charge	Q <sub>GD</sub>		20		nC	V <sub>DD</sub> = 480 V
Diode Forward Voltage	V <sub>F(S-D)</sub>		1.0		V	I <sub>F</sub> = 6.0 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		370		ns	I <sub>F</sub> = 6.0 A
Reverse Recovery Charge	Q <sub>rr</sub>		1.5		μC	di/dt = 50 A/μs

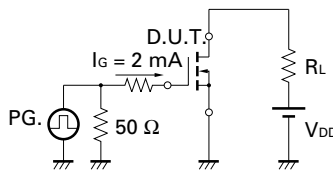
**Test Circuit 1: Avalanche Capability**



**Test Circuit 2: Switching Time**

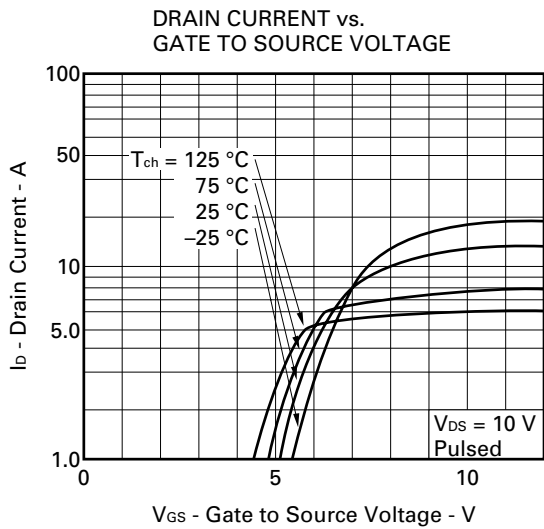
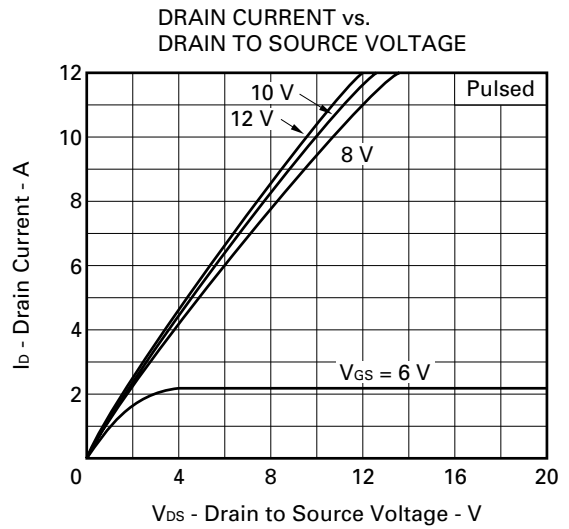
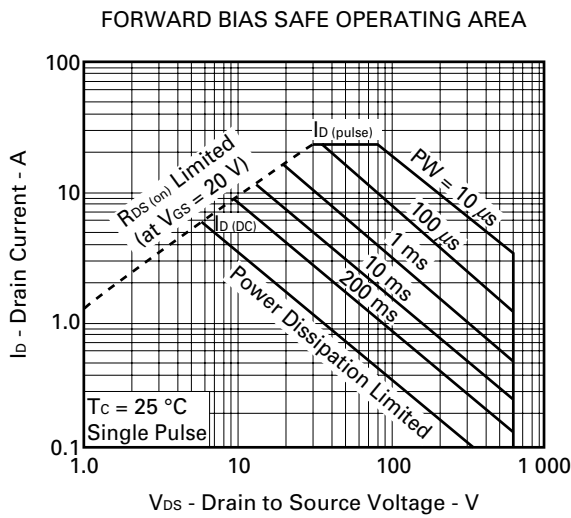
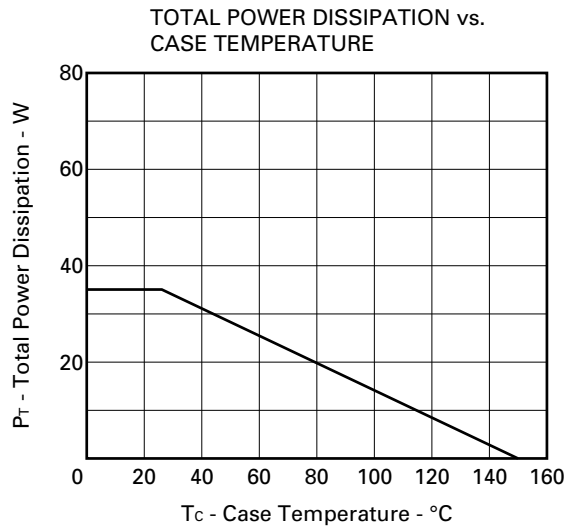
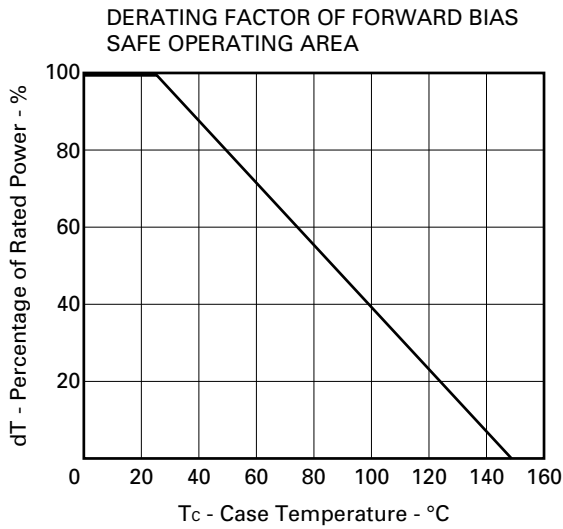


**Test Circuit 3: Gate Charge**

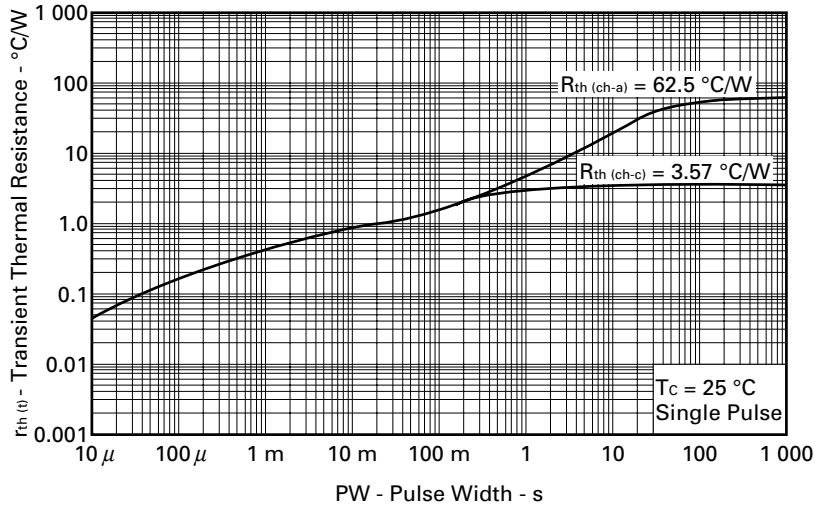


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

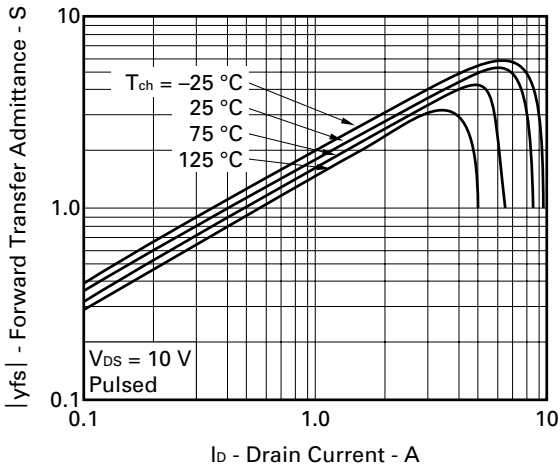
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)



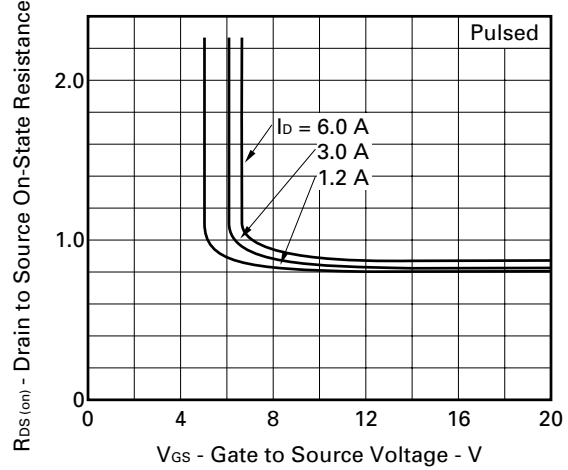
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



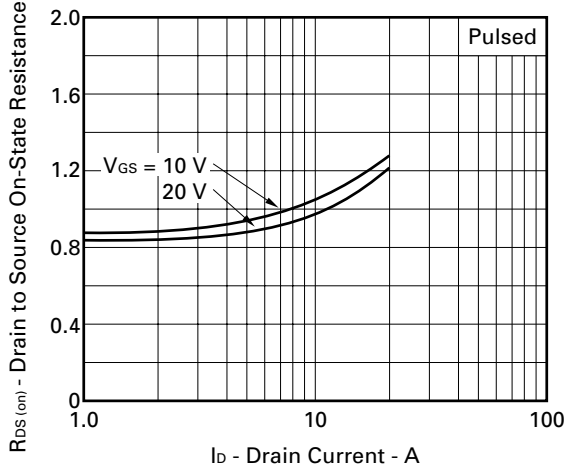
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



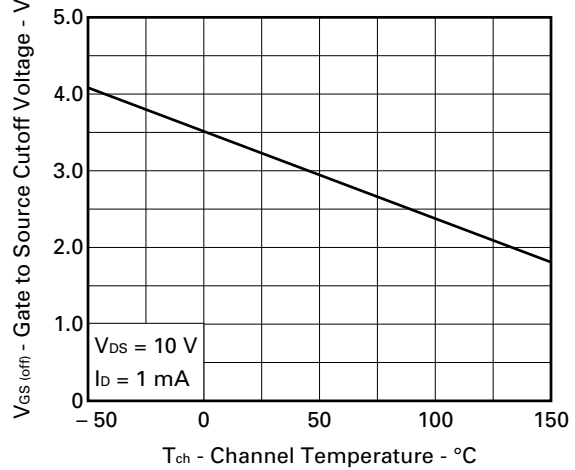
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

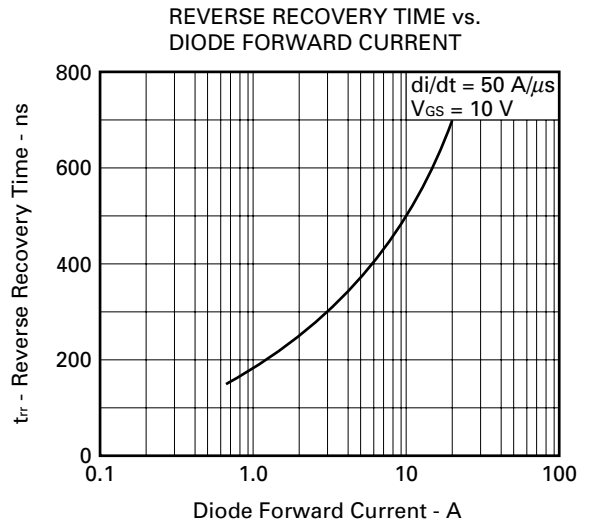
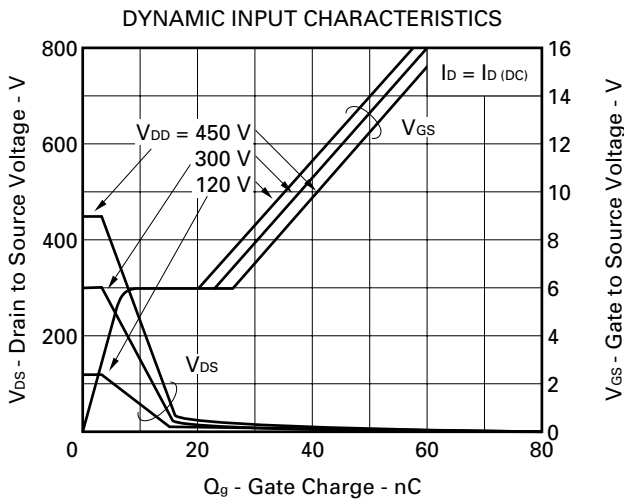
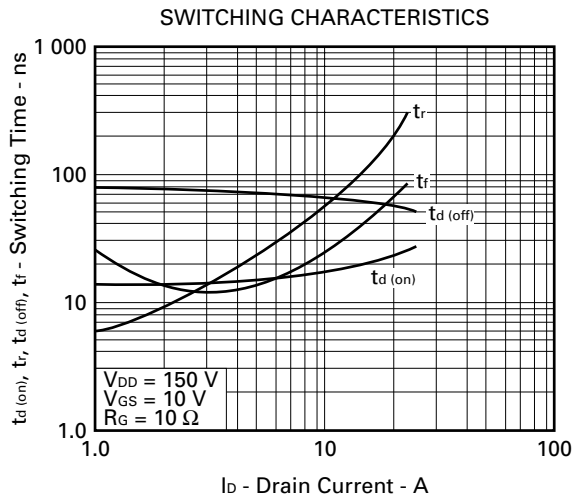
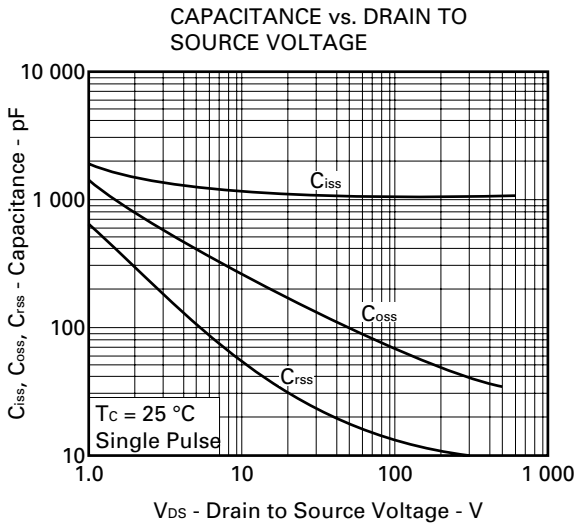
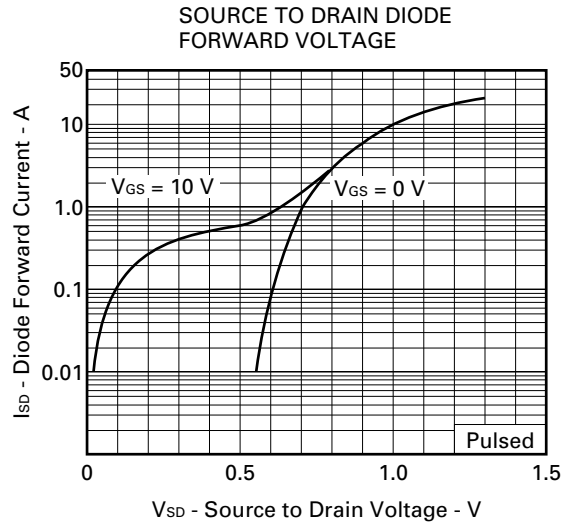
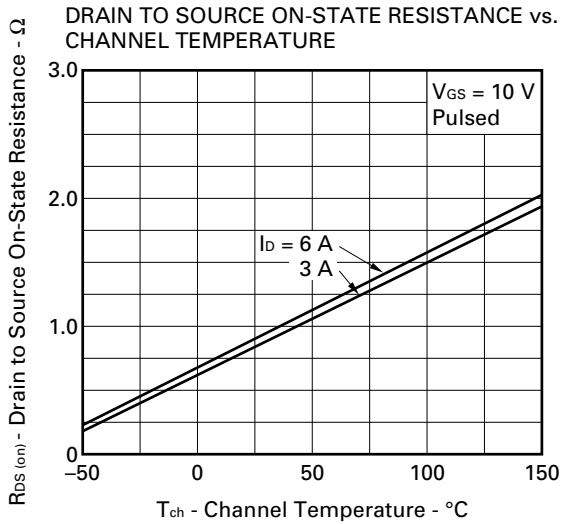


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

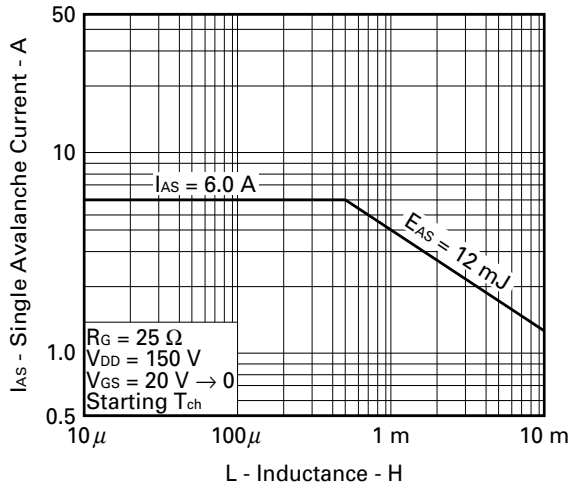


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

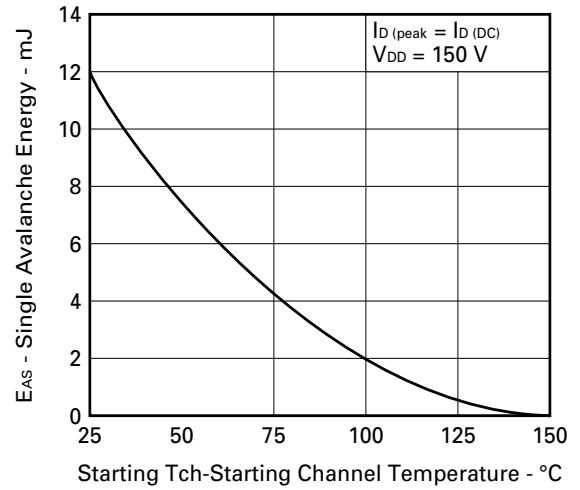




SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



**REFERENCE**

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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