



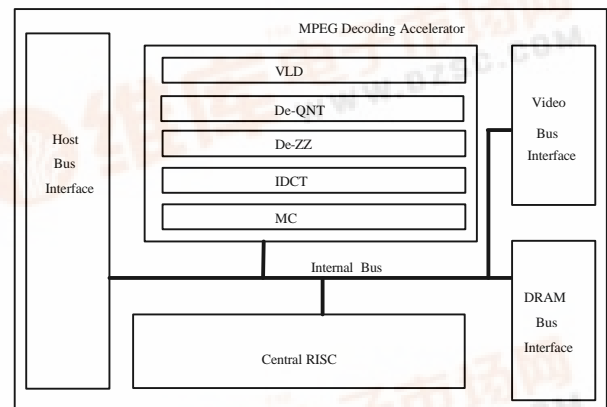
GENERAL DESCRIPTION

The W9920IF MPEG-1 VIDEO DECODER is a high-performance single-chip video decompression processor. It implements the international standard proposed by ISO MPEG (Moving Picture Experts Group) Phase-1 for real-time moving-pictures decompression. The processor is designed for applications that manipulate high-quality digital video with compact storage media such as CD-ROM. The processor not only decompresses MPEG-1 video but also performs some post processing on the decompressed video data. For video output, the processor can deliver the decompressed video sequences either in master-driven mode or slave-driven mode. In master mode, the processor directly displays the decompressed pictures with on-chip generated TV or VGA-like scan timing on a TV screen or a VGA monitor respectively. While in slave mode, the delivery of the decompressed pictures is controlled by an external video clock and synchronization signals.

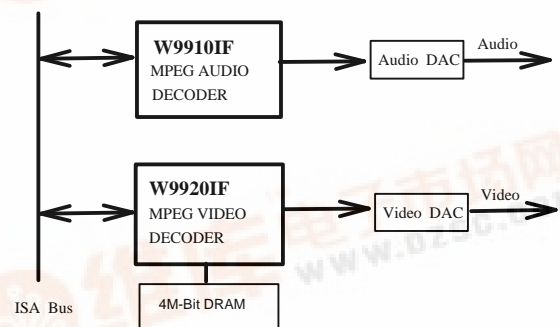
FEATURES

- Supports I/O address setup procedure and on-the-fly I/O address changeable
 - Supports board-level external interrupt sources, general control output pins and address select output pins
 - Requires only one 4Mbits DRAM, even for high resolution still pictures
 - Supports up to 45MHz operating frequency
 - Built-in power down mode
 - Fabricated using Winbond advanced 0.6 um triple-layer metal CMOS technology
 - Packaged in standard 160-pin plastic QFP
- Conforms to ISO/IEC 11172-2 MPEG-1 video standard
 - Fully supports Karaoke CD, Video CD 1.1, Video CD 2.0 and CD-I movie titles
 - Decompresses SIF resolution motion pictures, including 352x240 at 30Hz, 352x288 at 25Hz and 384x240 at 24Hz
 - Decompresses still pictures, including normal resolution of 352x240 or 352x288 and high resolution of 704x480 or 704x576
 - Performs horizontal/vertical interpolation for reducing video artifact
 - Provides clipping function on decompressed pictures
 - Provides either RGB or YCbCr video output
 - Performs frame rate conversion for different display rates regardless of coded frame rate
 - Provides on-chip interlace, non-interlace TV scan timing and VGA-like progressive scan timing generation
 - Supports TV and VGA displays without need of additional line buffers
 - Supports direct frame buffer access, i.e. write or capture pictures through host processor
 - Supports macro play functions
 - Supports on-chip STC for audio/video synchronization
 - Supports 16 bits ISA bus interface

ARCHITECTURE



APPLICATIONS



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