



**W9966CF/TF**

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**Video Camera Interface Controller with Compression**

# **W9966CF/TF**

## **TECHNICAL REFERENCE MANUAL**

**VERSION 1.0**

**NOVEMBER 1997**

## Video Camera Interface Controller with Compression

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**Video Camera Interface Controller with Compression****1 General Description**

The W9966CF/TF is an interface chip offered by Winbond to facilitate adapterless connection between video camera and personal computer, via the industrial IEEE P1284 compatible parallel port. It, along with advanced compression technology, provides high performance solution for video and still image capturing, video e-mail and video conferencing applications.

The W9966CF/TF eliminates the need of traditional capture cards by using the popular SPP/EPP/ECP parallel port for video data transfer to host computers and thus reduce the cost of the video input subsystem while making it easier for users to set up. To cope with the still-limited bandwidth of the parallel port, the W9966CF/TF employs advanced programmable compression technology to reduce the amount of data transferred, and supports a wide range of video quality as required by different application areas. A host-residing software program will decode the compressed video and present it in industrial standard formats (e.g. VFW) to the applications.

The W9966CF/TF provides wide-ranging application-programmable video resolutions and compression ratios. For POTS-based video conferencing application, where the host processor is usually used as the H-protocols CODEC, the mode of QCIF (176x144) resolution with no compression is recommended to save the host processor power from video recovering calculation. For high quality video capturing with high resolution and high frame rate for non-realtime applications such as video e-mail and video editing, the mode of CIF (352x288) with high compression ratio can be used. For high quality snapshot image capturing, modes from QCIF to VGA resolution (640x480) with no compression can be used.

The W9966CF/TF adapts to a variety of CCD modules. It provides a serial bus and general I/O ports as control interface for different CCD chipsets. The input format can be 16-bit YUV 4:2:2 data, or 8-bit digitized CCD raw data from the CCD sensor, which most CCD DSP modules are supporting.

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**Video Camera Interface Controller with Compression****2Features****❑ CCD-module Interface**

- Input data can be in 16-bit YUV 4:2:2 format from the CCD chipset or in 8-bit digitized CCD raw data from the CCD sensor
- Serial bus control for the CCD chipset
- General I/O ports control for different CCD chipsets
- Cropping and down-scaling (1/64 ~ 1) for digital pan and zoom

**❑ Image Data Processing**

- YUV output data can be in YUV 4:2:2 or 4:2:0 format
- Advanced compression algorithms

**❑ PC Interface**

- Supports Plug & Play Device ID using Nibble mode reverse channel transfer
- Supports industrial standard SPP/EPP/ECP interface for register programming
- Supports industrial standard EPP/ECP interface for reverse data transfer to host computer

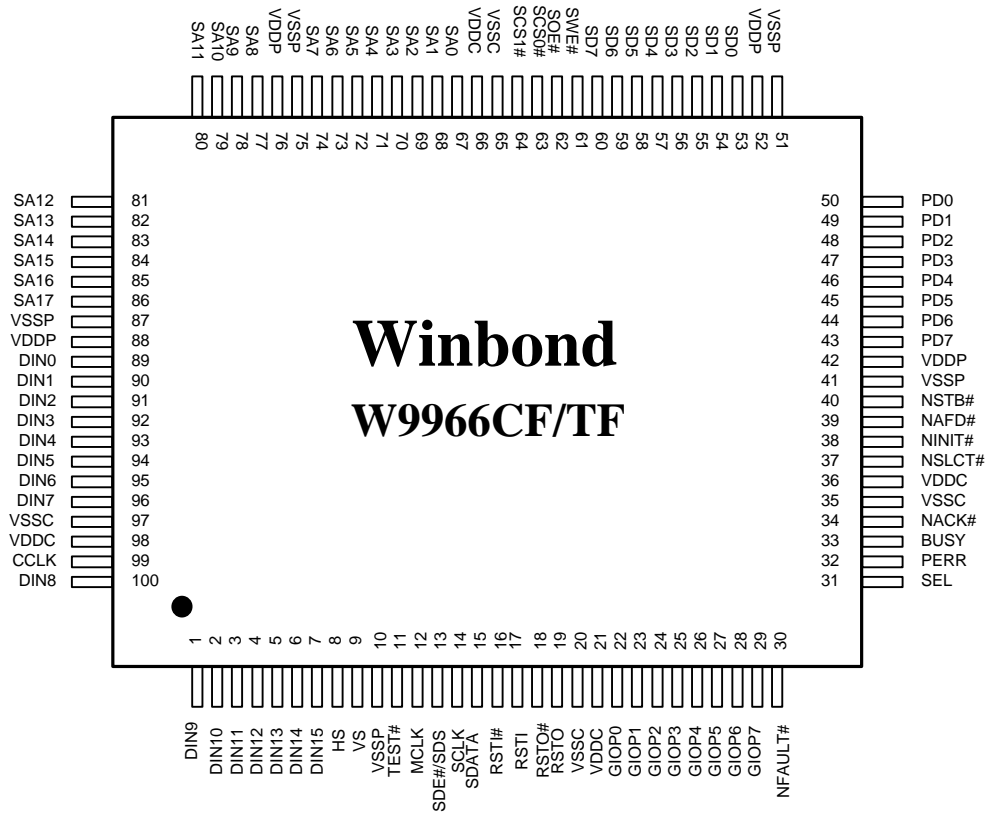
**❑ Programmable Frame Rate**

- 352x288 : 5 - 12 fps or still image capture
- 320x240 : 7 - 15 fps or still image capture
- 176x144 : 23 - 30 fps or still image capture
- 160x120 : 30 fps or still image capture

**❑ 5V CMOS Technology****❑ 100-pin PQFP (W9966CF) and 100-pin TQFP (W9966TF) Package**

## Video Camera Interface Controller with Compression

### 3Pin Configuration



**FIGURE 3.1 W9966CF/TF PIN CONFIGURATION**

**Video Camera Interface Controller with Compression**
**4Pin Description**
**4.1Pin Description**
**TABLE 4.1 SIGNAL TYPE DEFINITION**

SYMBOL	ST INPUT	PULL-up/down	I <sub>OH</sub> (mA)	I <sub>OL</sub> (mA)	DEFINITION
I					Input
IPU		û			Input, Pull-up
IPD		û			Input, Pull-down
IST	û	û			Schmitt Trigger Input, Pull-up
O4			-2	4	4 mA Output
O16			-5	16	16 mA Output
IO4			-2	4	Input, 4 mA Output
IO16		û	-5	16	Input, 16 mA Output, Pull-up
PC					Power/Ground for Core Logic
PP					Power/Ground for Pad Buffer

**CCD-Module Interface**

NAME	NUMBER	TYPE	DESCRIPTION
CCLK	99	I	CCD Data Clock.
HS	8	I	Horizontal Sync.
VS	9	I	Vertical Sync.
DIN15-DIN0	7-1, 100, 96-89	I	CCD Data Input.
SDE#/SDS	13	O4	Serial Data Enable/Serial Data Strobe
SCLK	14	IO4	Serial Interface Clock.
SDATA	15	IO4	Serial Interface Data.

**Memory Interface**

NAME	NUMBER	TYPE	DESCRIPTION
SA17-SA0	86-77, 74-67	O4	Memory Address Bus.
SD7-SD0	60-53	IO4	Memory Data Bus.
SWE#	61	O4	Memory Write Enable.

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SOE#	62	O4	Memory Output Enable.
SCS0#	63	O4	Bank 0 Memory Chip Select.
SCS1#	64	O4	Bank 1 Memory Chip Select.

**PC Interface**

NAME	NUMBER	TYPE	DESCRIPTION
NSTB#	40	IST	Strobe.
NAFD#	39	IST	Auto Line Feed.
NINIT#	38	IST	Initiate.
NSLCT#	37	IST	SelectIn.
NACK#	34	O16	Acknowledge.
BUSY	33	O16	Busy.
PERR	32	O16	Paper Error.
SEL	31	O16	Select
NFAULT#	30	O16	Fault.
PD7-PD0	43-50	IO16	Parallel Port Data Bus.

**Miscellaneous**

NAME	NUMBER	TYPE	DESCRIPTION
MCLK	12	I	Main System Clock Input.
RSTI#	16	IPU	System Reset Input, active low.
RSTI	17	IPD	System Reset Input, active high.
RSTO#	18	O4	System Reset Output, active low.
RSTO	19	O4	System Reset Output, active high.
GIOP7-GIOP0	29-22	IO4	General Purpose I/O.
TEST#	11	IPU	Test Mode Input, active low. When in test mode, GIOP3-GIOP0 are used as test mode select inputs.

**Power and Ground**

NAME	NUMBER	TYPE	DESCRIPTION
VDDP	42,52,76,88	PP	Power for Pad Buffer.
VSSP	10,41,51,75,87	PP	Ground for Pad Buffer.
VDDC	21,36,66,98	PC	Power for Core Logic.



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VSSC	20,35,65,97	PC	Ground for Core Logic.
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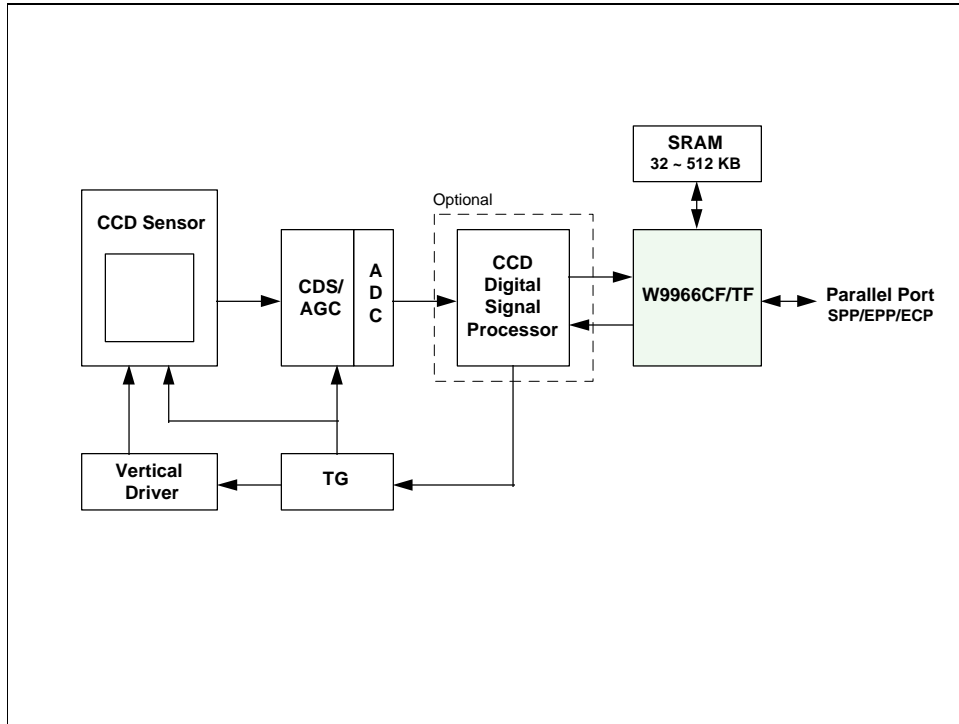
**4.2 Pin List**
**TABLE 4.2 W9966CF/TF PIN LIST**

Number	Name	Number	Name	Number	Name	Number	Name
1	DIN9	26	GIOP4	51	VSSP	76	VDDP
2	DIN10	27	GIOP5	52	VDDP	77	SA8
3	DIN11	28	GIOP6	53	SD0	78	SA9
4	DIN12	29	GIOP7	54	SD1	79	SA10
5	DIN13	30	NFAULT#	55	SD2	80	SA11
6	DIN14	31	SEL	56	SD3	81	SA12
7	DIN15	32	PERR	57	SD4	82	SA13
8	HS	33	BUSY	58	SD5	83	SA14
9	VS	34	NACK#	59	SD6	84	SA15
10	VSSP	35	VSSC	60	SD7	85	SA16
11	TEST#	36	VDDC	61	SWE#	86	SA17
12	MCLK	37	NSLCT#	62	SOE#	87	VSSP
13	SDE#/SDS	38	NINIT#	63	SCS0#	88	VDDP
14	SCLK	39	NAFD#	64	SCS1#	89	DIN0
15	SDATA	40	NSTB#	65	VSSC	90	DIN1
16	RSTI#	41	VSSP	66	VDDC	91	DIN2
17	RSTI	42	VDDP	67	SA0	92	DIN3
18	RSTO#	43	PD7	68	SA1	93	DIN4
19	RSTO	44	PD6	69	SA2	94	DIN5
20	VSSC	45	PD5	70	SA3	95	DIN6
21	VDDC	46	PD4	71	SA4	96	DIN7
22	GIOP0	47	PD3	72	SA5	97	VSSC
23	GIOP1	48	PD2	73	SA6	98	VDDC
24	GIOP2	49	PD1	74	SA7	99	CCLK
25	GIOP3	50	PD0	75	VSSP	100	DIN8

**Note:**

**Video Camera Interface Controller with Compression**

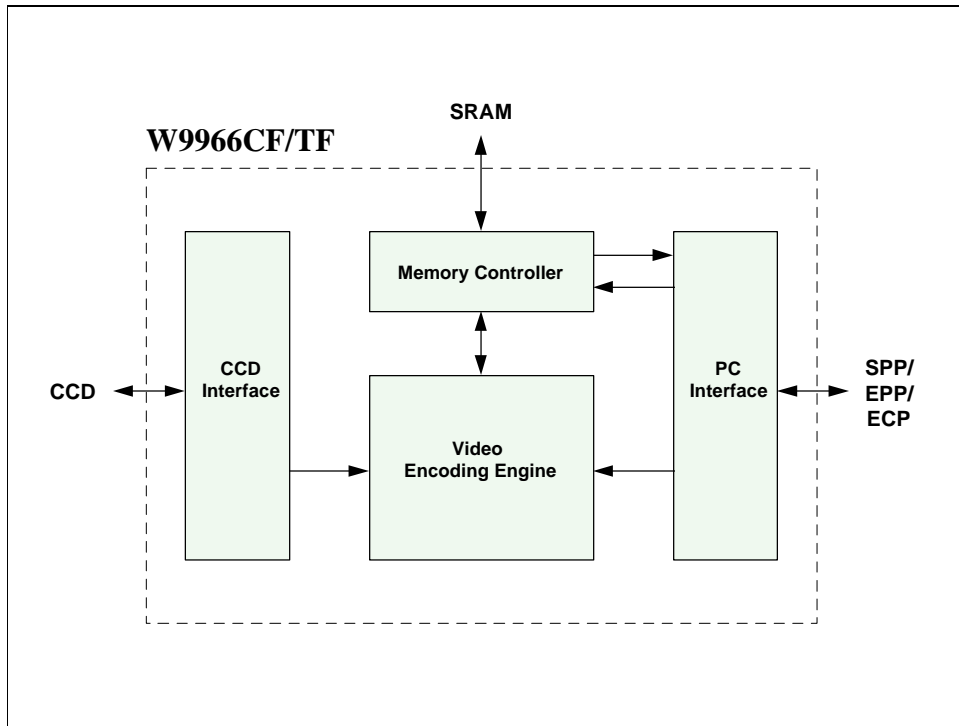
**5 System Diagram**



**FIGURE 5.1 W9966CF/TF SYSTEM DIAGRAM**

**Video Camera Interface Controller with Compression**

**6Block Diagram**



**FIGURE 6.1 W9966CF/TF BLOCK DIAGRAM**

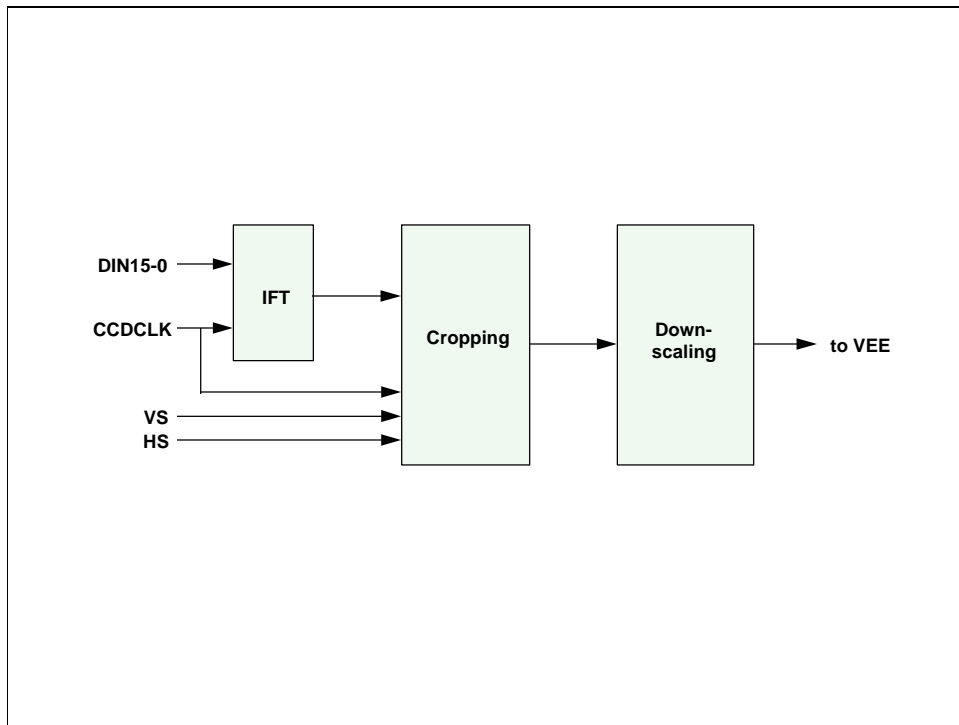
**Video Camera Interface Controller with Compression**

**7 Functional Description**

The block diagram for the W9966CF/TF is shown in Figure 6.1.

**7.1 CCD Interface**

CCD input data is translated, cropped and/or down-scaled in the CCD Interface block, then is sent to the VEE (Video Encoding Engine) block for data encoding. Figure 7.1 shows the functional block diagram for the CCD Interface block.



**FIGURE 7.1 CCD INTERFACE BLOCK DIAGRAM**

**7.1.1 Input Format Translator (IFT)**

The W9966CF/TF accepts CCD data in either 16-bit YUV 4:2:2 format, or in 8-bit digitized CCD raw data format. DIN15-0 are defined as following in either format:

**TABLE 7.1 CCD INPUT PIN DEFINITION**

PIN NAME	16-BIT YUV 4:2:2	8-BIT CCD RAW DATA
DIN15	Y7	Unused
DIN14	Y6	Unused
DIN13	Y5	Unused

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DIN12	Y4	Unused
DIN11	Y3	Unused
DIN10	Y2	Unused
DIN9	Y1	Unused
DIN8	Y0	Unused
DIN7	U7/V7	D7
DIN6	U6/V6	D6
DIN5	U5/V5	D5
DIN4	U4/V4	D4
DIN3	U3/V3	D3
DIN2	U2/V2	D2
DIN1	U1/V1	D1
DIN0	U0/V0	D0

**Note:** in 16-bit YUV 4:2:2 format, chrominance data stream can be either in U01, V01, U23, V23, ... sequence (CR01\_0 = 0), or in V01, U01, V23, U23, ... sequence (CR01\_0 = 1).

**7.1.2 Cropping**

A rectangular cropping window is supported for cropping or clipping the incoming CCD data. Only interested CCD data located inside the cropping window is processed and sent to the host system.

**7.1.3 Down-scaling**

The down-scaling function is performed by dropping pixels for sub-sampling the incoming CCD data. A 6-bit DDA (Digital Differential Accumulator) is used to drop pixels smoothly.

## Video Camera Interface Controller with Compression

### 7.2 Video Encoding Engine (VEE)

The Video Encoding Engine is used to compress or bypass the CCD data, which is then stored in the frame buffer for frame rate adjustment. CCD data may be bypassed or quantized, or compressed in this block, depending on the input/output format, resolution, video quality, and parallel port bandwidth. Two kinds of transfer mode are provided:

**Original Transfer Mode** : CCD data is bypassed or quantized. Normally it is used when input data is CCD raw data (bypass only), or when input data is in YUV 4:2:2 format with low resolution while very high video quality is required. When input data is in YUV 4:2:2 format, the output data stream may be in either YUV4:2:2 or YUV4:2:0 format. The output data stream is in YUV4:2:2 format when the CR13\_2 bit is 0, while it is in YUV4:2:0 format when the CR13\_2 bit is 1.

**Compressed Transfer Mode** : CCD data is compressed using proprietary algorithms. There are two types of pictures used for compression ratio/SNR scalability: base layer and enhancement layer pictures. Most of the compression algorithm is done for the base layer picture, which introduces artifacts and distortions. The coding error picture can be encoded and sent to the host, producing an enhancement layer picture to the decoded base layer picture. The extra data of the enhancement layer picture serves to increase the signal-to-noise ratio (SNR) and also decrease the compression ratio of the input video picture, and hence decrease the term compression ratio/SNR scalability. The output data stream can be in YUV4:2:2 format only, the CR13\_2 bit must be programmed 0.

Figure 7.2 shows functional block diagram for the VEE.

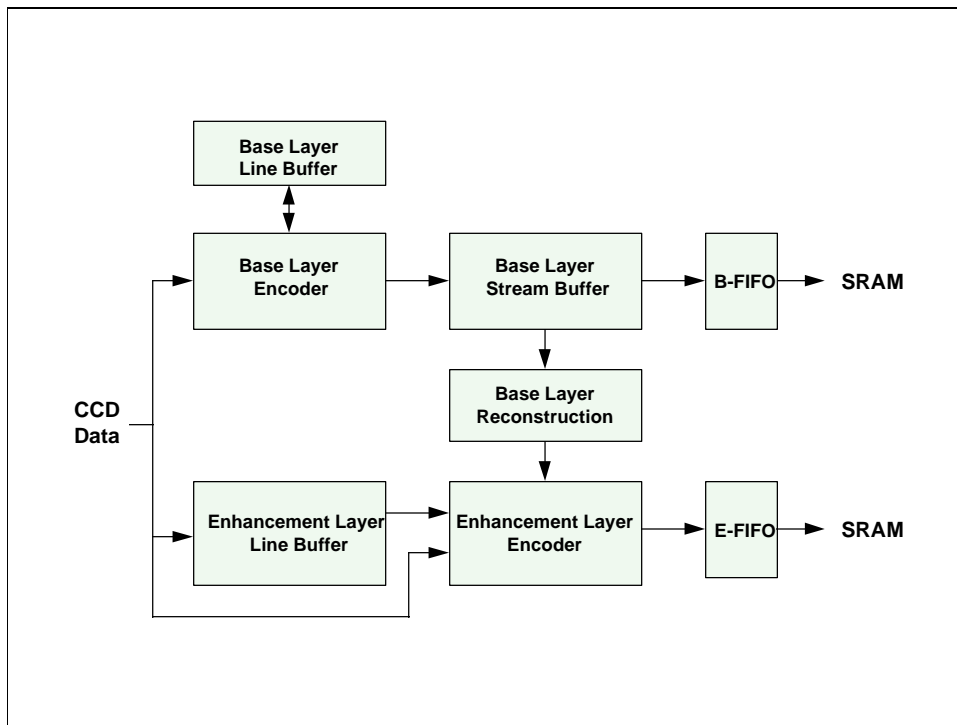


FIGURE 7.2 VIDEO ENCODING ENGINE (VEE) BLOCK DIAGRAM

## **Video Camera Interface Controller with Compression**

### **7.2.1 Base Layer Coding**

The base layer coding is used only when the W9966CF/TF is programmed in the Compressed Transfer Mode. It provides most compression using Winbond's proprietary compression algorithm. A Base Layer Line Buffer is needed to store data of the previous line for reference. The encoded data stream is stored in the frame buffer (SRAM) through the Base Layer Stream Buffer and the B-FIFO. Several lines of the encoded data, stored in the Base Layer Stream Buffer, are needed for the Base Layer Reconstruction, which reconstructs the original image from the encoded base layer data stream.

The base layer coded data stream can be in YUV4:2:2 format only. The CR13\_2 bit must be programmed 0.

### **7.2.2 Enhancement Layer Coding**

The enhancement layer coding is used either in the Original Transfer Mode or in the Compressed Transfer Mode. When the W9966CF/TF is programmed in the Original Transfer Mode, the CCD data, after cropped and down-scaled in the CCD Interface block, is bypassed by the Enhancement Layer Encoder, then is stored in the frame buffer, where it is to be transmitted to the host system via the parallel port.

The Original Transfer Mode output data may be in either YUV4:2:2 or YUV4:2:0 format. The output data stream is in YUV4:2:2 format when the CR13\_2 bit is 0, while it is in YUV4:2:0 format when the CR13\_2 bit is 1.

When the W9966CF/TF is programmed in the Compressed Transfer Mode, the Enhancement Layer Encoding is used to generate an enhancement layer picture to produce an enhancement to the decoded picture. Because base layer compression introduces artifacts and distortions, the difference between a reconstructed picture, generated from the Base Layer Reconstruction, and its original from the Enhancement Layer Line Buffer is a nonzero-valued picture, containing what can be called the coding error. The coding error picture is quantized to generate the enhancement layer picture, which is stored in the frame buffer through the E-FIFO, and then is sent to the host system. Three quantization levels, EyEuEv4:2:2, EyEuEv3:1:1, and EyEuEv2:1:1, are supported and can be selected by programming the CR13\_4-3 bits. EyEuEv4:2:2 level uses 4 bits for Y, 2 bits for U, and 2 bits for V, EyEuEv3:1:1 level uses 3 bits for Y, 1 bit for U, and 1 bit for V, and EyEuEv2:1:1 level uses 2 bits for Y, 1 bit for U, and 1 bit for V. EyEuEv4:2:2 level has the highest quality but with the lowest compression ratio, EyEuEv3:1:1 level has a medium quality and a medium compression ratio, while EyEuEv2:1:1 level has the lowest quality but with the highest compression ratio. A 2-line Enhancement Layer Line Buffer is needed to generate the enhancement layer data stream.

The enhancement layer coded data stream can be in YUV4:2:2 format only. The CR13\_2 bit must be programmed 0.

**Video Camera Interface Controller with Compression**
**7.3PC Interface**

The W9966CF/TF supports industrial standard SPP/EPP/ECP for PC interface. It also supports device ID in Nibble Mode reverse channel transfer. The following interface signals, according to IEEE P1284 standard, are redefined in SPP/EPP/ECP modes:

**TABLE 7.2 PARALLEL PORT REDEFINED SIGNALS**

<b>SIGNAL (DRIVEN)</b>	<b>SPP</b>	<b>EPP</b>	<b>ECP</b>
NSTB# (Host)	nStrobe	nWrite	HostClk
NAFD# (Host)	nAutoFd	nDStrb	HostAck
NINIT# (Host)	nInit	nInit	nReverseRequest
NSLCT# (Host)	nSelectIn	nAStrb	1284 Active
NACK# (Peripheral)	nAck	Intr	PeriphClk
BUSY (Peripheral)	Busy	nWait	PeriphAck
PERR (Peripheral)	PError	User Defined 1	nAckReverse
NFAULT# (Peripheral)	nFault	User Defined 2	nPeriphRequest
SEL (Peripheral)	Select	User Defined 3	Xflag

**Note:** in EPP mode, PERR signal is re-defined as DATA FIFO empty status (active high), NFAULT# signal is re-defined as DATA FIFO full status (active high), and SEL signal is re-defined as DATA FIFO half full status (active high).

**7.3.1Negotiation**

The interface is always initialized to the SPP mode. Host may reinitialize the interface at any time by asserting nInit (NINIT#) low conjunction with nSelectIn (NSLCT#) low. The W9966CF/TF returns to the Compatibility Mode Idle phase after initialization.

A P1284 compliant host negotiates with the W9966CF/TF to verify that the W9966CF/TF is P1284 compliant. Upon the verification the host will request a communication mode for the W9966CF/TF. The W9966CF/TF will acknowledge the request for communication mode based on its capabilities and execute or reject the request as appropriate. This is accomplished by the host placing an extensibility request value on the data bus during the negotiation phase. Table 7.3 shows the communication modes supported by the W9966CF/TF.

**TABLE 7.3 W9966CF/TF COMMUNICATION MODES AND THEIR EXTENSIBILITY REQUEST VALUES**

<b>MODE DEFINITION</b>	<b>EXTENSIBILITY REQUEST VALUE</b>
Request EPP Mode	0100 0000
Request ECP Mode	0001 0000
Request Device ID Using Nibble Mode Rev Chan Transfer	0000 0100



## Video Camera Interface Controller with Compression

### 7.3.2 Device ID

The Device ID is a length field followed by a string of ASCII characters defining W9966CF/TF characteristics and capabilities. The Device ID will be sent from the W9966CF/TF to the host using the Nibble Mode, which is required by the P1284.

The W9966CF/TF Device ID contains four keys: MANUFACTURER, MODEL, CLASS, and DESCRIPTION. Currently implemented ID string is shown below, which may be modified depending on individual vendor's need.

```
x'00', x'60',
MFG:Winbond;
MDL:SA5459;
CLS:DIGCAM;
DES:Winbond's DIGCAM driver can not be found in the system;
```

### 7.3.3 Device Addressing

The bi-directional SPP/EPP/ECP protocol describes two basic types of 8-bit information transfers: data read/write operations and address read/write operations. Table 7.4 specifies the control signals used by each mode to perform address/data cycle and to indicate reverse data flow.

**TABLE 7.4 PARALLEL PORT READ/WRITE SIGNALS**

SIGNAL	SPP	EPP	ECP
Address Strobe	NSTB (NAFD=0)	NSLCT	NSTB (NAFD=0)
Data Strobe	NSTB (NAFD=1)	NAFD	NSTB (NAFD=1)
Reverse Channel	Not supported	Implicit	NINIT=0

An address write cycle is used to select the W9966CF/TF's address mode for subsequent data cycles. Figure 7.3 defines the data bits of this parallel port data path during an address write operation to the W9966CF/TF.

Three kinds of output format are provided:

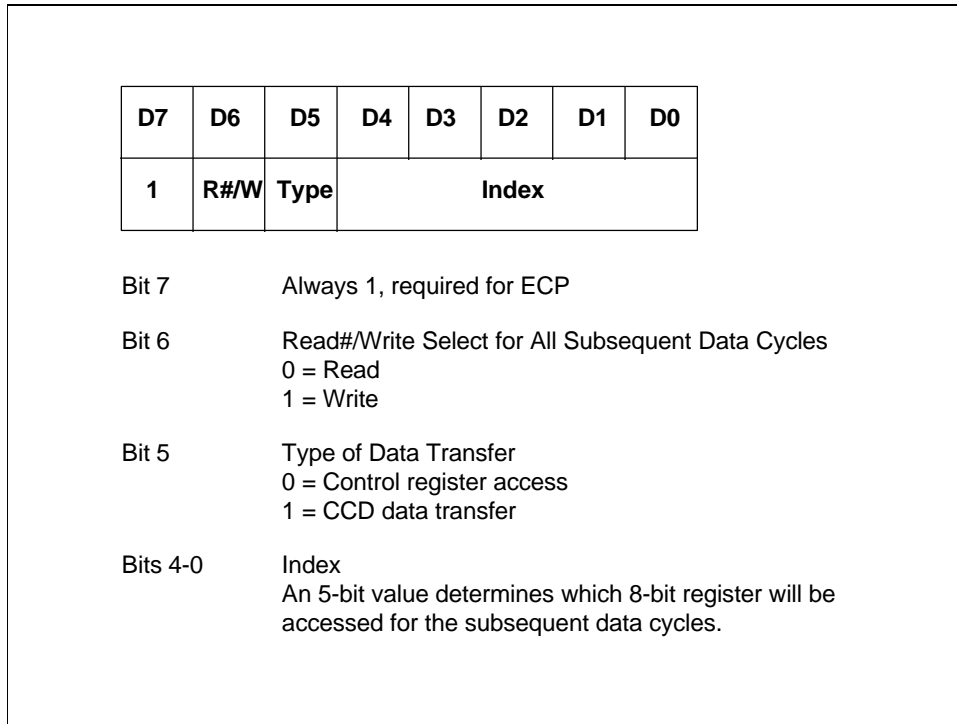
**CCD Raw Data** : used only when input data is the CCD raw data (CR01\_1 = 0).

**YUV 4:2:2** : used when input data is in 16-bit YUV 4:2:2 format (CR01\_1 = 1).

**YUV 4:2:0** : used when input data is in 16-bit YUV 4:2:2 format (CR01\_1 = 1).

CCD Raw Data format is supported only in the Original Transfer Mode, while YUV 4:2:2 and YUV 4:2:0 formats are both supported in either Original Transfer Mode or Compressed Transfer Mode.

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**FIGURE 7.3 PARALLEL PORT ADDRESS REGISTER DEFINITION**

**7.3.4 Control Register Data Write**

The desired control register data write operation is performed by :

1. using an address write cycle with data bits 7-5 = 110, and bits 4-0 = index of the desired register.
2. Write data to the desired register by performing a data write cycle.

**7.3.5 Control Register Data Read**

The desired control register data read operation is performed by :

1. using an address write cycle with data bits 7-5 = 100, and bits 4-0 = index of the desired register.
2. The W9966CF/TF performs an reverse data transfer phase for the desired register data transfer.

**7.3.6 CCD Data Transfer (Peripheral to Host Only)**

The CCD data transfer is performed by :

1. using an address write cycle with data bits 7-5 = 101, and bits 4-0 = XXXXX.

**Video Camera Interface Controller with Compression**

2. The W9966CF/TF performs reverse data transfer phase if DATA FIFO is not empty.

## Video Camera Interface Controller with Compression

### 7.4 Memory Controller

A frame buffer (SRAM) is needed to buffer the real-time CCD data for frame rate adjustment. The Memory Controller is designed to arbitrate memory requests from the CCD and the host, and to generate all SRAM control signals.

#### 7.4.1 Memory Size and Estimated Performance

Table 7.5 shows the memory size needed and the estimated performance for various picture formats. The performance is estimated based on the assumption of 1.2 Mbytes/s ECP bandwidth.

**TABLE 7.5 MEMORY SIZE AND ESTIMATED PERFORMANCE**

PICTURE FORMAT	SRAM	PERFORMANCE (fps)
160x120, Raw Data, Original Transfer	32Kx8x1	30
160x120, YUV4:2:0, Original Transfer	32Kx8x1	30
160x120, YUV4:2:2, Original Transfer	32Kx8x2	30
176x144, Raw Data, Original Transfer	32Kx8x1	30
176x144, YUV4:2:0, Original Transfer	32Kx8x2	30
176x144, YUV4:2:2, Original Transfer	32Kx8x2	23.67
320x240, Raw Data, Original Transfer	128Kx8x1	15.63
320x240, YUV4:2:0, Original Transfer	128Kx8x1	10.42
320x240, YUV4:2:2, Original Transfer	128Kx8 + 32Kx8	7.81
320x240, YUV4:2:2, Compressed Transfer	128Kx8x1	15.63
352x288, Raw Data, Original Transfer	128Kx8x1	11.84
352x288, YUV4:2:0, Original Transfer	128Kx8 + 32Kx8	7.89
352x288, YUV4:2:2, Original Transfer	128Kx8x2	5.92
352x288, YUV4:2:2, Compressed Transfer	128Kx8x1	11.84
640x480, Raw Data, Original Transfer	256Kx8 + 128Kx8	3.90
640x480, YUV4:2:0, Original Transfer	256Kx8x2	2.60

**Note:** assumes EyEuEv4:2:2 quantization level is used in Compressed Transfer.

**Video Camera Interface Controller with Compression**
**8 Control and Status Registers**

The internal control registers of the W9966CF/TF are selected by performing an address write cycle with data bits 7-5 = 1X0 (X = 0 for read access, X = 1 for write access). The desired register is selected by the 5-bit index value. All internal registers are 8-bit wide. Table 8.1 shows the control register map.

**TABLE 8.1 CONTROL REGISTER MAP**

INDEX	SYMBOL	DESCRIPTION
00H	CR00	Software Reset Control Register
01H	CR01	CCD/DSP Pixel Data Capture Control Register
02H	CR02	Vertical Down-Scaling Control Register
03H	CR03	Horizontal Down-Scaling Control Register
04H	CR04	Capture Window X-Start Low Register
05H	CR05	Capture Window X-Start High Register
06H	CR06	Capture Window Y-Start Low Register
07H	CR07	Capture Window Y-Start High Register
08H	CR08	Capture Window X-End Low Register
09H	CR09	Capture Window X-End High Register
0AH	CR0A	Capture Window Y-End Low Register
0BH	CR0B	Capture Window Y-End High Register
0CH	CR0C	SRAM Type Register
0DH	CR0D	Enhancement Layer Start Address - 0 Register
0EH	CR0E	Enhancement Layer Start Address - 1 Register
0FH	CR0F	Enhancement Layer Start Address - 2 Register
10H	CR10	Enhancement Layer End Address - 0 Register
11H	CR11	Enhancement Layer End Address - 1 Register
12H	CR12	Enhancement Layer End Address - 2 Register
13H	CR13	Video Encoding Engine Control Register
18H	CR18	Serial Bus Control Register
19H	CR19	General I/O Port Direction Control Register
1AH	CR1A	General I/O Port Data Register
Others		Reserved

## Video Camera Interface Controller with Compression

### 8.1 CCD Interface Register Descriptions

#### Software Reset Control Register (CR00)

---

Read/Write                      Index : 00H

Default : XXXXXXX1B

7	6	5	4	3	2	1	0
Reserved						EF_RST	SD_RST

**Bits 7-2**                      Reserved

**Bit 1**                              ECP FIFO Reset  
 0 = Normal operation  
 1 = Reset the ECP fifo

**Bit 0**                              SD Bus Reset  
 0 = Normal operation  
 1 = Reset the SD bus (tri-stated)

#### CCD/DSP Pixel Data Capture Control Register (CR01)

---

Read/Write                      Index : 01H

Default : 00H

7	6	5	4	3	2	1	0
VCE	HOLD		SKP	VSP	HSP	CM	SWAP

**Bit 7**                              CCD/DSP Pixel Data Capture Enable  
 0 = Disable  
 1 = Enable

**Bits 6-5**                        Capture Hold Control  
 00 = Continuously capture pixel data (non-interlaced mode)  
 01 = Continuously capture pixel data (interlaced mode)  
 10 = Capture and hold after one frame/field (non-interlaced/interlaced mode)  
 11 = Capture and hold after one frame (interlaced mode)

**Bit 4**                              Skip Frame or Field  
 0 = Capture all received frames or fields of pixel data  
 1 = Capture every other received frames or fields of pixel data

**Bit 3**                              VS Input Pin Polarity  
 0 = Active low  
 1 = Active high

## Video Camera Interface Controller with Compression

- Bit 2**            HS Input Pin Polarity  
 0 = Active low  
 1 = Active high
- Bit 1**            Capture Mode  
 0 = 16-bit pixel data input (YUV 4:2:2)  
 1 = 8-bit pixel data input (CCD raw data)
- Bit 0**            UV Input Data Byte Swap  
 0 = UV input data stream is in U01, V01, U23, V23 .... sequence  
 1 = UV input data stream is in V01, U01, V23, U23 .... sequence

### Vertical Down-Scaling Control Register (CR02)

---

Read/Write                      Index : 02H

Power-on Default: Undefined

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
VDS	Reserved	Vertical Down-Scaling Factor					

- Bit 7**            Vertical Down-Scaling Enable  
 0 = Disable  
 1 = Enable
- Bit 6**            Reserved
- Bits 5-0**        Vertical Down-Scaling Factor  
 This 6-bit value specifies the vertical down-scaling factor form 1/64 to 63/64.

### Horizontal Down-Scaling Control Register (CR03)

---

Read/Write                      Index : 03H

Power-on Default: Undefined

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
VDS	Reserved	Horizontal Down-Scaling Factor					

- Bit 7**            Horizontal Down-Scaling Enable  
 0 = Disable  
 1 = Enable
- Bit 6**            Reserved
- Bits 5-0**        Horizontal Down-Scaling Factor  
 This 6-bit value specifies the horizontal down-scaling factor form 1/64 to 63/64.

## Video Camera Interface Controller with Compression

### Capture Window X-Start Low Register (CR04)

---

Read/Write                      Index : 04H

Power-on Default: Undefined

7	6	5	4	3	2	1	0
Capture Window X-Start Low							

**Bits 7-0**                      Capture Window X-Start Low  
 A 10-bit value specifies number of pixels between HS and the first valid pixel data.  
 This register contains the least significant 8-bit of this value.

### Capture Window X-Start High Register (CR05)

---

Read/Write                      Index : 05H

Power-on Default: Undefined

7	6	5	4	3	2	1	0
Reserved						CWXSH	

**Bits 7-2**                      Reserved

**Bits 1-0**                      Capture Window X-Start High  
 A 10-bit value specifies number of pixels between HS and the first valid pixel data.  
 This register contains the most significant 2-bit of this value.

### Capture Window Y-Start Low Register (CR06)

---

Read/Write                      Index : 06H

Power-on Default: Undefined

7	6	5	4	3	2	1	0
Capture Window Y-Start Low							

**Bits 7-0**                      Capture Window Y-Start Low  
 A 10-bit value specifies number of lines between VS and the first valid data line. This register contains the least significant 8-bit of this value.

### Capture Window Y-Start High Register (CR07)

---

Read/Write                      Index : 07H

Power-on Default: Undefined

7	6	5	4	3	2	1	0
Reserved						CWYSH	



## Video Camera Interface Controller with Compression

**Bits 7-2**      Reserved

**Bits 1-0**      Capture Window Y-Start High  
 A 10-bit value specifies number of lines between VS and the first valid data line. This register contains the most significant 2-bit of this value.

---

### Capture Window X-End Low Register (CR08)

Read/Write                  Index : 08H

Power-on Default: Undefined

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
Capture Window X-End Low							

**Bits 7-0**      Capture Window X-End Low  
 A 10-bit value specifies number of pixels will be captured. This register contains the least significant 8-bit of this value.

---

### Capture Window X-End High Register (CR09)

Read/Write                  Index : 09H

Power-on Default: Undefined

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
Reserved						CWXEH	

**Bits 7-2**      Reserved

**Bits 1-0**      Capture Window X-End High  
 A 10-bit value specifies number of pixels of will be captured. This register contains the most significant 2-bit of this value.

---

### Capture Window Y-End Low Register (CR0A)

Read/Write                  Index : 0AH

Power-on Default: Undefined

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
Capture Window Y-End Low							

**Bits 7-0**      Capture Window Y-End Low  
 A 10-bit value specifies number of lines will be captured. This register contains the least significant 8-bit of this value.

**Video Camera Interface Controller with Compression****Capture Window Y-End High Register (CR0B)**

---

Read/Write                      Index : 0BH

Power-on Default: Undefined

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
Reserved						CWYEH	

**Bits 7-2**                      Reserved**Bits 1-0**                      Capture Window Y-End High  
A 10-bit value specifies number of lines will be captured. This register contains the most significant 2-bit of this value.

**Video Camera Interface Controller with Compression**
**8.2MCTL Register Descriptions**
**SRAM Type Register (CR0C)**


---

Read/Write                      Index : 0CH

Power-on Default: 1FH

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
Reserved			Bank-1 Type			Bank-0 Type	

**Bits 7-5**                      Reserved

**Bits 4-2**                      Bank-1 SRAM Type  
 000 = No SRAM  
 001 = 32Kx8 SRAM  
 010 = 64Kx8 SRAM  
 011 = 128Kx8 SRAM  
 1XX = 256Kx8 SRAM

**Bits 1-0**                      Bank-0 SRAM Type  
 00 = 32Kx8 SRAM  
 01 = 64Kx8 SRAM  
 10 = 128Kx8 SRAM  
 11 = 256Kx8 SRAM

**Enhancement Layer Start Address - 0 Register (CR0D)**


---

Read/Write                      Index : 0DH

Power-on Default: Undefined

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
Enhancement Layer Start Address - 0							

**Bits 7-0**                      Enhancement Layer Start Address - 0  
 A 19-bit value specifies the starting address of frame buffer for the enhancement layer data stream. This register contains the least significant 8-bit of this value.

**Enhancement Layer Start Address -1 Register (CR0E)**


---

Read/Write                      Index : 0EH

Power-on Default: Undefined

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
----------	----------	----------	----------	----------	----------	----------	----------

## Video Camera Interface Controller with Compression

Enhancement Layer Start Address - 1
-------------------------------------

**Bits 7-0**      Enhancement Layer Start Address -1  
 A 19-bit value specifies the starting address of frame buffer for the enhancement layer data stream. This register contains bits 15-8 of this value.

---

### Enhancement Layer Start Address -2 Register (CR0F)

---

Read/Write                      Index : 0FH

Power-on Default: Undefined

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
Reserved					ELSA2		

**Bits 7-2**      Reserved

**Bits 1-0**      Enhancement Layer Start Address -2  
 A 19-bit value specifies the starting address of frame buffer for the enhancement layer data stream. This register contains bits 18-16 of this value.

---

### Enhancement Layer End Address - 0 Register (CR10)

---

Read/Write                      Index : 10H

Power-on Default: Undefined

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
Enhancement Layer End Address - 0							

**Bits 7-0**      Enhancement Layer End Address - 0  
 A 19-bit value specifies the ending address of frame buffer for the enhancement layer data stream. This register contains the least significant 8-bit of this value.

---

### Enhancement Layer End Address -1 Register (CR11)

---

Read/Write                      Index : 11H

Power-on Default: Undefined

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
Enhancement Layer End Address - 1							

**Bits 7-0**      Enhancement Layer End Address -1  
 A 19-bit value specifies the starting address of frame buffer for the enhancement layer data stream. This register contains bits 15-8 of this value.

**Video Camera Interface Controller with Compression****Enhancement Layer End Address -2 Register (CR12)**

---

Read/Write                      Index : 12H

Power-on Default: Undefined

7	6	5	4	3	2	1	0
Reserved					ELEA2		

**Bits 7-2**                      Reserved**Bits 1-0**                      Enhancement Layer End Address -2  
A 19-bit value specifies the starting address of frame buffer for the enhancement layer data stream. This register contains bits 18-16 of this value.

**Video Camera Interface Controller with Compression**
**8.3 Video Encoding Engine Register Descriptions**
**Video Encoding Engine Control Register (CR13)**


---

Read/Write                      Index : 13H

Power-on Default : 00H

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
BLE	ELE	ECE	ECDF		EDF	RES	

- Bit 7**                      Base Layer Enable  
 0 = Disable  
 1 = Enable
- Bit 6**                      Enhancement Layer Enable  
 0 = Disable  
 1 = Enable
- Bit 5**                      Enhancement Layer Error Correction Enable  
 0 = Disable  
 1 = Enable
- Bits 4-3**                    Enhancement Layer Error Correction Quantization Level  
 00 = EyEuEv4:2:2  
 01 = Reserved  
 10 = EyEuEv3:1:1  
 11 = EyEuEv2:1:1
- Bit 2**                      Output Data Format  
 0 = Equivalent YUV 4:2:2 data format  
 1 = Equivalent YUV 4:2:0 data format
- Bits 1-0**                    Reserved

**Video Camera Interface Controller with Compression**
**8.4 Miscellaneous Control Register Descriptions**
**Serial Bus Control Register (CR18)**


---

Read/Write                      Index 18H

Power-on Default: 03H

7	6	5	4	3	2	1	0
Reserved			DE/DS	SIDR	SICR	SIDW	SICW

**Bits 7-5**                      Reserved

**Bit 4**                      Serial Data Enable/Serial Data Strobe  
 0 = SDE#/SDS pin is driven low  
 1 = SDE#/SDS pin is driven high

**Bit 3**                      Serial Interface Data Read (Read only)  
 0 = SDATA is low  
 1 = SDATA is high

**Bit 2**                      Serial Interface Clock Read (Read only)  
 0 = SCLK is low  
 1 = SCLK is high

**Bit 1**                      Serial Interface Data Write  
 0 = SDATA is driven low  
 1 = SDATA is tri-stated

**Bit 0**                      Serial Interface Clock Write  
 0 = SCLK is driven low  
 1 = SCLK is tri-stated

**General I/O Port Direction Control Register (CR19)**


---

Read/Write                      Index 19H

Power-on Default: 00H

7	6	5	4	3	2	1	0
GIOP7D	GIOP6D	GIOP5D	GIOP4D	GIOP3D	GIOP2D	GIOP1D	GIOP0D

**Bit 7**                      GIOP7 Direction  
 0 = Input  
 1 = Output

**Bit 6**                      GIOP6 Direction  
 0 = Input

## Video Camera Interface Controller with Compression

1 = Output

- Bit 5**      GIOP5 Direction  
0 = Input  
1 = Output
- Bit 4**      GIOP4 Direction  
0 = Input  
1 = Output
- Bit 3**      GIOP3 Direction  
0 = Input  
1 = Output
- Bit 2**      GIOP2 Direction  
0 = Input  
1 = Output
- Bit 1**      GIOP1 Direction  
0 = Input  
1 = Output
- Bit 0**      GIOP0 Direction  
0 = Input  
1 = Output

### General I/O Port Data Register (CR1A)

---

Read/Write                  Index 1AH

Power-on Default: 00H

7	6	5	4	3	2	1	0
GIOP7R	GIOP6R	GIOP5R	GIOP4R	GIOP3R	GIOP2R	GIOP1R	GIOP0R

- Bit 7**      GIOP7 Data  
0 = GIOP7 pin is 0  
1 = GIOP7 pin is 1
- Bit 6**      GIOP6 Data  
0 = GIOP6 pin is 0  
1 = GIOP6 pin is 1
- Bit 5**      GIOP5 Data  
0 = GIOP5 pin is 0  
1 = GIOP5 pin is 1
- Bit 4**      GIOP4 Data  
0 = GIOP4 pin is 0  
1 = GIOP4 pin is 1



---

**Video Camera Interface Controller with Compression**

<b>Bit 3</b>	GIOP3 Data 0 = GIOP3 pin is 0 1 = GIOP3 pin is 1
<b>Bit 2</b>	GIOP2 Data 0 = GIOP2 pin is 0 1 = GIOP2 pin is 1
<b>Bit 1</b>	GIOP1 Data 0 = GIOP1 pin is 0 1 = GIOP1 pin is 1
<b>Bit 0</b>	GIOP0 Data 0 = GIOP0 pin is 0 1 = GIOP0 pin is 1

**Video Camera Interface Controller with Compression**
**9 Electrical Characteristics**
**9.1 Absolute Maximum Ratings**
**TABLE 9.1 ABSOLUTE MAXIMUM RATINGS**

Ambient temperature	0° C to 70° C
Storage temperature	-40° C to 125° C
DC supply voltage	-0.5V to 7V
I/O pin voltage with respect to $V_{SS}$	-0.5V to $V_{DD} + 0.5V$

**9.2 DC Specifications**
**TABLE 9.2 DC SPECIFICATIONS**

(VDD= 4.75 V to 5.25 V, VSS= 0 V, TA= 0 °C to 70 °C)

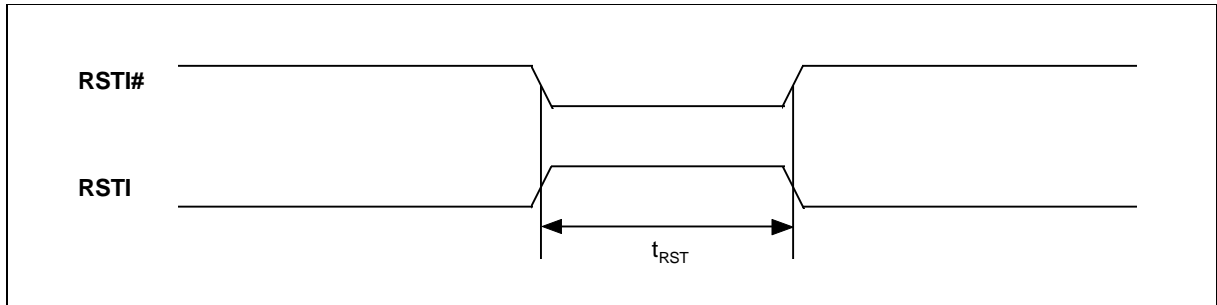
Symbol	Parameter	Condition	Min	Max	Unit
$V_{DD}$	Power Supply		4.75	5.25	V
$V_{IL}$	Input Low Voltage			0.8	V
$V_{IH}$	Input High Voltage		2.0		V
$V_{OL}$	Output Low Voltage			$V_{SS} + 0.4$	V
$V_{OH}$	Output High Voltage		2.4		V
$I_{IL}$	Input Low Leakage Current	$V_{IN} = 0.4 V$		-70	$\mu A$
$I_{IH}$	Input High Leakage Current	$V_{IN} = 2.4 V$		70	$\mu A$
$I_{UP}$	Pull-up Current	$V_{IN} = 0 V$	-133.2	-400.6	$\mu A$
$C_{IN}$	Input Capacitance			5	pF
$C_{OUT}$	Output Capacitance			5	pF
$I_{CC}$	Power Supply Current			TBD	mA

**Note :** Input leakage currents include Hi-Z output leakage for bi-directional buffers with tri-state outputs.

**Video Camera Interface Controller with Compression**

**9.3 AC Specifications**

**9.3.1 Reset Specifications**

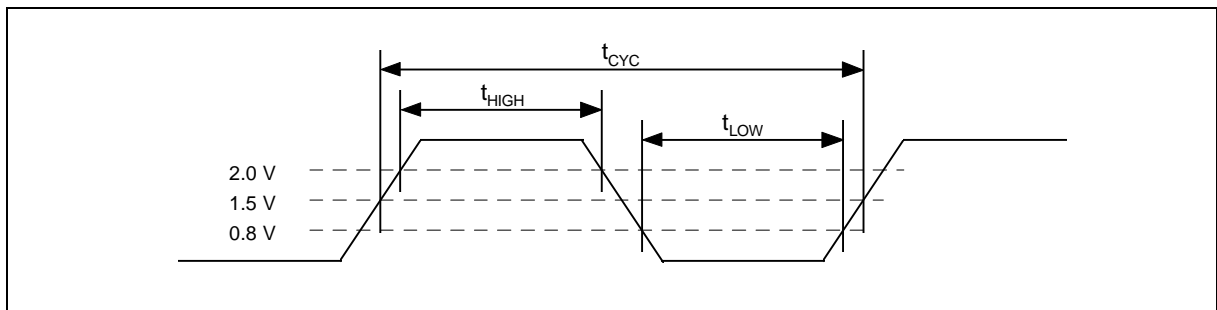


**FIGURE 9.1 RESET TIMING**

**TABLE 9.3 RESET TIMING PARAMETERS**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{RST}$	System Reset Pulse Width	100			ns

**9.3.2 Clock Specifications**



**FIGURE 9.2 CLOCK WAVEFORM**

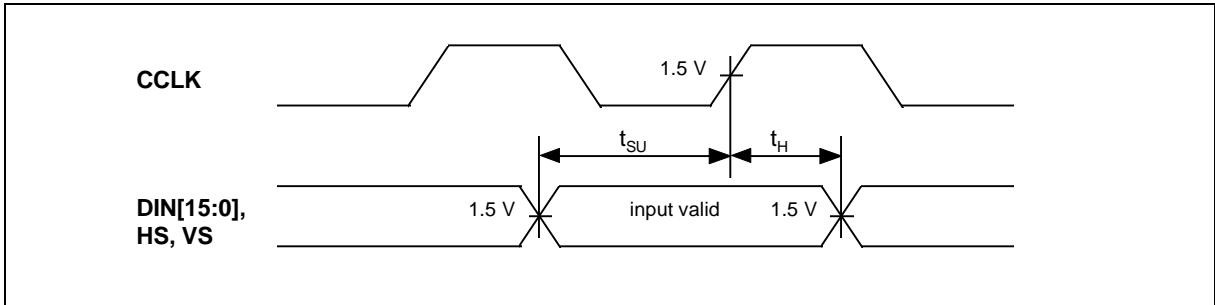
**TABLE 9.4 CLOCK TIMING PARAMETERS**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC}$	CCLK Cycle Time		74.1	200	ns
	MCLK Cycle Time			37	ns
$t_{HIGH}$	CCLK High Time	5			ns
	MCLK High Time	5			ns

**Video Camera Interface Controller with Compression**

$t_{LOW}$	CCLK Low Time	5			ns
	MCLK Low Time	5			ns

**9.3.3 Video Input Timing Specifications**

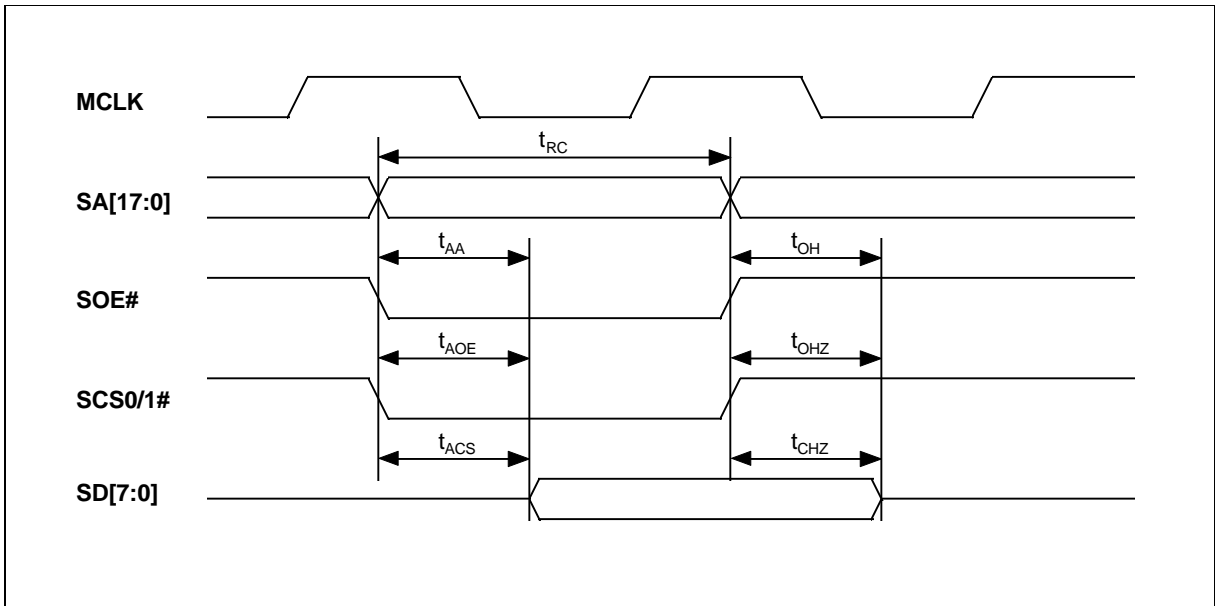


**FIGURE 9.3 VIDEO INPUT TIMING**

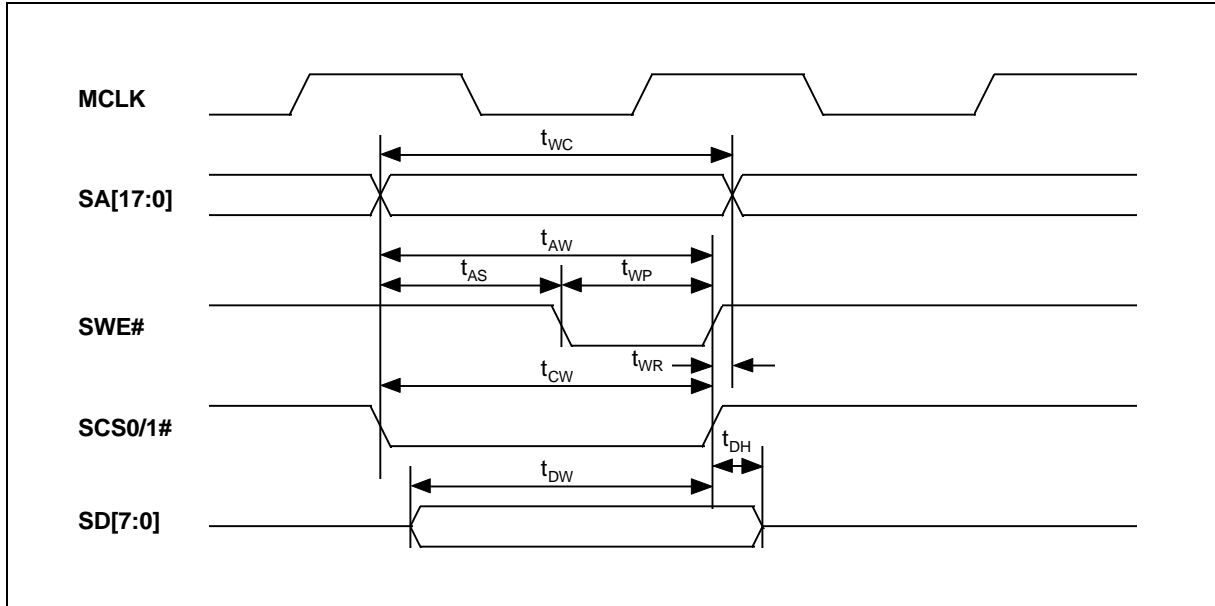
**TABLE 9.5 VIDEO INPUT TIMING PARAMETERS**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{SU}$	DIN[15:0], HS, VS	6			ns
$t_H$	DIN[15:0], HS, VS	4			ns

**9.3.4 SRAM Timing Specifications**



**FIGURE 9.4 SRAM READ CYCLE TIMING**

**Video Camera Interface Controller with Compression**

**FIGURE 9.5 SRAM WRITE CYCLE TIMING**
**TABLE 9.6 SRAM READ CYCLE TIMING PARAMETERS**

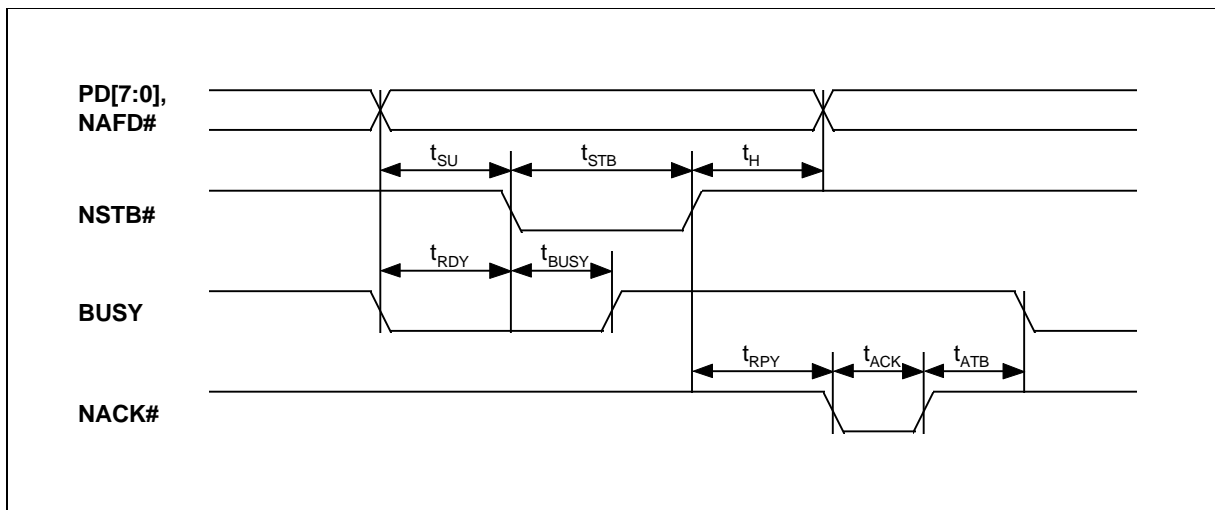
Symbol	Parameter	Min	Typ	Max	Unit
$t_{RC}$	Read Cycle Time	25		37	ns
$t_{AA}$	Address Access Time			$t_{RC} - 10$	ns
$t_{ACS}$	Chip Select Access Time			$t_{RC} - 10$	ns
$t_{AOE}$	Output Enable to Output Valid			$t_{RC} - 10$	ns
$t_{CHZ}$	Chip De-selecting to Output in High Z	0			ns
$t_{OHZ}$	Output Disable to Output in High Z	0			ns
$t_{OH}$	Output Hold Time from Address Change	0			ns

**TABLE 9.7 SRAM WRITE CYCLE TIMING PARAMETERS**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{WC}$	Write Cycle Time	25		37	ns
$t_{CW}$	Chip Select to End of Write	$t_{RC} - 7$			ns
$t_{AW}$	Address Valid to End of Write	$t_{RC} - 5$			ns
$t_{AS}$	Address Setup Time	10			ns

**Video Camera Interface Controller with Compression**

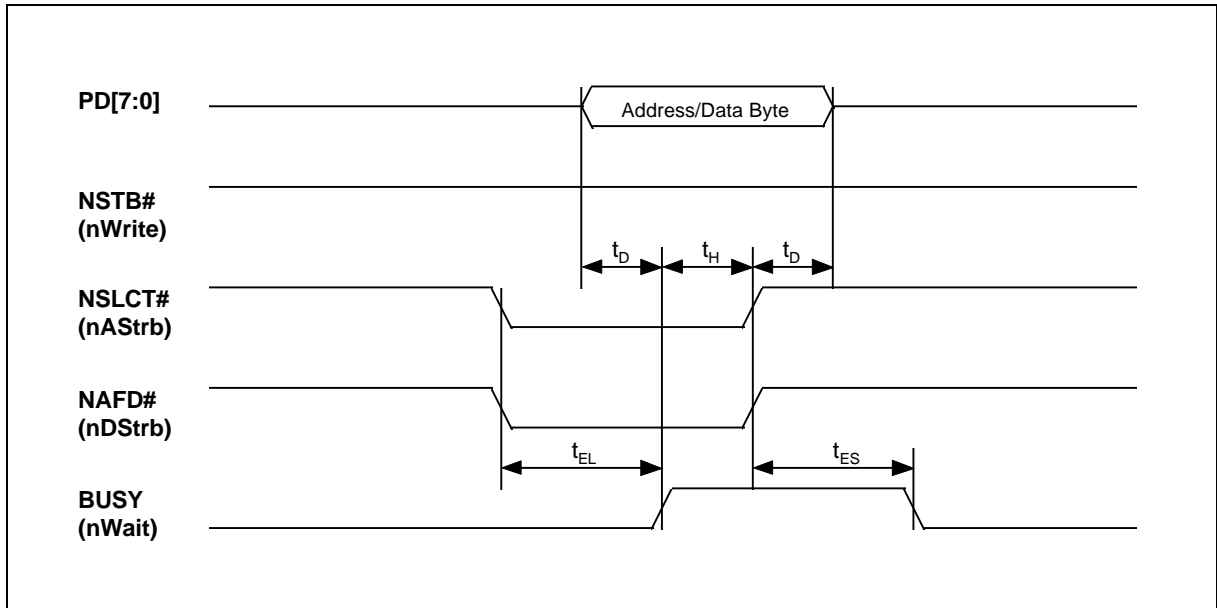
$t_{WP}$	Write Pulse Width	$0.4 t_{WC}$		$0.6 t_{WC}$	ns
$t_{WR}$	Write Recovery Time (SCS0/1#, SWE#)	1			ns
$t_{DW}$	Data Valid to End of Write	$t_{RC} - 5$			ns
$t_{DH}$	Data Hold Time from End of Write	2			ns

**9.3.5 Standard Parallel Port (SPP) Timing Specifications**

**FIGURE 9.6 STANDARD PARALLEL PORT (SPP) TIMING**
**TABLE 9.8 STANDARD PARALLEL PORT (SPP) TIMING PARAMETERS**

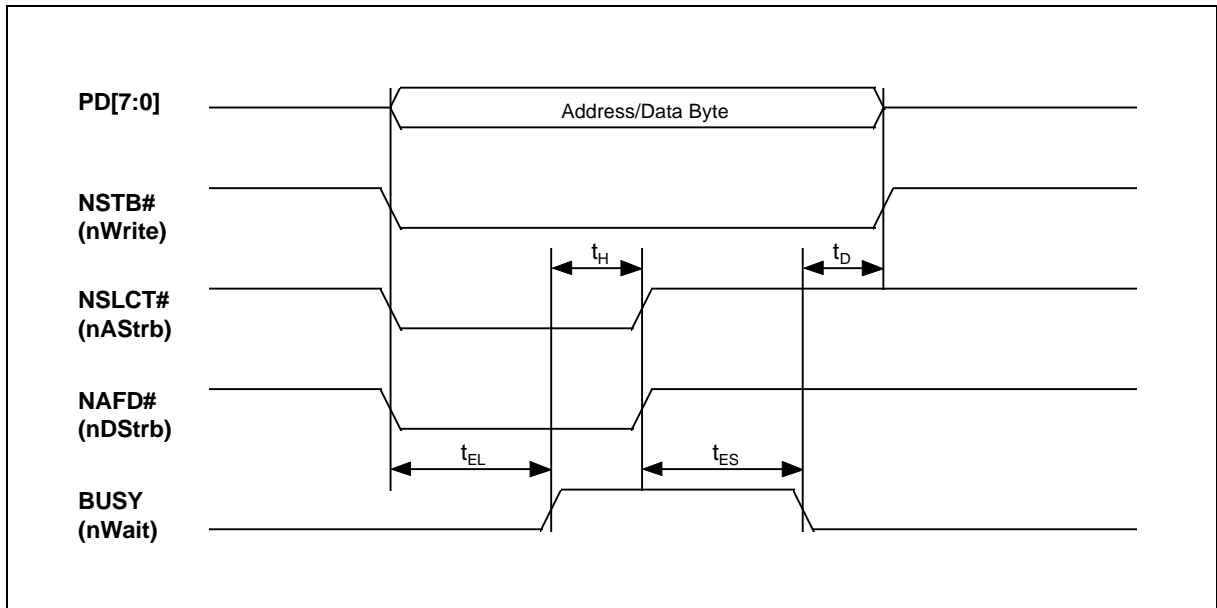
Symbol	Parameter	Min	Typ	Max	Unit
$t_{SU}$	Data Setup Time	500			ns
$t_{STB}$	Strobe Pulse Width	500			ns
$t_H$	Data Hold Time	500			ns
$t_{RDY}$	Busy Inactive to Strobe Active	0			ns
$t_{BUSY}$	Strobe Active to Bust Active			500	ns
$t_{RPY}$	Strobe Inactive to Ack Active	0			ns
$t_{ACK}$	Ack Pulse Width	500		10000	ns
$t_{ATB}$	Ack Inactive to Busy Inactive	0			ns

**9.3.6 Enhanced Parallel Port (EPP) Timing Specifications**

**Video Camera Interface Controller with Compression**



**FIGURE 9.7 EPP DATA OR ADDRESS READ TIMING**



**FIGURE 9.8 EPP DATA OR ADDRESS WRITE TIMING**

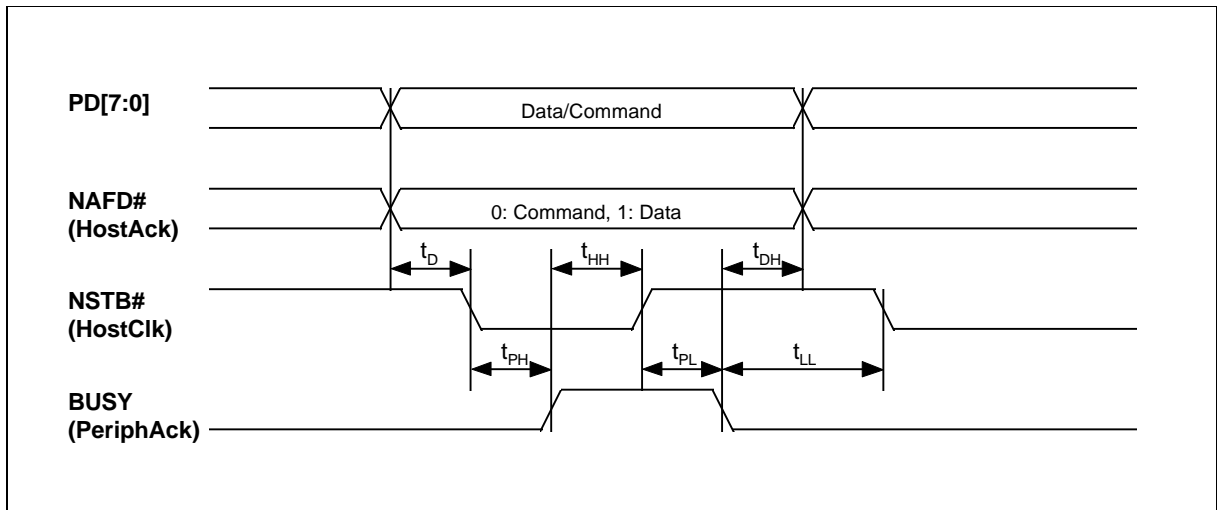
**TABLE 9.9 EPP TIMING PARAMETERS**

Symbol	Parameter	Min	Typ	Max	Unit
--------	-----------	-----	-----	-----	------

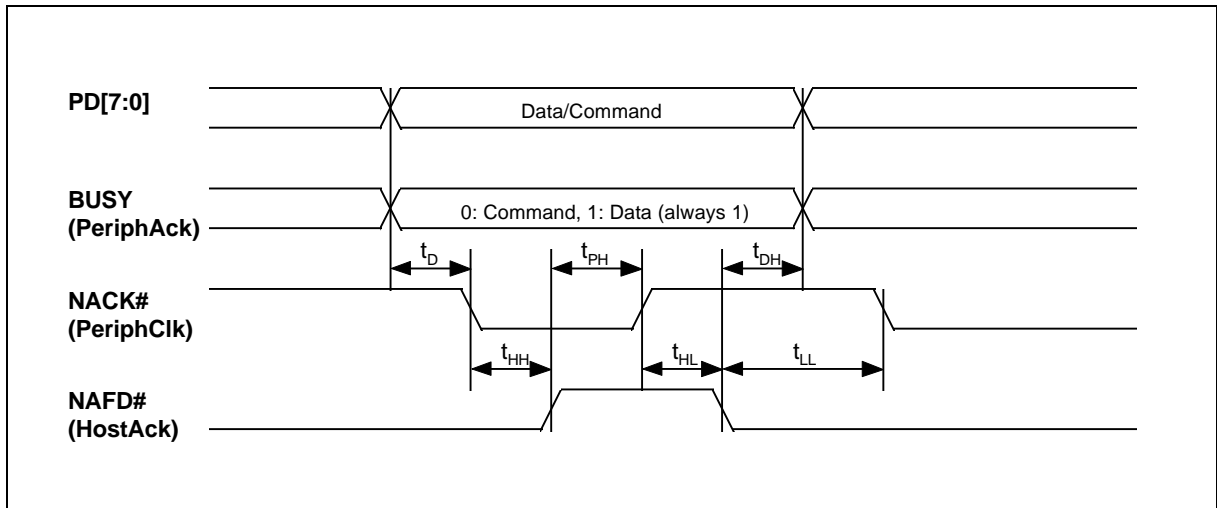
**Video Camera Interface Controller with Compression**

$t_D$	Data Setup Time	0			ns
$t_H$	Host Response Time	0		1	s
$t_{EL}$	Long Response Time	0		10	us
$t_{ES}$	Short Response Time	0		125	ns

**9.3.7 Extended Capabilities Port (ECP) Timing Specifications**



**FIGURE 9.9 ECP FORWARD TIMING**



**FIGURE 9.10 ECP REVERSE TIMING**

**TABLE 9.10 ECP TIMING PARAMETERS**



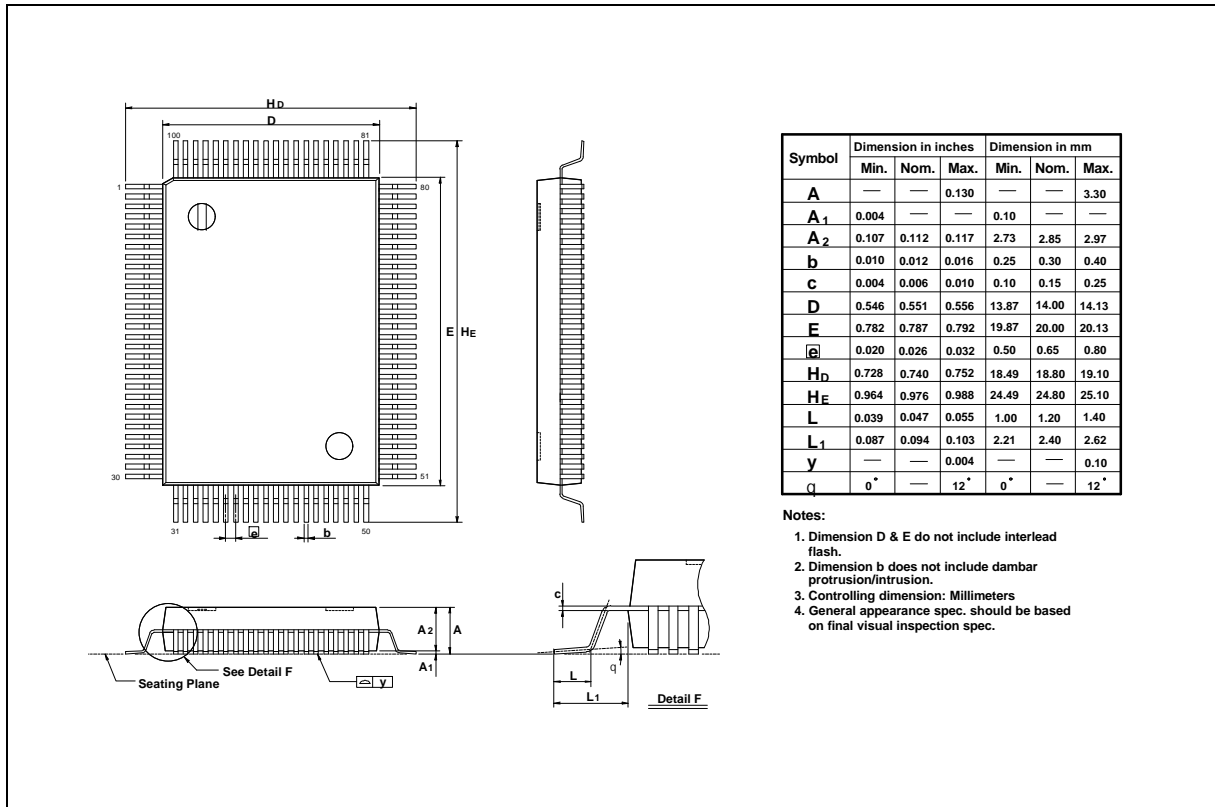
**Video Camera Interface Controller with Compression**

<b>Symbol</b>	<b>Parameter</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>
$t_D$	Data Setup Time	0			ns
$t_{PH}$	Peripheral Response High Time	75			ns
$t_{HH}$	Host Response High Time	0		1	s
$t_{PL}$	Peripheral Response Low Time	0		35	ms
$t_{HL}$	Host Response Low Time	0		1	s
$t_{DH}$	Data Hold Time	0			ns
$t_{LL}$	Low to Low Response Time	0			ns

## Video Camera Interface Controller with Compression

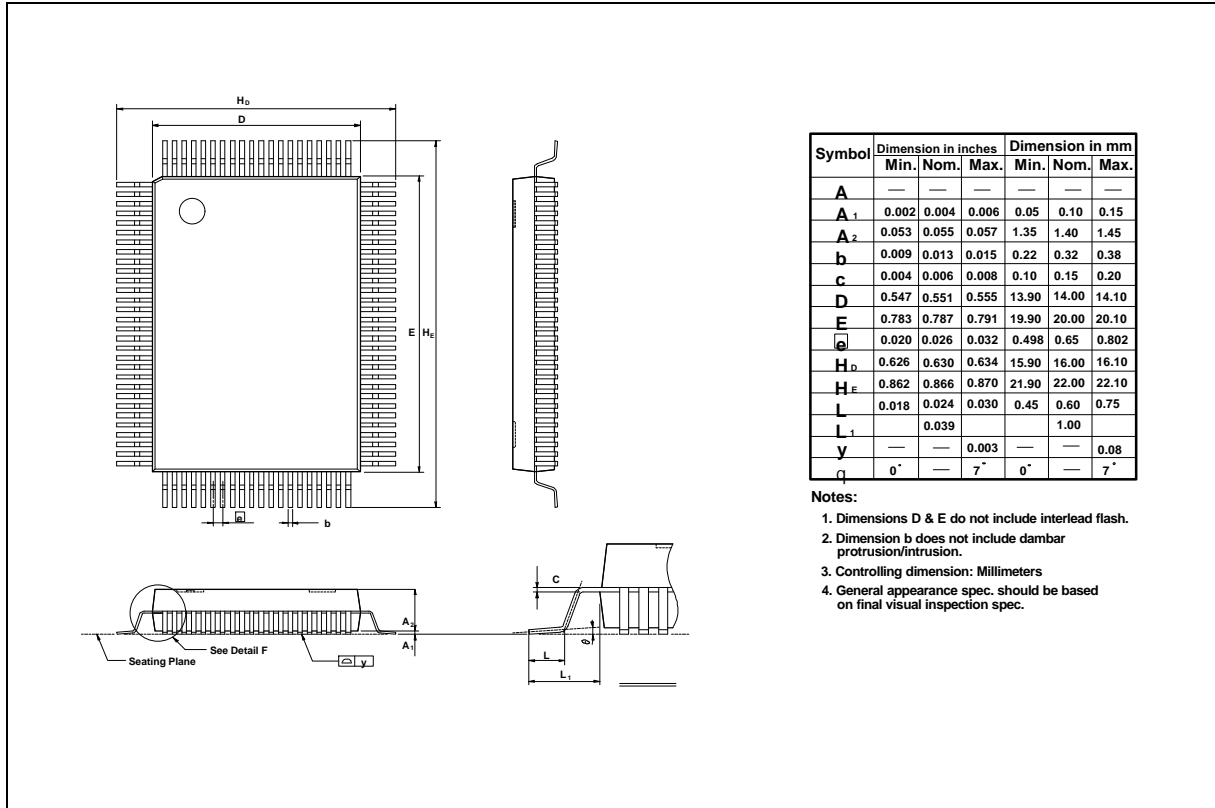
### 10Package Spec.

The W9966CF/TF is packaged in a 100-pin PQFP/TQFP package. Figure 10.1 shows the mechanical dimensions for W9966CF, and Figure 10.2 shows the mechanical dimensions for W9966TF.



**FIGURE 10.1 W9966CF 100-PIN PQFP DIMENSIONS**

## Video Camera Interface Controller with Compression



**FIGURE 10.2 W9966TF 100-PIN TQFP DIMENSIONS**

**Video Camera Interface Controller with Compression****11 Ordering Information**

<b>Part No.</b>	<b>Package</b>
W9966CF	100-pin PQFP
W9966TF	100-pin TQFP

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**Note: All data and specifications are subject to change without notice.**