Winbond Electronics Corp.

JPEG USB CAMERA CHIP

W9967CF

JPEG USB Camera Chip

Revision History

Revision	Issue Date	Comments
A1	April, 1998	Formal release.
A2	February, 1999	Removed SerialNumber string descriptor. Changed IHV-specific information support through external EEPROM or uC to only Vendor ID and Product ID.
A3	April, 1999	Removed uC interface.
A4	May, 1999	Supports USB Spec. Rev. 1.1. Changed bcdUSB and bcdDevice values from 0x0100 to 0x0110. Added CR39_4 for JPEG clock enable.

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1 GENERAL DESCRIPTION

The W9967CF is a digital video processing chip offered by Winbond to facilitate adapterless connection between digital video camera and personal computer for video and still image capturing and editing, video e-mail, and video conferencing applications. Low-cost, high-performance, and high-quality digital video camera can be realized by using Winbond's W9967CF, which includes Universal Serial Bus (USB) technology and the international standard JPEG compression.

The digital video camera is becoming the next great input device for the PC. USB is now a common PC standard for connecting peripheral products, which features low cost, hot-attachable plug and play, adequate 12 Mb/s full speed bandwidth, and simultaneous attachment of multiple devices. The W9967CF has built-in full speed USB controller which benefits from using the isochronous data transfer mode of the USB bus, and which is compliant with the full power management requirements of the USB specification, including startup, operating, and suspend modes. To prevent saturation of the USB bus, the W9967CF uses no more than 8 Mb/s of available bandwidth to ensure the continued operation of other low bandwidth devices such as USB mice and keyboards.

Although USB provides a low-cost solution for low to medium speed peripherals, its 12 Mb/s bandwidth is not enough for high-quality and high-performance digital video camera. High-quality and low-cost compression is necessary to boost frame rate for a high-performance digital video camera. The W9967CF has built-in the baseline JPEG compression, which corresponds to the ISO/IEC international standard 10918-1, with YCbCr4:2:2 or YCbCr4:2:0 components in non-interleaved scan. The baseline JPEG implementation in the W9967CF includes Discrete Cosine Transform (DCT), quantization, zig-zag scan, and Huffman encoder. With JPEG compression, the W9967CF can easily achieve good quality 30 frames per second (fps) in CIF resolution (352×288) and 10~15 fps in VGA resolution (640×480) by consuming no more than 8 Mb/s USB bandwidth.

The W9967CF can accept NTSC, PAL, or VGA video in 8- or 16-bit YCbCr4:2:2 format, square or rectangular pixels, and converts to sub-QCIF (128×96), QCIF (176×144), CIF (128×96), SIF (352×240), 320×240, or VGA (640×480) format. Built-in cropping window control and arbitrary scaling in both the horizontal and vertical directions can serve as the digital pan and zoom over a user-specified region for camera control.

An on-chip DRAM controller is used to interface to SDRAM or EDO DRAM through a 16-bit data bus. An external serial E^2PROM is also supported if IHV-specific Vendor ID and Product ID are needed. The W9967CF is a 3.3 V device with TTL-compatible 3.3 V or 5.0 V I/O, and is packaged in a 128L QFP.

2 FEATURES

❑ USB Interface

- Fully compliant with USB Specification Revision 1.1
- Supports for full speed devices with maximum 12 Mb/s USB bandwidth
- Uses no more than 8 Mb/s USB bandwidth to prevent saturation of the USB bus
- Provides multiple alternate settings for various isochronous bandwidth consumptions
- Does not use isochronous bandwidth for default alternate setting 0
- Complies with USB power management requirements
- USB Control and Isochronous transfers
- On-chip USB full speed transceivers
- Bus-powered high power devices

❑ Video Compression

- Fully compliant with ISO/IEC 10918-1 international JPEG standard
- On-chip DCT, quantization, zig-zag scan, and Huffman encoder
- Contains two AC and two DC Huffman code tables, and two programmable quantization tables
- Supports baseline sequential mode in YCbCr4:2:2 or YCbCr4:2:0 non-interleaved scan
- Encodes in sub-QCIF (128x96), QCIF (176x144), CIF (352x288), SIF (352x240), 320x240, or VGA (640x480) picture format
- Encodes sub-QCIF/QCIF/CIF/SIF/320x240 format at 30 frames per second (fps), VGA format at 10~15 fps

❑ Video Pre-processing

- Direct connect to digital camera through an 8- or 16-bit data bus
- Glueless interface to NTSC/PAL TV decoder
- Input video format compliant with YCbCr 4:2:2 CCIR 601 standard
- Built-in cropping, arbitrary scaling, and filtering functions for digital pan and zoom camera control

❑ **Video Output**

- Video output can be either compressed bit stream or original video
- Compressed bit stream is fully compliant with ISO baseline JPEG standard in YCbCr4:2:2 or YCbCr4:2:0 non-interleaved scan
- Original video output can be in YCbCr4:2:2 or YCbCr4:2:0 packed format

❑ **DRAM Interface**

- Supports SDRAM or 1-cycle EDO DRAM
- Supports SDRAM Self Refresh
- Supports 16-bit DRAM interface in 0.5, 1, 2 or 4 Mbytes configuration

❑ **Serial EEPROM Interface**

- Supports optional 1K (128×8) serial EEPROM for IHV-specific Vendor ID and Product ID

❑ **Supports Hardware and Software Snap Shot**

❑ **Built-in PLL (Phase-Locked Loops) Clock Synthesizer**

❑ **Operating Frequency is 48 MHz with Video Input Frequency of 13.5 MHz (typical)**

❑ **3.3 V Device with TTL-compatible 3.3 V or 5.0 V I/O**

❑ **128L QFP Package**

3 PIN CONFIGURATION

The W9967CF is packaged in a 128L QFP. The pin configuration is shown in Figure 3.1.

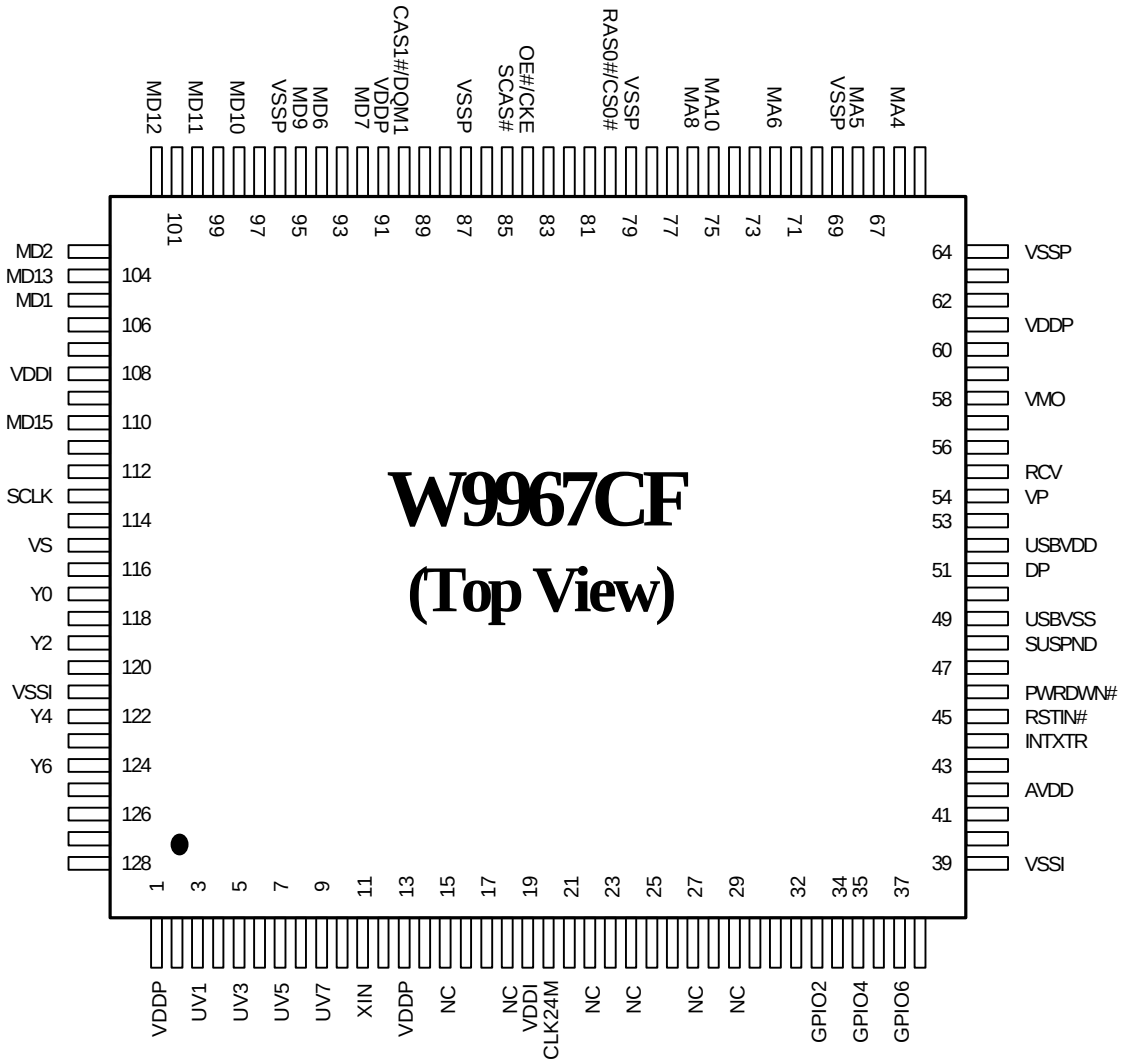


Figure 3.1 W9967CF Pin Configuration

4 PIN DESCRIPTION

The following signal types are used in these descriptions.

I	Input pin
IU	Input pin with internal pull-up resistor
B	Bi-directional input/output pin
O	Output pin
AIO	Analog input/output pin
P	Power supply pin
G	Ground pin
#	Active low

4.1 Pin Definition

USB and External Transceiver Interface (8 pins)

Pin Name	Pin Number	Type	Description
DM	50	AIO	Data Minus line of differential USB upstream port.
DP	51	AIO	Data Plus line of differential USB upstream port. Note: provide an external 1.5 KΩ pull-up resistor at DP so the device indicates to the host that it is a full-speed device.
VM	53	IU	Single-ended Receiver Input of the data minus line.
VP	54	IU	Single-ended Receiver Input of the data plus line.
RCV	55	IU	Differential Receiver Input.
TOE#	57	O	Output Enable for external transceiver.
VMO	58	O	Data Minus Output to the differential driver.
VPO	59	O	Data Plus Output to the differential driver.

DRAM Interface (37 pins)

Pin Name	Pin Number	Type	Description
MD[15:0]	92-95, 97-106, 109-110	B	Data Bus.
MA[10:0]	65-68, 70, 72-77	O	Address Bus. Note: for SDRAM, MA[10:0] are sampled during the ACTIVE

			command (row address MA[10:0]) and READ/WRITE command (column address MA[7:0], with MA10 defining AUTO PRECHARGE) to select one location out of the 521K available in the respective bank. MA10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (MA10 HIGH).
BA	78	O	EDO DRAM: Not used. SDRAM: Bank Address Input. BA defines to which internal bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA is also used to program the 12th bit of the Mode Register.
RAS[1:0]# CS[1:0]#	80, 81	O	EDO DRAM: Row Address Strobes. SDRAM: Chip Select. CS# enables the command decoder for the SDRAM.
CAS[1:0]# DQM[1:0]	89, 90	O	EDO DRAM: Column Address Strobes. SDRAM: Input/Output Mask. DQM[1:0] are input mask signals for write accesses and output enable signals for read accesses. DQM0 corresponds to MD[7:0]; DQM1 corresponds to MD[15:8].
OE# CKE	84	O	EDO DRAM: Output Enable. SDRAM: Clock Enable. CKE activates the SMCLK signal. The SDRAM enters precharge power-down to deactivate the input and output buffers, excluding CKE, for maximum power saving when CKE is LOW coincident with a NOP.
WE#	88	O	EDO DRAM: Write Enable. SDRAM: Command Input. SRAS#, SCAS#, and WE# (along with CS#) define the command being entered.
SRAS#	82	O	EDO DRAM: Not used. SDRAM: Command Input. SRAS#, SCAS#, and WE# (along with CS#) define the command being entered.
SCAS#	85	O	EDO DRAM: Not used. SDRAM: Command Input. SRAS#, SCAS#, and WE# (along with CS#) define the command being entered.
SMCLK	86	O	EDO DRAM: Not used. SDRAM: Clock.

Input Video Interface (22 pins)

Pin Name	Pin Number	Type	Description
Y[7:0]	117-120, 122-125	I	Digital Y (Luminance) Inputs in 16-bit Mode, or Digital YUV Inputs in 8-bit Mode.

UV[7:0]	2-9	I	Digital UV (Chrominance) Inputs in 16-bit Mode, or Not Used in 8-bit Mode.
HS	116	I	Horizontal Sync Input. Programmable polarity.
VS	115	I	Vertical Sync Input. Programmable polarity.
VICLK	127	I	Input Video Clock.
SDE#/SDS	112	O	Serial Data Enable/Serial Data Strobe.
SCLK	113	B	Serial Interface Clock.
SDATA	114	B	Serial Interface Data.

Serial E^2PROM Interface (2 pins)

Pin Name	Pin Number	Type	Description
SCL	62	O	Serial Clock.
SDA/EEPROM	63	B	Serial Data/Serial E^2PROM Detection. During a reset operation, the W9967CF samples this signal to see if an external E^2PROM exists. A 10K ohm pull-up resistor should be used if an external E^2PROM is used; otherwise it should be tied to VSS.

Miscellaneous (31 pins)

Pin Name	Pin Number	Type	Description
XIN	11	I	Reference frequency input from a crystal or a clock source. It should be 48 Mhz if PLL is off (PLLSEL = 0) or 12 Mhz if PLL is on (PLLSEL = 1) for full-speed device.
XOUT	12	O	Oscillator output to a crystal. This pin is left unconnected if an external clock source is employed.
SANP#	17	IU	Snap Shot Input.
CLK24M	20	O	24 Mhz Clock Output.
GPIO[7:0]	31-38	B	General Purpose I/Os.
TEST#	40	IU	Test Input.
INTXTR	44	I	Internal USB Transceiver Select. 0: off; 1: on.
RSTIN#	45	IU	System Reset Input.
PWRDWN#	46	O	Low-active Power Down Control. This pin is active upon reset, suspended, or when the Camera Power-on Control register (CR00_4) is 0. Once active, it remains active until the CR00_4 is set to 1.

PWRDWN	47	O	High-active Power Down Control. This pin is active upon reset, suspended, or when the Camera Power-on Control register (CR00_4) is 0. Once active, it remains active until the CR00_4 is set to 1.
SUSPND	48	O	USB Suspend Mode. This pin is active when the W9967CF is in the suspend mode. It is cleared to 0 when the W9967CF is resumed, or reset by RSTIN# pin or a USB reset command.
RSTOUT	56	O	Reset Output. This pin is active when RSTIN# pin is active, or a USB reset command is received.
NC	14-16, 18, 21-24, 26-29		Not Connected.

Power and Ground (28 pins)

Pin Name	Pin Number	Type	Description
VDD5V	128	P	5V Buffer Power Supply. Provide 5V power to the I/O buffers for 5V input tolerance. +4.4 V ~ +5.25 V.
VDDP	1, 13, 30, 61, 71, 91, 107	P	Buffer Power Supply. Provide isolated power to the I/O buffers for improved noise immunity. +3.3 V ± 0.3 V.
VSSP	10, 25, 64, 69, 79, 87, 96, 111, 126	G	Buffer Ground.
USBVDD	52	P	USB Transceiver Power Supply. +3.3 V ± 0.3 V.
USBVSS	49	G	USB Transceiver Ground.
AVDD	42	P	PLL Power Supply. +3.3 V ± 0.3 V.
AVSS	43	G	PLL Ground.
VDDI	19, 60, 108	P	Core Logic Power Supply. +3.3 V ± 0.3 V.
VSSI	39, 41, 83, 121	G	Core Logic Ground.

4.2 Pin List

Table 4.1 W9967CF Pin List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VDDP	33	GPIO2	65	MA3	97	MD5
2	UV0	34	GPIO3	66	MA4	98	MD10
3	UV1	35	GPIO4	67	MA2	99	MD4
4	UV2	36	GPIO5	68	MA5	100	MD11
5	UV3	37	GPIO6	69	VSSP	101	MD3
6	UV4	38	GPIO7	70	MA1	102	MD12
7	UV5	39	VSSI	71	VDDP	103	MD2
8	UV6	40	TEST#	72	MA6	104	MD13
9	UV7	41	VSSI	73	MA0	105	MD1
10	VSSP	42	AVDD	74	MA7	106	MD14
11	XIN	43	AVSS	75	MA10	107	VDDP
12	XOUT	44	INTXTR	76	MA8	108	VDDI
13	VDDP	45	RSTIN#	77	MA9	109	MD0
14	NC	46	PWRDWN#	78	BA	110	MD15
15	NC	47	PWRDWN	79	VSSP	111	VSSP
16	NC	48	SUSPND	80	RAS0#/CS0#	112	SDE#/SDS
17	SNAP#	49	USBVSS	81	RAS1#/CS1#	113	SCLK
18	NC	50	DM	82	SRAS#	114	SDATA
19	VDDI	51	DP	83	VSSI	115	VS
20	CLK24M	52	USBVDD	84	OE#/CKE	116	HS
21	NC	53	VM	85	SCAS#	117	Y0
22	NC	54	VP	86	SMCLK	118	Y1
23	NC	55	RCV	87	VSSP	119	Y2
24	NC	56	RSTOUT	88	WE#	120	Y3
25	VSSP	57	TOE#	89	CAS0#/DQM0	121	VSSI
26	NC	58	VMO	90	CAS1#/DQM1	122	Y4
27	NC	59	VPO	91	VDDP	123	Y5
28	NC	60	VDDI	92	MD7	124	Y6
29	NC	61	VDDP	93	MD8	125	Y7
30	VDDP	62	SCL	94	MD6	126	VSSP
31	GPIO0	63	SDA/EEPROM	95	MD9	127	VICLK
32	GPIO1	64	VSSP	96	VSSP	128	VDD5V

Note 1. All output and bi-directional pins, except XOUT pin, are tri-stated during reset.

4.3 Power-on Reset Initialization

During power-on reset, states of the memory data lines MD[7:0] are latched into the W9967CF's internal configuration registers as device configuration information. Since each pin of MD[7:0] is internally pulled up on its I/O buffer, no external pull-up resistor is required. For pull-down, a 4.7K ohm resistor is recommended. Table 4.2 describes the power-on reset configuration definitions.

Table 4.2 Power-on Reset Configuration Definitions

MD Bit	Value	Definition	Conf Reg
MD7	0	Normal operation	CR00_15
	1	Force suspend mode if suspend mode is enabled	
MD6	0	Suspend mode is disabled	CR00_14
	1	Suspend mode is enabled	
MD5	0	Isochronous handshake phase is enabled	CR00_13
	1	Isochronous handshake phase is disabled	
MD4	0	Internal RCV comes from SIE	CR00_12
	1	Internal RCV comes from USB Transceiver	
MD3	0	PLL Disable	CR00_11
	1	PLL Enable	
MD2	0	Low Power, Bus-powered Devices	CR00_10
	1	High Power, Bus-powered Devices	
MD1	0	EDO DRAM	CR00_9
	1	SDRAM	
MD0	0	256Kx DRAM	CR00_8
	1	1Mx DRAM	

5 SYSTEM DIAGRAM

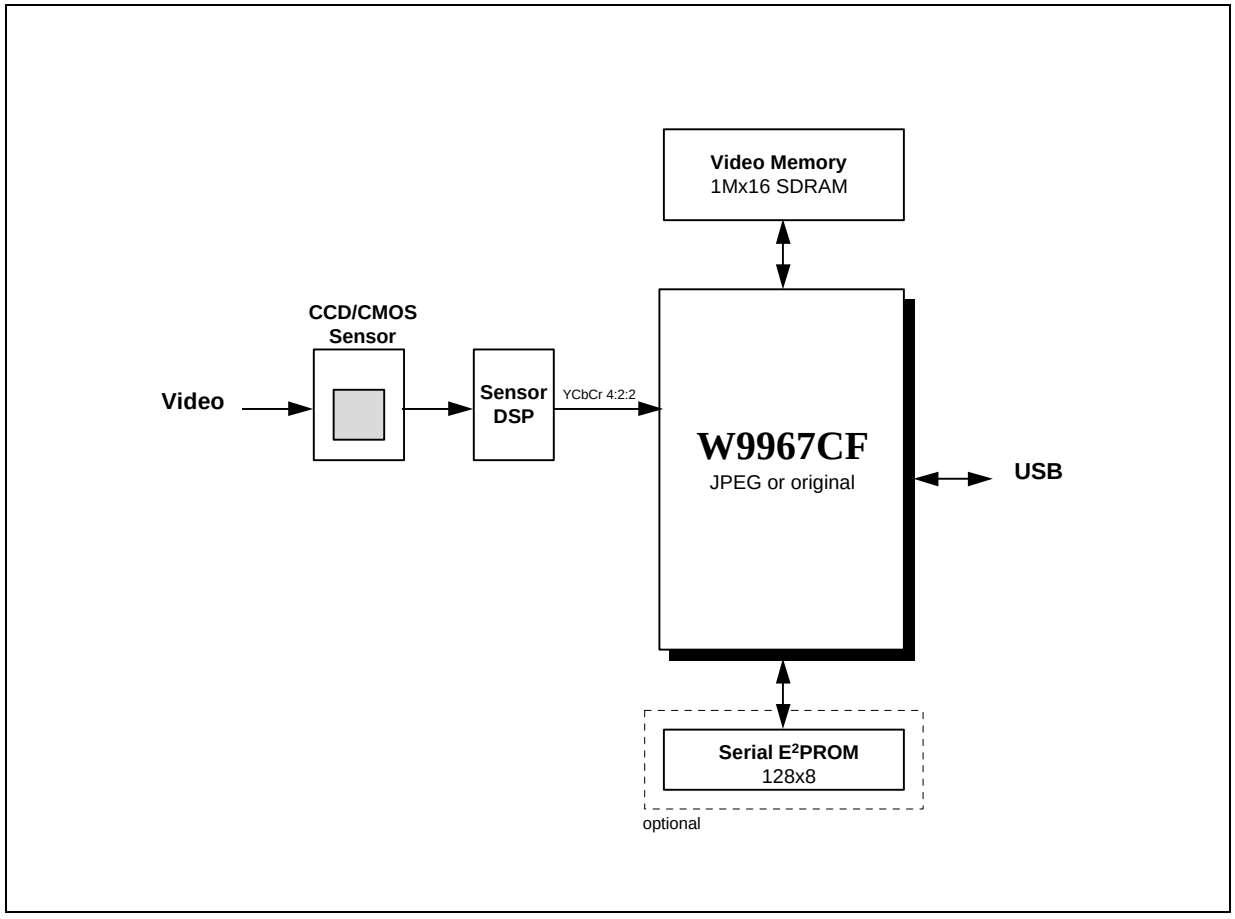


Figure 5.1 W9967CF-Based USB Digital Video Camera System Diagram

6 BLOCK DIAGRAM

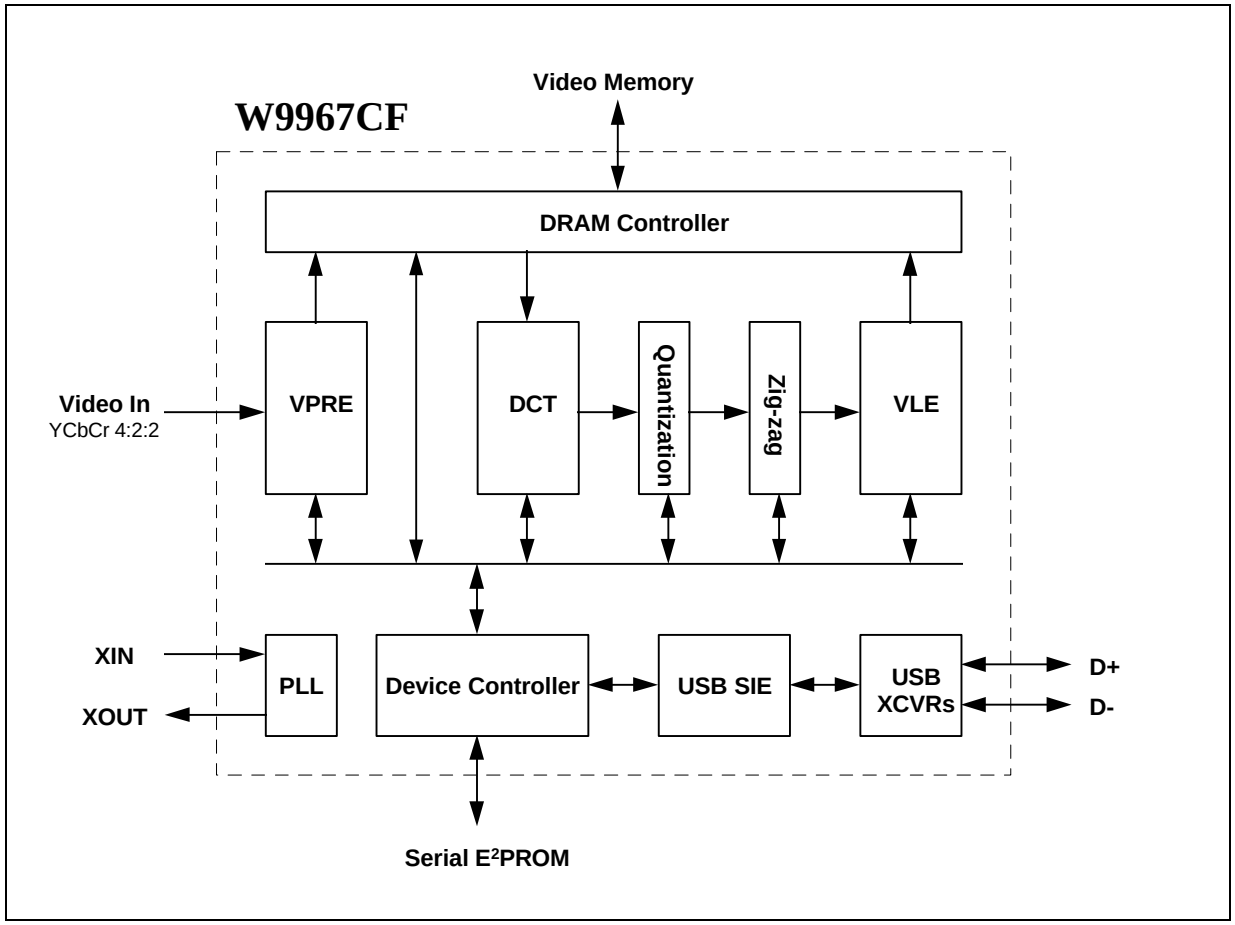


Figure 6.1 W9967CF Block Diagram

7 FUNCTIONAL DESCRIPTION

7.1 Video Input Interface

Video input data is cropped, down-scaled, and filtered in the video pre-processing (VPRE) block, then is stored into the DRAM as captured video for the following JPEG compression and transfer.

7.1.1 Camera Control Serial Bus

A dedicated programmable serial bus is supported for camera control. The serial bus includes SCLK, SDATA, and SDE#/SDS signals. During serial bus read, these signals are controlled by the host via bits 4-0 of the Serial Bus Control register (CR01_4-0).

There are two serial bus write modes which are controlled by bit 5 of the Serial Bus Control register (CR01_5).: normal serial bus write mode (CR01_5 = 0) and fast serial bus write mode (CR01_5 = 1).

Normal serial bus write mode (CR01_5 = 0): SDATA and SCLK signals are output from CR01_1-0 directly.

Fast serial bus write mode (CR01_5 = 1): SDATA and SCLK signals are output from CR06-CR09 in about 400 Khz bit frequency.

7.1.2 Input Video Data Format

The W9967CF accepts video data in YUV 4:2:2 format through a 16-bit (Y[7:0] and UV[7:0]) or 8-bit (Y[7:0]) data bus. Many YUV ordering formats are supported which are selected by bits 9-8 of the Video Capture Control register (CR26) as shown in Figure 7.1. Video data can be latched by the W9967CF by using either rising-edge or falling-edge of the VICLK clock signal. In the 8-bit modes the VICLK frequency is twice the pixel rate, only Y[7:0] pins are used for video data input and UV[7:0] pins are not used.

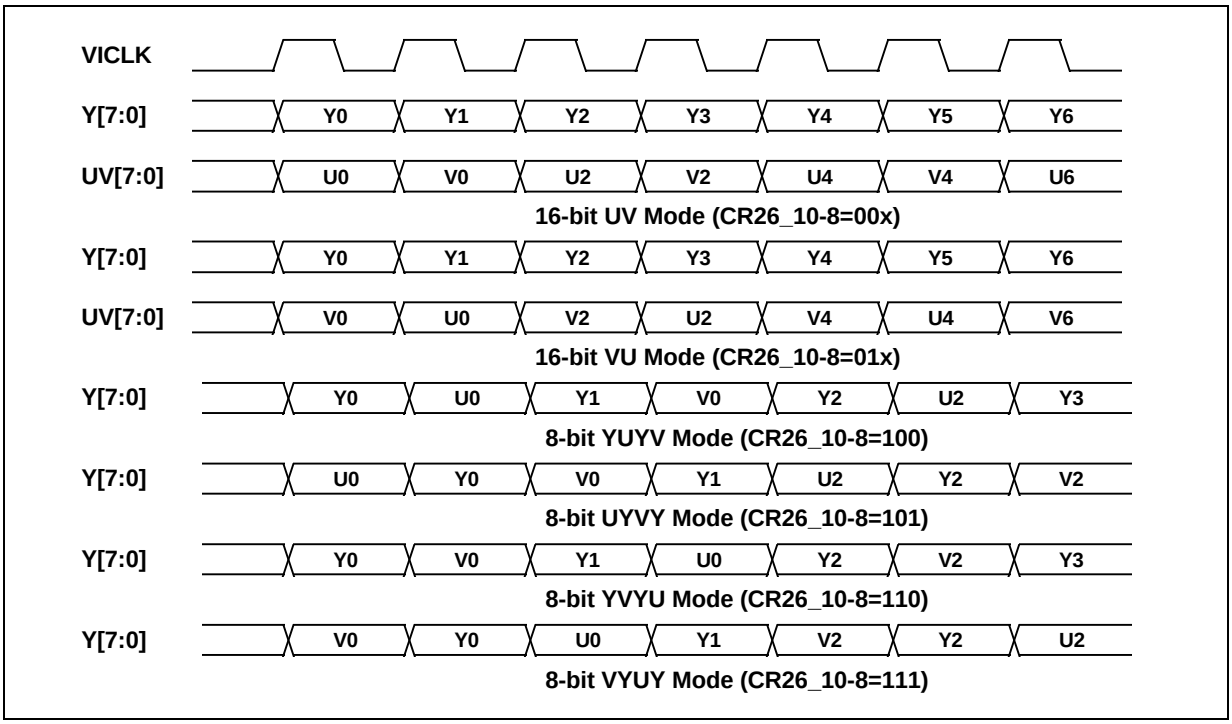


Figure 7.1 Input Video Data Formats

7.1.3 Cropping

A cropping rectangle (or window) is supported for cropping or clipping the incoming video data. Only interested video data located inside the cropping rectangle is processed and sent to the host system. The cropping rectangle can be moved within the input rectangle by programming the Cropping Window Start X and Cropping Window Start Y registers. Cropping is performed based on the VS signal for vertical cropping and HS signal for horizontal cropping. Both VS and HS are programmable polarity for maximum flexibility.

7.1.4 Scaling

The cropped video can be down-scaled horizontally and/or vertically. The horizontal down-scaling and vertical down-scaling are performed independently by using two DDAs (Digital Differential Accumulator) with

$$\text{Horizontal Down-scaling Factor} = \left(\frac{\text{Captured Video Width}}{\text{Cropping Window End X} - \text{Cropping Window Start X}} \right) \text{ and}$$

$$\text{Vertical Down-scaling Factor} = \left(\frac{\text{Captured Video Height}}{\text{Cropping Window End Y} - \text{Cropping Window Start Y}} \right).$$

The W9967CF does not perform up-scaling during video pre-processing. To produce CIF format from 240-line video for the JPEG compression, a special vertical up-scaling can be performed by the JPEG encoder. For the original video transfer, the CIF format from 240-line video can be produced

by the software driver.

7.1.5 Filtering

A 3-tap or 5-tap FIR filter is used to reduce noise and aliasing artifacts produced by the CCD or CMOS sensor, and the scaling process.

7.1.6 Captured Video Data Format

After cropped, down-scaled, and filtered in the video pre-processing (VPRE) block, the input video is stored into the DRAM as captured video. Four different formats are supported for the captured video: YUV4:2:2 packed, YUV4:2:0 packed, YUV4:2:2 planar, and YUV4:2:0 planar modes, which are selected by bits 1-0 of the Video Capture Control register (CR26) as described in Table 7.1. YUV4:2:2 and YUV4:2:0 packed modes are used for original video transfer, while YUV4:2:2 and YUV4:2:0 planar modes are used for JPEG compression video transfer.

Table 7.1 Captured Video Data Format

CR26_1-0	Captured Video Data Format
00	YUV4:2:2 packed mode for original video transfer
01	YUV4:2:0 packed mode for original video transfer
10	YUV4:2:2 planar mode for JPEG compression video transfer
11	YUV4:2:0 planar mode for JPEG compression video transfer

7.2 DRAM Control and Interface

The W9967CF supports 256K×16 and 1M×16 SDRAM or EDO DRAM in a 0.5 ~ 4 Mbytes configuration with 16-bit data bus. A single 1M×16, -15 or above, SDRAM is recommended for better cost/performance.

7.2.1 DRAM Access Arbitration

The DRAM arbiter helps to maximize performance by orchestrating memory access requests from internal engines. Two priority levels are defined for these requests:

- First priority: DRAM refresh request and SDRAM mode register write request
- Second priority: Capture FIFO write request, DCT read request, VLE read request, VLE FIFO write request, USB FIFO read request, and USB control read/write request

Programmable FIFO status are provided by the Capture FIFO, VLE FIFO, and USB FIFO such that the DRAM Controller arbitrates according to these FIFO status to prevent any video data loss and to achieve the best performance.

7.2.2 DRAM Interface

The DRAM controller provides many programmable controls for the DRAM operations which include:

- DRAM Type: supports SDRAM and EDO DRAM
- DRAM Address: programmable 9-bit (256K× EDO DRAM), 10-bit (1M× EDO DRAM or 256K× SDRAM), and 12-bit (1M× SDRAM) address
- DRAM Timing: adjustable Trp, Trcd, Tras, and Tcas timings
- DRAM Refresh: 1 ~ 8 refresh cycles per scan line
- SDRAM Read Latency: 1 ~ 3 clocks
- SDRAM Burst Type: sequential or interleaved
- SDRAM Burst Length: 1, 2, 4, 8, or full page
- SDRAM Self Refresh

Table 7.2 shows the interface signals for SDRAM and EDO DRAM.

Table 7.2 SDRAM and EDO DRAM Interface Signals

Pin Name	256K´ EDO DRAM	1M´ EDO DRAM	256K´ SDRAM	1M´ SDRAM
MD[15:0]	MD[15:0]	MD[15:0]	MD[15:0]	MD[15:0]
MA[10:0]	MA[8:0]	MA[9:0]	MA[8:0]	MA[10:0]
BA			BA	BA
RAS[1:0]#/CS[1:0]#	RAS[1:0]#	RAS[1:0]#	CS[1:0]#	CS[1:0]#
CAS[1:0]#/DQM[1:0]	CAS[1:0]#	CAS[1:0]#	DQM[1:0]	DQM[1:0]

OE#/CKE	OE#	OE#	CKE	CKE
WE#	WE#	WE#	WE#	WE#
SRAS#			SRAS#	SRAS#
SCAS#			SCAS#	SCAS#
SMCLK			SMCLK	SMCLK

7.3 JPEG Compression

The W9967CF supports JPEG baseline sequential process for video data compression. For the sequential DCT-based mode, 8×8 sample blocks are typically input block by block from left to right, and block-row by block-row from top to bottom. Each block is transformed by the forward DCT (FDCT) into a set of 64 values referred to as DCT coefficients. Each of the 64 coefficients is then quantized using one of 64 corresponding values from a quantization table. After quantization, the DC coefficients and the 63 AC coefficients are converted into a one-dimensional zig-zag sequence, then are passed to a Huffman encoder for entropy encoding procedure which compresses the data further.

7.3.1 Level Shift and Forward DCT

Prior to computing the FDCT the input data are level shifted to a signed two′s complement representation. For 8-bit precision the level shift is achieved by subtracting 128. The following equation specifies the mathematical definition of the FDCT.

$$S_{vu} = \frac{1}{4} C_u C_v \sum_{x=0}^{7} \sum_{y=0}^{7} s_{yx} \cos\frac{(2x+1)up}{16} \cos\frac{(2y+1)vp}{16}$$

where

$$C_u, C_v = 1/\sqrt{2} \text{ for u, v = 0}$$
$$C_u, C_v = 1 \text{ otherwise}$$

7.3.2 Quantization

After the FDCT is computed for a block, each of the 64 resulting DCT coefficients is quantized by a uniform quantizer. The uniform quantizer is defined by the following equation. Rounding is to the nearest integer:

$$Sq_{vu} = round\left(\frac{S_{vu}}{Q_{vu}}\right)$$

The quantizer step size for each coefficient S_{vu} is the value of the corresponding element Q_{vu} from the quantization table. The W9967CF supports two programmable quantization tables, luminance quantization table and chrominance quantization table, which are made by two internal 64×8 SRAMs, and which should be loaded by the host via the USB bus before start of the JPEG compression.

The quantized DCT coefficient values are signed, two′s complement integers with 11-bit precision for 8-bit input precision.

7.3.3 Huffman Encoding

After quantization, the quantized coefficients are converted to the zig-zag sequence for Huffman

encoding. The DC coefficients are coded differently from the AC coefficients. The value that should be encoded is the difference (DIFF) between the quantized DC coefficient of the current block (DC_i which is also designated as Sq_{00}) and that of the previous block of the same component (PRED):

$$DIFF = DC_i - PRED$$

At the beginning of the scan and at the beginning of each restart interval, the prediction for the DC coefficient prediction is initialized to 0.

For the AC coefficient encoding, since many AC coefficients are zero, runs of zeros are identified and coded efficiently. In addition, if the remaining coefficients in the zig-zag sequence order are all zero, this is coded explicitly as an end-of-block (EOB).

The W9967CF Huffman encoder employs two DC and two AC Huffman tables within one scan for luminance and chrominance components.

7.3.4 JPEG Encoding Order

The W9967CF JPEG encoder supports two non-interleaved encoding orders shown in Figure 7.2:

- YUV4:2:2 non-interleaved encoding order
- YUV4:2:0 non-interleaved encoding order

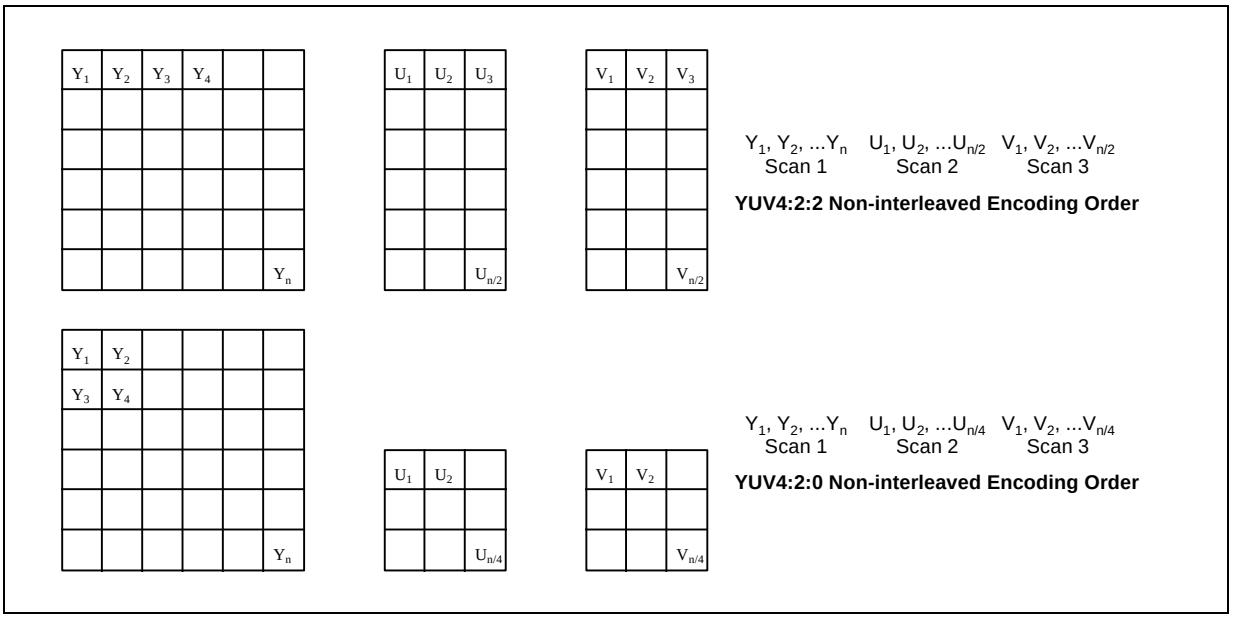


Figure 7.2 JPEG Encoding Order

7.4 USB Interface and Device Control

The W9967CF contains two endpoints: default and Video Data-In endpoints. Figure 7.3 shows the device configuration for the W9967CF-based USB digital video camera.

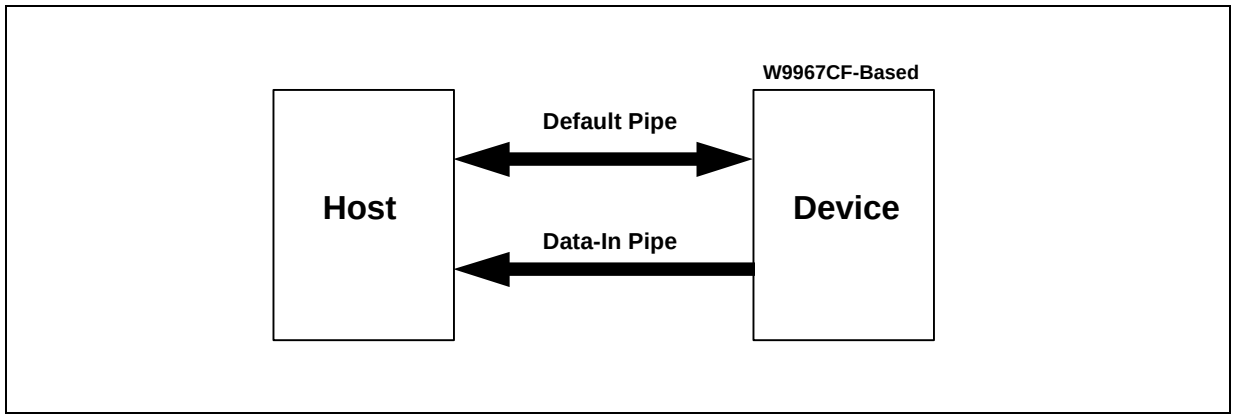


Figure 7.3 Device Configuration

7.4.1 Endpoints

7.4.1.1 Default Endpoint (Endpoint 0)

The default endpoint uses control transfers as defined in the USB specification. The default endpoint provides access to the W9967CF-based device′s configuration, status, and control information by sending standard, class, and vendor-specific requests to the device, an interface, or an endpoint.

7.4.1.2 Video Data-In Endpoint (Endpoint 1)

The Video Data-In endpoint is used to receive video image data from the device intended for delivery to a video capture application on the host. The Video Data-In endpoint uses isochronous transfers. The direction is always IN. The maximum packet size can be varied for different alternate settings for limited USB bandwidth.

7.4.2 USB Device Requests

The W9967CF responds to requests from the host on the default pipe. The W9967CF supports standard, class, and vendor-specific USB device requests.

7.4.2.1 Standard Device Requests

The W9967CF supports the standard USB device requests as shown in Table 7.3 and described below. It responds to standard device requests whether it has been assigned a non-default address or is currently configured. If any unrecognized or unsupported standard request is received, it returns STALL.

Table 7.3 Standard Device Requests

bmRequestType	bRequest	wValue	wIndex	wLength	Data
00000010B	CLEAR_FEATURE (1)	Feature Selector (0)	Endpoint	Zero	None
10000000B	GET_CONFIGURATION (8)	Zero	Zero	One	Configurati-on Value
10000000B	GET_DESCRIPTOR (6)	Descriptor Type and Descriptor Index	Zero or Language ID	Descriptor Length	Descriptor
10000001B	GET_INTERFACE (10)	Zero	Interface (0)	One	Alternate Setting
10000000B 10000001B 10000010B	GET_STATUS (0)	Zero	Zero Interface Endpoint	Two	Device, Interface, or Endpoint Status
00000000B	SET_ADDRESS (5)	Device Address	Zero	Zero	None
00000000B	SET_CONFIGURATION (9)	Configura -tion Value	Zero	Zero	None
00000000B	SET_DESCRIPTOR (7) (Not Supported)				
00000010B	SET_FEATURE (3)	Feature Selector (0)	Endpoint	Zero	None
00000001B	SET_INTERFACE (11)	Alternate Setting	Interface (0)	Zero	None
00000010B	SYNCH_FRAME (12) (Not Supported)				

Clear Feature The W9967CF supports the following Clear Feature request:

- When directed to an endpoint recipient for ENDPOINT_STALL

The W9967CF returns STALL if any unrecognized or unsupported Clear Feature request is received.

Get Configuration The W9967CF returns zero if it is unconfigured or the bConfiguration value defined in the Configuration Descriptor is configured.

Get Descriptor The W9967CF supports Get Descriptor requests for standard descriptors (Device, Configuration, and String). The W9967CF returns STALL if a Get Descriptor request is

received for a class-specific descriptor or a vendor-specific descriptor, is unrecognized or unsupported.

Get Interface The W9967CF supports a Get Interface request for Interface 0 by returning the selected alternate setting. The default alternate setting is zero. The W9967CF returns STALL for a Get Interface request for any other Interface or any Get Interface request before the Device is configured.

Get Status The W9967CF supports a Get Status directed at the device, Interface 0, or any defined endpoint (default or Video Data-In). The W9967CF returns STALL if a Get Status request is received for Interface 0 or any defined endpoint before the Device is configured, or if a Get Status request is received for any unrecognized or unsupported recipient.

Set Address The W9967CF supports a Set Address request to change the Device Address from the default address (zero) to a unique address.

Set Configuration The W9967CF supports Set Configuration requests to set the Device Configuration to zero (unconfigured) or the bConfiguration value defined in the Configuration Descriptor. The W9967CF returns STALL if a Set Configuration request is received with any other value.

Set Descriptor The W9967CF does not support update for any defined Descriptor (Device, Configuration, Interface, Endpoint, or String). It returns STALL for any Set Descriptor request.

Clear Feature The W9967CF supports the following Set Feature request:

- When directed to an endpoint recipient for ENDPOINT_STALL

The W9967CF returns STALL if any unrecognized or unsupported Set Feature request is received.

Set Interface When configured, the W9967CF supports a Set Interface request to Interface 0 for defined Alternate Settings. This request allows the host to select the desired alternate setting. The W9967CF returns STALL for any other Set Interface request.

Synch Frame The W9967CF returns STALL for any Synch Frame request.

7.4.2.2 Video Camera Class-Specific Requests

Currently, there is no class-specific request is defined for the video camera devices. The W9967CF returns STALL for any class-specific request.

7.4.2.3 Vendor-Specific Requests

The W9967CF supports two vendor-specific requests for the control registers In/Out transfers on the default pipe (Endpoint 0): Get W9967CF Control and Set W9967CF Control. The vendor-specific requests defined for the W9967CF are shown in Table 7.4. The W9967CF returns STALL if an unrecognized or unsupported vendor-specific request is received.

Table 7.4 W9967CF Vendor-Specific Requests

bmRequestType	bRequest	wValue	wIndex	wLength	Data
11000000B	GET_W9967CF_CONTROL (1)	Zero	Index[1]	Length[2]	Data
01000000B	SET_W9967CF_CONTROL (0)	Data0[3]	Index[1]	Length[2]	Data

Note 1. Index specifies the starting index of the control registers to be accessed. An index counter, loaded with the Index value, will be incremented by one after every two bytes of data transferred.
Note 2. Length specifies number of data bytes transferred during the second phase of the control transfer. It should be an even number value. If this field is zero, there is no data transfer phase.
Note 3. Data0 is a word-sized data to be programmed into the control register indexed by the Index field, no matter the Length field is zero or not. The internal index counter will be incremented by one once Data0 is transferred.

Get W9967CF Control The W9967CF supports a Get W9967CF Control request for W9967CF control registers IN transfer. Length field should be an even number value. The W9967CF returns STALL for any unrecognized or unsupported Get W9967CF Control request.

Set W9967CF Control The W9967CF supports a Set W9967CF Control request for W9967CF control registers OUT transfer. Length field should be an even number value. If the Length field is zero, only Data0 is transferred with no data transfer phase. The W9967CF returns STALL for any unrecognized or unsupported Set W9967CF Control request.

7.4.3 Descriptors

The W9967CF supports the standard USB descriptors as described below. The W9967CF returns STALL if a request is received for any unrecognized or unsupported standard descriptor.

7.4.3.1 Device Descriptors

The W9967CF returns a Device Descriptor with the values shown in Table 7.5.

Table 7.5 W9967CF Device Descriptor

Offset	Field	Size	Value	Description
0	*bLength*	1	0x12	Size of this descriptor in bytes
1	*bDescriptorType*	1	0x01	Device Descriptor Type
2	*bcdUSB*	2	0x0110	USB Specification Release Number in BCD
4	*bDeviceClass*	1	0x00	Class code
5	*bDeviceSubClass*	1	0x00	Subclass code
6	*bDeviceProtocol*	1	0x00	Protocol code
7	*bMaxPacketSize0*	1	0x08	Maximum packet size for endpoint zero
8	*idVendor*	2	0x1046	Vendor ID
10	*idProduct*	2	0x9967	Product ID

12	*bcdDevice*	2	0x0110	Device release number in BCD
14	*iManufacturer*	1	0x01	Index of string descriptor describing manufacturer
15	*iProduct*	1	0x02	Index of string descriptor describing product
16	*iSerialNumber*	1	0x00	Index of string descriptor describing the device's serial number
17	*bNumConfigurations*	1	0x01	Number of possible configurations

Note 1. Vendor ID and Product ID will be replaced with bytes 0-3 of an external serial E^2PROM if present.

7.4.3.2 Configuration Descriptors

The W9967CF returns a Configuration Descriptor and other configuration related descriptors as described below. When the host requests the Configuration Descriptor, all related interface and endpoint descriptors are returned.

Table 7.6 W9967CF Configuration Descriptor

Offset	Field	Size	Value	Description
0	*bLength*	1	0x09	Size of this descriptor in bytes
1	*bDescriptorType*	1	0x02	Configuration Descriptor Type
2	*wTotalLength*	2	0x0119	Total length of data returned for this configuration. Includes the combined length of all descriptors returned for this configuration.
4	*bNumberInterfaces*	1	0x01	Number of interfaces supported by this configuration
5	*bConfigurationValue*	1	0x01	Value used as an argument to Set Configuration to select this configuration
6	*iConfiguration*	1	0x00	No configuration string
7	*bmAttributes*	1	0x80	Configuration characteristics
8	*Maxpower*	1	0xFA or 0x32 (Note 1)	Maximum power consumption from the bus when the device is fully operational. Expressed in 2 mA units.

Note 1. Value of this field is 0xFA (500 mA) for high power devices (CR00_10 = 1), or 0x32 (100 mA) for low power devices (CR00_10 = 0).

Table 7.7 W9967CF Video Interface Descriptor

Offset	Field	Size	Value	Description
0	*bLength*	1	0x09	Size of this descriptor in bytes
1	*bDescriptorType*	1	0x04	Interface Descriptor Type
2	*bInterfaceNumber*	1	0x00	Number of interface

3	*bAlternateSetting*	1	0x00	Default alternate setting zero
4	*bNumEndpoints*	1	0x01	Number of endpoints used by this interface
5	*bInterfaceClass*	1	0x00	Image interface class code
6	*bInterfaceSubClass*	1	0x00	Digital Video Camera subclass code
7	*bInterfaceProtocol*	1	0x00	Protocol code. No class specific protocol.
8	*iInterface*	1	0x00	No interface string

Table 7.8 W9967CF Data-In Endpoint Descriptor

Offset	Field	Size	Value	Description
0	*bLength*	1	0x07	Size of this descriptor in bytes
1	*bDescriptorType*	1	0x05	Endpoint Descriptor Type
2	*bEndpointAddress*	1	0x81	Endpoint number. Direction is set to IN.
3	*bmAttributes*	1	0x01	Isochronous transfer type
4	*wMaxPacketSize*	2	0x00	Default zero bandwidth
6	*bInterval*	1	0x01	Interval in milliseconds for polling endpoint for data transfers

The W9967CF Video interface includes 16 alternate settings that allow the Data-In endpoint bandwidth to be varied decreasingly from 8 Mbps down to 0.5 Mbps in descending 0.5 Mbps steps such that the device driver can request subsequently smaller bandwidth quantities. A separate interface descriptor and its associated endpoint are included for each setting. When the host requests the Configuration Descriptor, all 16 pairs of interface and endpoint descriptors for alternate setting should follow the interface and endpoint descriptors for the default alternate setting zero.

The W9967CF supports the Get Interface and Set Interface requests to report or select a specific alternate setting for the Video interface.

Table 7.9 W9967CF Video Interface Alternate Setting 1-16 Interface Descriptor

Offset	Field	Size	Value	Description
0	*bLength*	1	0x09	Size of this descriptor in bytes
1	*bDescriptorType*	1	0x04	Interface Descriptor Type
2	*bInterfaceNumber*	1	0x00	Number of interface
3	*bAlternateSetting*	1	1-16 (Note 1)	Alternate setting 1-16 for this interface
4	*bNumEndpoints*	1	0x01	Number of endpoints used by this interface
5	*bInterfaceClass*	1	0x00	Image interface class code

6	*bInterfaceSubClass*	1	0x00	Digital Video Camera subclass code
7	*bInterfaceProtocol*	1	0x00	Protocol code. No class specific protocol.
8	*iInterface*	1	0x00	No interface string

Note 1. Refer to Table 7.11.

Table 7.10 W9967CF Alternate Setting 1-16 Data-In Endpoint Descriptor

Offset	Field	Size	Value	Description
0	*bLength*	1	0x07	Size of this descriptor in bytes
1	*bDescriptorType*	1	0x05	Endpoint Descriptor Type
2	*bEndpointAddress*	1	0x81	Endpoint number. Direction is set to IN.
3	*bmAttributes*	1	0x01	Isochronous transfer type
4	*wMaxPacketSize*	2	Note 1	Maximum packet size of this alternate setting
6	*bInterval*	1	0x01	Interval in milliseconds for polling endpoint for data transfers

Note 1. Refer to Table 7.11.

Table 7.11 shows *bAlternateSetting* fields and *wMaxPacketSize* fields for these alternate settings.

Table 7.11 The Maximum Data Payload Size in Bytes for Alternate Settings

Alternate Setting	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
bAlternateSetting	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
wMaxPacketSize	1023	959	895	831	767	703	639	575	511	447	383	319	255	191	127	63

7.4.3.3 String Descriptors

The W9967CF includes strings describing the manufacturer and product as shown in Table 7.12.

Table 7.12 W9967CF Default Stream Descriptors

Offset	Field	Size	Value	Description
0	*bLength*	1	0x04	Length of String descriptor in bytes
1	*bDescriptorType*	1	0x03	String Descriptor Type
2	*bString*	2	0x0409	Array of two-byte LangID codes (English American)
4	*bLength*	1	0x10	Length of String descriptor in bytes
5	*bDescriptorType*	1	0x03	String Descriptor Type
6	*bString*	14	WINBOND	Manufacturer
20	*bLength*	1	0x10	Length of String descriptor in bytes
21	*bDescriptorType*	1	0x03	String Descriptor Type

22	*bString*	14	W9967CF	Product

7.5 Video/Still Image Data Transfer

Video or still image data from the device is delivered to the host system through an isochronous pipe (Endpoint 1). The maximum packet size can be varied for different alternate settings for limited USB bandwidth for other USB devices.

7.5.1 Output Video Data Format

The W9967CF supports two video transfer modes: original video transfer mode and JPEG compression video transfer mode. The captured video stored in the DRAM will be compressed by the JPEG encoder and then transferred to the host if JPEG compression video transfer mode is selected, or will be directly transferred to the host if original video transfer mode is selected. Four different formats are supported for the output video which are selected by bits 1-0 of the Video Capture Control register (CR26) and bits 1 of the JPEG Encoder Control register (CR39) as described in Table 7.13.

Table 7.13 Output Video Data Format

CR39_1	CR26_1-0	Output Video Data Format
0	00	Original YUV4:2:2 packed mode
0	01	Original YUV4:2:0 packed mode
1	0X	Reserved
1	10	JPEG YUV4:2:2 non-interleaved scan mode
1	11	JPEG YUV4:2:0 non-interleaved scan mode

7.5.2 Video Frame Synchronization

A single video frame typically requires multiple USB packets. One or more zero length isochronous data packets are used to mark the end of a video frame. The first non-zero data packet is the start of the next video frame.

If an error is encountered during the reception of a USB packet, the host may discard the entire video frame. Processing begins again with the next video frame as indicated by the first non-zero length isochronous data packet after one or more zero-length packet.

7.5.3 Bandwidth Management

The W9967CF provides for varying the bandwidth required by providing a zero-bandwidth interface (alternate setting zero) and 16 alternate settings interfaces with 8 Mbps down to 0.5 Mbps bandwidth in descending 0.5 Mbps steps. The default alternate setting zero (with zero bandwidth) selected by a Set Configuration request allows a video camera to be initially configured even on a highly utilized USB bus. Before the device begins streaming video data, the host software must select an alternate setting with the appropriate amount of bandwidth by using the Set Interface request.

7.6 Power Management

The W9967CF provides three output pins as described below for the video camera power management to meet the USB specification requirements.

- **PWRDWN/PWRDWN#**: These pins, when active, are used to turn off the USB 5V power supply to the video source circuits (CCD/CMOS sensor device, ADC, DSP, video decoder, etc.).
- **SUSPND**: This pin, when active, is used to turn off the 3.3V power supply to the W9967CF (excluding USBVDD pin, the power supply for the transceiver), DRAM, and E^2PROM.

Bit 10 of the Miscellaneous Control register (CR00) determines whether the W9967CF-based device is a high power device or a low power device as described below:

- **CR00_10 = 1**: High power, bus-powered devices. They must draw no more than 100 mA upon power up and may draw up to 500 mA after being configured.
- **CR00_10 = 0**: Low power, bus-powered devices. May draw up to 100 mA from their upstream connection to allow the interface to function when the remainder of the hub is powered down.

7.6.1 W9967CF Reset

The W9967CF has two reset sources: system reset from the input RSTIN# pin, and the USB reset detected by seeing a single-ended zero (SE0) for more than 2.5 us. All reset sources are joined inside the W9967CF into a single reset signal which initializes the W9967CF and is also output via the RSTOUT pin to initialize other external circuits.

Reset can wake the W9967CF from the suspended mode (SUSPND is inactive low) and turn off the USB 5V power supply to the video source circuits (PWRDWN is active high and PWRDWN# is active low).

7.6.2 Before Configured

Before configured, the W9967CF should be reset and keep PWRDWN and PWRDWN# to be active (CR00_4 = 0) such that the W9967CF-based devices will not draw more than 100 mA from the USB bus power supply. It is required that an external power-on reset should be applied to the RSTIN# pin before any USB transaction is sent to the W9967CF by the host.

7.6.3 After Configured

After configured, PWRDWN and PWRDWN# pins should be inactive by programming the Camera Power-on Control register to one (CR00_4 = 1) to enable device functions. The W9967CF-based devices must draw less than 100 mA (CR00_10 = 0) or 500 mA (CR00_10 = 1) from the bus during normal operation. The SOF (Start of Frame) packet is guaranteed to occur once a frame to keep full speed devices awake during normal bus operation.

7.6.4 Suspend

The W9967CF goes into the suspend mode from any powered state when it sees a constant idle state on the USB bus lines for more than 3.0 ms. When suspended, both SUSPND and PWRDWN are active high, PWRDWN# is active low, and the Camera Power-on Control register is cleared to zero (CR00_4 = 0). The W9967CF-based devices must draw less than 500 uA from the bus when suspended.

7.6.5 Resume

Once the W9967CF is in the suspended state, it can be resumed by receiving non-idle signaling on the bus. SUSPND will be inactive low when resumed. PWRDWN and PWRDWN# will remain active until the Camera Power-on Control register is set to one (CR00_4 = 1) by the host.

7.7 Serial EEPROM Interface

The W9967CF supports an external 1K (128×8) serial E^2PROM as an optional source for IHV-specific Vendor ID and Product ID. The external E^2PROM data, in stead of the default data, will be used when a high is sampled at SDA pin (pin 49) during a reset operation.

7.7.1 EEPROM Data Structure

The E^2PROM contains IHV-specific Vendor ID and Product ID as described in Table 7.14.

Table 7.14 EEPROM Data Structure

Address	Field	Size	Value	Description
0x00		2	TL	Total length of E^2PROM data to be returned
0x02	*idVendor*	2		Vendor ID
0x04	*idProduct*	2		Product ID

7.7.2 EEPROM Operations

The external E^2PROM will be only read right after a reset operation. TL (defined in address 0x00) bytes of data will be read by using a sequential read operation.

START condition: A high-to-low transition of SDA with SCL high is a start condition which must proceed any other command.

STOP condition: A low-to-high transition of SDA with SCL high is a stop condition which terminates all communications. After a read sequence, the stop command will place the E^2PROM in a standby power mode.

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the E^2PROM in 8-bit words. The E^2PROM will acknowledge by pulling SDA low after receiving each address. The W9967CF will likewise acknowledge by pulling SDA low after receiving each data word. This must happen during the ninth clock cycle after each word received and after all other devices have freed the SDA bus.

Refer to Figure 7.4, a sequential read is initiated by the W9967CF with a start condition followed by a 7-bit data word address (always 0) and a high read bit. The E^2PROM will respond with an acknowledge and then serially output 8 data bits. After the W9967CF receives an 8-bit data word, it responds with an acknowledge. As long as the E^2PROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. The sequential read operation is terminated when the memory address limit (TL) is reached and the W9967CF does not respond with an acknowledge but does generate a following stop condition.

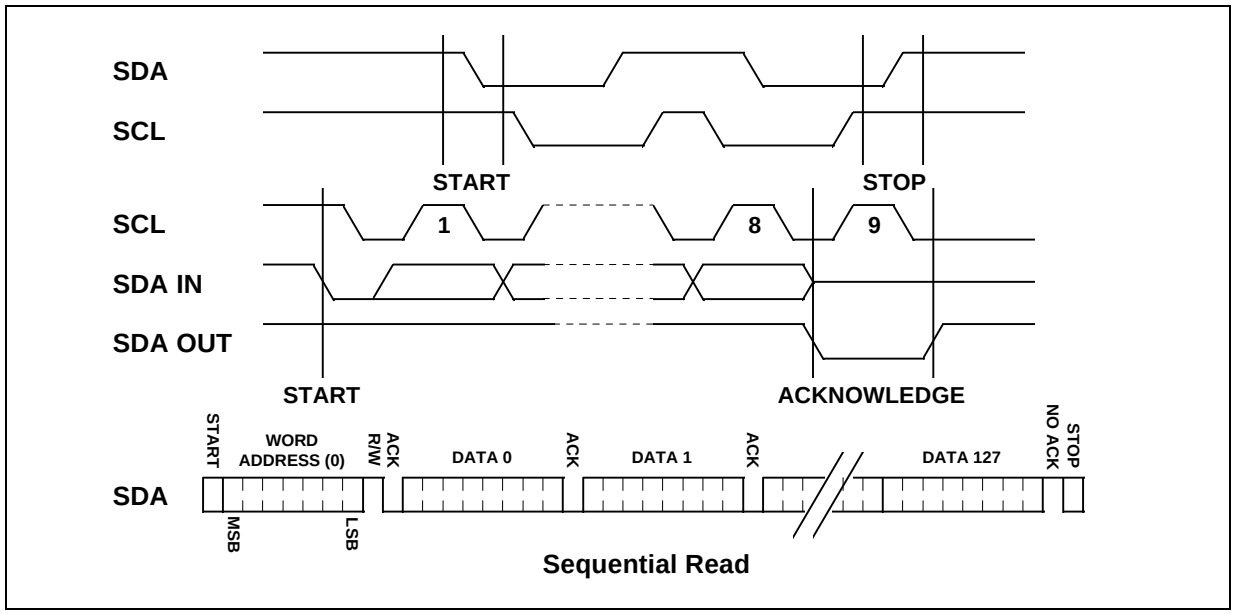


Figure 7.4 EEPROM Timing Diagram

8 CONTROL AND STATUS REGISTERS

The internal W9967CF control registers can be accessed by performing one of the two vendor-specific requests on the default pipe (Endpoint 0): Get W9967CF Control for read access and Set W9967CF Control for write access. All W9967CF control registers are 16-bit wide and can be accessed in WORD only. Table 8.1 shows the control register map.

Table 8.1 W9967CF Control Register Map

Index	Symbol	Description
0000H	CR00	Miscellaneous Control Register
0001H	CR01	Serial Bus Control Register
0002H	CR02	General I/O Port Control Register
0003H	CR03	DRAM Timing Control Register
0004H	CR04	SDRAM Control Register
0005H	CR05	Memory Controller Test Mode Control Register
0006H	CR06	Fast Serial Bus Control Register 0
0007H	CR07	Fast Serial Bus Control Register 1
0008H	CR08	Fast Serial Bus Control Register 2
0009H	CR09	Fast Serial Bus Control Register 3
000AH - 000FH		Reserved
0010H	CR10	Cropping Window Start X Register
0011H	CR11	Cropping Window Start Y Register
0012H	CR12	Cropping Window End X Register
0013H	CR13	Cropping Window End Y Register
0014H	CR14	Captured Video Width Register
0015H	CR15	Captured Video Height Register
0016H	CR16	Video Capture Control Register
0017H	CR17	Video Capture Test Mode Control Register
0018H	CR18	Capture Test Data Register
0019H - 001FH		Reserved
0020H	CR20	Capture Y Frame Buffer 0 Start Address Low Register
0021H	CR21	Capture Y Frame Buffer 0 Start Address High Register
0022H	CR22	Capture Y Frame Buffer 1 Start Address Low Register
0023H	CR23	Capture Y Frame Buffer 1 Start Address High Register

0024H	CR24	Capture U Frame Buffer 0 Start Address Low Register
0025H	CR25	Capture U Frame Buffer 0 Start Address High Register
0026H	CR26	Capture U Frame Buffer 1 Start Address Low Register
0027H	CR27	Capture U Frame Buffer 1 Start Address High Register
0028H	CR28	Capture V Frame Buffer 0 Start Address Low Register
0029H	CR29	Capture V Frame Buffer 0 Start Address High Register
002AH	CR2A	Capture V Frame Buffer 1 Start Address Low Register
002BH	CR2B	Capture V Frame Buffer 1 Start Address High Register
002CH	CR2C	Capture Y Frame Buffer Stride Register
002DH	CR2D	Capture UV Frame Buffer Stride Register
002EH	CR2E	Video Capture Y FIFO Threshold Register
002FH	CR2F	Video Capture UV FIFO Threshold Register
0030H	CR30	Image Maximum Width Register
0031H	CR31	Image Maximum Height Register
0032H	CR32	Compressed Bitstream Buffer 0 Start Address Low Register
0033H	CR33	Compressed Bitstream Buffer 0 Start Address High Register
0034H	CR34	Compressed Bitstream Buffer 1 Start Address Low Register
0035H	CR35	Compressed Bitstream Buffer 1 Start Address High Register
0036H	CR36	Restart Interval Register
0037H	CR37	VLE FIFO Threshold Register
0038H	CR38	Vertical Up-scaling Control Register
0039H	CR39	JPEG Encoder Control Register
003AH	CR3A	JPEG Image Size Low Register
003BH	CR3B	JPEG Image Size High Register
003CH	CR3C	USB FIFO Enable and Threshold Register
003DH	CR3D	USB Isochronous Transfer Size Low Register
003EH	CR3E	USB Isochronous Transfer Size High Register
003FH	CR3F	JPEG/MCTL Test Data Register
0040H - 005FH	CR40 - CR5F	JPEG Luminance Quantization Table Registers
0060H - 007FH	CR60 - CR7F	JPEG Chrominance Quantization Table Registers

8.1 General Control Registers

Miscellaneous Control Register (CR00)

Read/Write Index: 0000H

Power-on Default: FF00H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FS	SUS	ISO	RCV	PLL	BP	Type	MS	24M	Reserved		PWR	R	JR	UR	MR

Bit 15 Force Suspend Mode (It reflects status of the MD7 pin upon reset)
0 = Force suspend mode when suspend mode is enabled (CR00_14 = 1)
1 = Normal operation

Bit 14 Suspend Mode Enable (It reflects status of the MD6 pin upon reset)
0 = Disable
1 = Enable

Bit 13 Isochronous Handshake Phase Support (It reflects status of the MD5 pin upon reset)
0 = Enable
1 = Disable

Bit 12 Differential RCV Source (It reflects status of the MD4 pin upon reset)
0 = Generated by the SIE
1 = Generated by the USB transceiver

Bit 11 PLL Enable (It reflects status of the MD3 pin upon reset)
0 = Disable
1 = Enable

Bit 10 High Power Device (It reflects status of the MD2 pin upon reset)
0 = Low power device
1 = High power device

Bit 9 DRAM Type (It reflects status of the MD1 pin upon reset)
0 = EDO DRAM
1 = SDRAM

Bit 8 DRAM Size (It reflects status of the MD0 pin upon reset)

0 = 256K× DRAM

1 = 1M× DRAM

Bit 7 CLK24M Output Enable

0 = Disable, CLK24M pin is forced to low

1 = Enable

Bits 6-5 Reserved

Bit 4 Camera Power-on Control

0 = Power-down

1 = Power-on

Note. This register will be cleared to zero when suspended.

Bit 3 Reserved

Bit 2 JPEG Encoder Reset

0 = Normal operation

1 = Reset JPEG encoder

Bit 1 USB FIFO Reset

0 = Normal operation

1 = Reset USB FIFO

Bit 0 MD Bus Reset

0 = Normal operation

1 = Reset MD bus (tri-stated)

Serial Bus Control Register (CR01)

Read/Write Index: 0001H

Power-on Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					EEP	R	XTR	Reserved		FSB	SDE	SDR	SCR	SDW	SCW

Bits 15-11 Reserved

Bit 10 External EEPROM Enable (Read-only, it reflects status of the SDA pin upon reset)

0 = Disable

1 = Enable

Bit 9 Reserved

Bit 8 USB Transceiver (It reflects status of the INTXTR pin upon reset)

0 = External transceiver

1 = Internal transceiver

Bits 7-6 Reserved

Bit 5 Fast Serial Bus Enable

0 = Disable, serial bus outputs (SDATA and SCLK) are controlled by CR01_1-0

1 = Enable, serial bus outputs (SDATA and SCLK) are controlled by CR06 - CR09. Once CR09 is programmed, all 32-bit data for SDATA and 32-bit data for SCLK from CR06 - CR09 will be serially output in 400 Khz bit frequency (2.5 us bit time).

Bit 4 Serial Data Enable/Serial Data Strobe

0 = SDE#/SDS pin is driven low

1 = SDE#/SDS pin is driven high

Bit 3 Serial Interface Data Read (Read only)

0 = SDATA is low

1 = SDATA is high

Bit 2 Serial Interface Clock Read (Read only)

0 = SCLK is low

1 = SCLK is high

Bit 1 Serial Interface Data Write

0 = SDATA pin is driven low

1 = SDATA pin is tri-stated

Bit 0 Serial Interface Clock Write

0 = SCLK pin is driven low

1 = SCLK pin is tri-state

General I/O Port Control Register (CR02)

Read/Write Index: 0002H

Power-on Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P7W	P6W	P5W	P4W	P3W	P2W	P1W	P0W	P7D	P6D	P5D	P4D	P3D	P2D	P1D	P0D

Bits 15-8 GPIO[7:0] Direction

0 = Input

1 = Output

Bits 7-0 GPIO[7:0] Data

0 = Low

1 = High

DRAM Timing Control Register (CR03)

Read/Write Index: 0003H

Power-on Default: 405DH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Refresh Cycles			DCT	T_RP		RAS	T_RCD		T_RAS			RE	T_CAS	

Bit 15 Reserved

Bits 14-12 Refresh Cycles

000 = 1 refresh cycle per horizontal scan line

001 = 2 refresh cycles per horizontal scan line

010 = 3 refresh cycles per horizontal scan line

011 = 4 refresh cycles per horizontal scan line

100 = 5 refresh cycles per horizontal scan line

101 = 6 refresh cycles per horizontal scan line

110 = 7 refresh cycles per horizontal scan line

111 = 8 refresh cycles per horizontal scan line

Bit 11 DCT DRAM Data Access

0 = DCT DRAM data access can be interrupted by MCTL when other DRAM request is active.

1 = DCT DRAM data access cannot be interrupted by MCTL.

Bits 10-9 RAS# Precharge Time Control

00 = 2 MCLKs

01 = 3 MCLKs

10 = 4 MCLKs

11 = 5 MCLKs

Bit 8 RAS# Precharge Time Shrink

0 = Not shrink

1 = Shrink by 0.5 MCLK over that specified by bits 10-9 of this register

Bits 7-6 RAS# Low to CAS# Low Time Control

00 = 1 MCLK

01 = 2 MCLKs

10 = 3 MCLKs

11 = 4 MCLKs

Bits 5-3 Refresh Cycle RAS# Low Pulse Width Control

000 ~ 111 = 1 ~ 8 MCLK cycles

Bit 2 RAS# Low Extend

0 = Not extend

1 = Extend 1 MCLK

Bits 1-0 CAS# Low Stretch Control

00 = Not stretch

01 = Stretch approximately 1 ns

10 = Stretch approximately 2 ns

11 = Stretch approximately 3 ns

SDRAM Control Register (CR04)

Read/Write Index: 0004H

Power-on Default: 0030H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									Read Latency			BTyp	Burst Length		

Bits 15-7 Reserved

Bits 6-4 Read Latency

000 = Reserved

001 = 1 clock

010 = 2 clocks

011 = 3 clocks

100 ~ 111 = Reserved

Bit 3 Burst Type

0 = Sequential

1 = Interleaved

Bits 2-0 Burst Length

Bits 2-0	Burst Length	
	Sequential (Bit 3 =0)	Interleaved (Bit 3 = 1)
000	1	1
001	2	2
010	4	4
011	8	8
100	Reserved	Reserved
101	Reserved	Reserved
110	Reserved	Reserved
111	Full Page	Reserved

Memory Controller Test Mode Control Register (CR05)

Read/Write Index: 0005H

Power-on Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TEN	HD	SR	Test	R	MTS		

Bits 15-8 Reserved

Bit 7 Memory Controller Test Mode Enable

0 = Disable

1 = Enable

Bit 6 DRAM Controller Hold Control

0 = Normal operation

1 = Hold DRAM Controller operation

Bit 5 SDRAM Self Refresh

0 = Disable

1 = Enable

Bit 4 SDRAM Delay Test (used for test mode only)

Bit 3 Reserved

Bits 2-0 Memory Controller Test Mode Select

Fast Serial Bus Control Register 0~3 (CR06~CR09)

Read/Write Index: 0006H - 0009H

Power-on Default: 0000H

CR06

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C7	D7	C6	D6	C5	D5	C4	D4	C3	D3	C2	D2	C1	D1	C0	D0

CR07

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C15	D15	C14	D14	C13	D13	C12	D12	C11	D11	C10	D10	C9	D9	C8	D8

CR08

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C23	D23	C22	D22	C21	D21	C20	D20	C19	D19	C18	D18	C17	D17	C16	D16

CR09

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C31	D31	C30	D30	C29	D29	C28	D28	C27	D27	C26	D26	C25	D25	C24	D24

D[31:0] 32-bit data for SDATA output. When fast serial bus is enabled (CR01_5 = 1), D[31:0] will be output serially from LSB to MSB once CR09 is programmed.

C[31:0] 32-bit data for SCLK output. When fast serial bus is enabled (CR01_5 = 1), C[31:0] will be output serially from LSB to MSB once CR09 is programmed.

8.2 Video Input Control Registers

Cropping Window Start X Register (CR10)

Read/Write Index: 0010H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Cropping Window Start X											

Bits 15-10 Reserved

Bits 11-0 Cropping Window Start X

A 12-bit value specifies the number of pixels between the inactive edge of HS and the first cropped video pixel.

Cropping Window Start Y Register (CR11)

Read/Write Index: 0011H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Cropping Window Start Y										

Bits 15-11 Reserved

Bits 10-0 Cropping Window Start Y

An 11-bit value specifies the number of lines between the inactive edge of VS and the first cropped video data line.

Cropping Window End X Register (CR12)

Read/Write Index: 0012H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Cropping Window End X											

Bits 15-12 Reserved

Bits 10-1 Cropping Window End X

A 12-bit value specifies the number of pixels between the inactive edge of HS and the last cropped video pixel.

Cropping Window End Y Register (CR13)

Read/Write Index: 0013H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Cropping Window End Y										

Bits 15-11 Reserved

Bits 10-0 Cropping Window End Y

An 11-bit value specifies the number of lines between the inactive edge of VS and the last cropped video data line.

Captured Video Width Register (CR14)

Read/Write Index: 0014H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Captured Video Width										

Bits 15-11 Reserved

Bits 10-0 Captured Video Width

An 11-bit value specifies the width in pixel of the captured video which is down-scaled (or not) from the cropped video. CR14 ≤ CR12 – CR10. Down-scaling is automatically done by an internal DDA (Digital Differential Accumulator).

Captured Video Height Register (CR15)

Read/Write Index: 0015H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Captured Video Height										

Bits 15-11 Reserved

Bits 10-0 Captured Video Height

An 11-bit value specifies the height in line of the captured video which is down-scaled (or not) from the cropped video. CR15 ≤ CR13 – CR11. Down-scaling is automatically done by an internal DDA (Digital Differential Accumulator).

Video Capture Control Register (CR16)

Read/Write Index: 0016H

Power-on Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCE	CAPCTL		VSP	HSP	VIM	VI Format		DBE	DBS	CLM	CKF	FTE	FTM	VC Format	

Bit 15 Video Capture Enable

0 = Disable

1 = Enable

Bits 14-13 Video Capture Control

00 = Capture all received fields/frames video data

01 = Capture every other received fields/frames video data

10 = Capture and hold after one frame/field (non-interlaced/interlaced mode)

11 = Reserved

Bit 12 VS Input Pin Polarity

0 = Negative sync pulse

1 = Positive sync pulse

Bit 11 HS Input Pin Polarity

0 = Negative sync pulse

1 = Positive sync pulse

Bit 10 Input Video Mode

0 = 16-bit mode

1 = 8-bit mode

Bits 9-8 Input Video Data Format

	YUV Input Video Data Format	
Bits 9-8	8-bit Mode (Y[7:0])	16-bit Mode (UV[7:0])
00	Y, U, Y, V, …	U, V, U, V, …
01	U, Y, V, Y, …	U, V, U, V, …
10	Y, V, Y, U, …	V, U, V, U, …
11	V, Y, U, Y, …	V, U, V, U, …

Bit 7 Double Buffering Enable

0 = Disable

1 = Enable

Bit 6 Double Buffering Status (Read-only)

0 = Buffer 0 active

1 = Buffer 1 active

Bit 5 Video Data Clamping Enable (Clamped to CCIR-601 Format)

0 = Disable

1 = Enable (Y is clamped to 16 – 235, UV is clamped to 16 – 240)

Bit 4 VICLK Falling Edge Latch

0 = Input video data and signals are latched by rising edge of VICLK

1 = Input video data and signals are latched by falling edge of VICLK

Bit 3 Filter Enable

0 = Disable

1 = Enable

Bit 2 Filter Type

0 = 1-2-1 filter

1 = 2-3-6-3-2 filter

Bits 1-0 Captured Video Data Format

00 = YUV4:2:2 packed mode

01 = YUV4:2:0 packed mode

10 = YUV4:2:2 planar mode

11 = YUV4:2:0 planar mode

Video Capture Test Mode Control Register (CR17)

Read/Write Index: 0017H

Power-on Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TEN	Reserved		Video Test Selection				

Bits 15-8 Reserved

Bit 7 Video Capture Test Mode Enable

0 = Normal operation

1 = Test mode enable

Bits 6-5 Reserved

Bits 4-0 Video Capture Test Mode Selection

Capture Test Data Register (CR18)

Read/Write Index: 0018H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Capture Test Data															

Bits 15-0 Capture Test Data (used for test mode only)

Capture Y Frame Buffer 0 Start Address Low Register (CR20)

Read/Write Index: 0020H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPYSA0[15:0]															

Bits 15-0 Capture Y Frame Buffer 0 Start Address Low

A 21-bit value specifies the WORD offset from the start of the frame buffer for buffer 0 (packed mode), or Y components (planar mode) of the captured video. Buffer 0 is always used, no matter double buffering is enabled or disabled. This register contains 16 lower-order bits of the value. Bits 20-16 are located at CR17_4-0.

Capture Y Frame Buffer 0 Start Address High Register (CR21)

Read/Write Index: 0021H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											CAPYSA0[20:16]				

Bits 15-5 Reserved

Bits 4-0 CAPYSA0[20:16]

Capture Y Frame Buffer 1 Start Address Low Register (CR22)

Read/Write Index: 0022H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPYSA1[15:0]															

Bits 15-0 Capture Y Frame Buffer 1 Start Address Low

A 21-bit value specifies the WORD offset from the start of the frame buffer for buffer 1 (packed mode), or Y components (planar mode) of the captured video. Buffer 1 is not used if double buffering is disabled. This register contains 16 lower-order bits of the value. Bits 20-16 are located at CR19_4-0.

Capture Y Frame Buffer 1 Start Address High Register (CR23)

Read/Write Index: 0023H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											CAPYSA1[20:16]				

Bits 15-5 Reserved

Bits 4-0 CAPYSA1[20:16]

Capture U Frame Buffer 0 Start Address Low Register (CR24)

Read/Write Index: 0024H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPUSA0[15:0]															

Bits 15-0 Capture U Frame Buffer 0 Start Address Low

A 21-bit value specifies the WORD offset from the start of the frame buffer for U components (planar mode) of the captured video. It is not used if the captured video is in packed mode. Buffer 0 is always used, no matter double buffering is enabled or disabled. This register contains 16 lower-order bits of the value. Bits 20-16 are located at CR1B_4-0.

Capture U Frame Buffer 0 Start Address High Register (CR25)

Read/Write Index: 0025H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											CAPUSA0[20:16]				

Bits 15-5 Reserved

Bits 4-0 CAPUSA0[20:16]

Capture U Frame Buffer 1 Start Address Low Register (CR26)

Read/Write Index: 0026H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPUSA1[15:0]															

Bits 15-0 Capture U Frame Buffer 1 Start Address Low

A 21-bit value specifies the WORD offset from the start of the frame buffer for U components (planar mode) of the captured video. It is not used if the captured video is in packed mode. Buffer 1 is not used if double buffering is disabled. This register contains 16 lower-order bits of the value. Bits 20-16 are located at CR1D_4-0.

Capture U Frame Buffer 1 Start Address High Register (CR27)

Read/Write Index: 0027H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											CAPUSA1[20:16]				

Bits 15-5 Reserved

Bits 4-0 CAPUSA1[20:16]

Capture V Frame Buffer 0 Start Address Low Register (CR28)

Read/Write Index: 0028H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPVSA0[15:0]															

Bits 15-0 Capture V Frame Buffer 0 Start Address Low

A 21-bit value specifies the WORD offset from the start of the frame buffer for V components (planar mode) of the captured video. It is not used if the captured video is in packed mode. Buffer 0 is always used, no matter double buffering is enabled or disabled. This register contains 16 lower-order bits of the value. Bits 20-16 are located at CR1F_4-0.

Capture V Frame Buffer 0 Start Address High Register (CR29)

Read/Write Index: 0029H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											CAPVSA0[20:16]				

Bits 15-5 Reserved

Bits 4-0 CAPVSA0[20:16]

Capture V Frame Buffer 1 Start Address Low Register (CR2A)

Read/Write Index: 002AH

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPVSA1[15:0]															

Bits 15-0 Capture V Frame Buffer 1 Start Address Low

A 21-bit value specifies the WORD offset from the start of the frame buffer for V components (planar mode) of the captured video. It is not used if the captured video is in packed mode. Buffer 1 is not used if double buffering is disabled. This register contains 16 lower-order bits of the value. Bits 20-16 are located at CR21_4-0.

Capture V Frame Buffer 1 Start Address High Register (CR2B)

Read/Write Index: 002BH

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											CAPVSA1[20:16]				

Bits 15-5 Reserved

Bits 4-0 CAPVSA1[20:16]

Capture Y Frame Buffer Stride Register (CR2C)

Read/Write Index: 002CH

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					CAPYS[10:0]										

Bits 15-11 Reserved

Bits 10-0 Capture Y Frame Buffer Stride

This register specifies the WORD offset of vertically adjacent pixels (packed mode), or vertically adjacent Y components of the captured video. It is used for both buffer 0 and buffer 1.

Capture UV Frame Buffer Stride Register (CR2D)

Read/Write Index: 002DH

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						CAPYS[9:0]									

Bits 15-10 Reserved

Bits 9-0 Capture UV Frame Buffer Stride

This register specifies the WORD offset of vertically adjacent U or V components of the captured video which is in planar mode. It is used for both buffer 0 and buffer 1. It is not used if the captured video is in packed mode.

Video Capture Y FIFO Threshold Register (CR2E)

Read/Write Index: 002EH

Power-on Default: 0804H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			VCAPY_HT[4:0]					Reserved			VCAPY_LT[4:0]				

Bits 15-13 Reserved

Bits 12-8 Video Capture Y FIFO High Threshold

When video capture FIFO (packed mode), or Y FIFO (planar mode) is filled to this threshold, a request is generated to the DRAM controller for DRAM access. Initial value is 08H.

Bits 7-5 Reserved

Bits 4-0 Video Capture Y FIFO Low Threshold

When video capture FIFO (packed mode), or Y FIFO (planar mode) is fetched to this threshold by DRAM controller, the FIFO is ready to release DRAM access to other pending requests. Initial value is 04H.

Video Capture UV FIFO Threshold Register (CR2F)

Read/Write Index: 002FH

Power-on Default: 8484H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCAPU_HT[3:0]				VCAPU_LT[3:0]				VCAPV_HT[3:0]				VCAPV_LT[3:0]			

Bits 15-12 Video Capture U FIFO High Threshold

When video capture U FIFO (planar mode) is filled to this threshold, a request is generated to the DRAM controller for DRAM access. It is not used if the captured video is in packed mode. Initial value is 08H.

Bits 11-8 Video Capture U FIFO Low Threshold

When video capture U FIFO (planar mode) is fetched to this threshold by DRAM controller, the FIFO is ready to release DRAM access to other pending requests. It is not used if the captured video is in packed mode. Initial value is 04H.

Bits 7-4 Video Capture V FIFO High Threshold

When video capture V FIFO (planar mode) is filled to this threshold, a request is generated to the DRAM controller for DRAM access. It is not used if the captured video is in packed mode. Initial value is 08H.

Bits 3-0 Video Capture V FIFO Low Threshold

When video capture V FIFO (planar mode) is fetched to this threshold by DRAM controller, the FIFO is ready to release DRAM access to other pending requests. It is not used if the captured video is in packed mode. Initial value is 04H.

8.3 JPEG Encoder Control Registers

Image Maximum Width Register (CR30)

Read/Write Index: 0030H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					MAXW[10:0]										

Bits 15-11 Reserved

Bits 10-0 Image Maximum Width

Image Maximum Height Register (CR31)

Read/Write Index: 0031H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					MAXH[10:0]										

Bits 15-11 Reserved

Bits 10-0 Image Maximum Height

Compressed Bitstream Buffer 0 Start Address Low Register (CR32)

Read/Write Index: 0032H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BSSA0[15:0]															

Bits 15-0 Compressed Bitstream Buffer 0 Start Address Low

A 21-bit value specifies the WORD offset from the start of the frame buffer for the compressed bitstream buffer 0. Bits 20-16 are located at CR33_4-0.

Compressed Bitstream Buffer 0 Start Address High Register (CR33)

Read/Write Index: 0033H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											BSSA0[20:16]				

Bits 15-5 Reserved

Bits 4-0 BSSA0[20:16]

Compressed Bitstream Buffer 1 Start Address Low Register (CR34)

Read/Write Index: 0034H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BSSA1[15:0]															

Bits 15-0 Compressed Bitstream Buffer 1 Start Address Low

A 21-bit value specifies the WORD offset from the start of the frame buffer for the compressed bitstream buffer 1. Bits 20-16 are located at CR35_4-0.

Compressed Bitstream Buffer 1 Start Address High Register (CR35)

Read/Write Index: 0035H

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											BSSA1[20:16]				

Bits 15-5 Reserved

Bits 4-0 BSSA1[20:16]

Restart Interval Register (CR36)

Read/Write Index: 0036H

Power-on Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Restart Interval															

Bits 15-0 Restart Interval

Specifies the number of MCU (Minimum Coded Unit) in the restart interval. Restart interval processing is disabled if this value is 0.

VLE FIFO Threshold Register (CR37)

Read/Write Index: 0037H

Power-on Default: 0804H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				VLE_HT[3:0]				Reserved				VLE_LT[3:0]			

Bits 15-12 Reserved

Bits 11-8 VLE FIFO High Threshold

When VLE FIFO is filled with JPEG coded bitstream to this threshold, a request is generated to the DRAM controller for DRAM access. Initial value is 08H.

Bits 7-4 Reserved

Bits 3-0 VLE FIFO Low Threshold

When VLE FIFO is fetched to this threshold by DRAM controller, the FIFO is ready to release DRAM access to other pending requests. Initial value is 04H.

Vertical Up-scaling Control Register (CR38)

Read/Write Index: 0038H

Power-on Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	Reserved									Vertical Up-scaling Factor					

Bit 15 Vertical Up-scaling Enable

0 = Disable

1 = Enable

Bits 14-6 Reserved

Bits 5-0 Vertical Up-scaling Factor

Up-scaling ratio (Scaled Height/Original Height) = 1.x, where x = Vertical Up-scaling Factor/64. The maximum 2× up-scaling will be done if 0 is programmed.

JPEG Encoder Control Register (CR39)

Read/Write Index: 0039H

Power-on Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							QRD	Reserved			JCLK	Test	TEN	JEN	R

Bits 15-9 Reserved

Bit 8 JPEG Quantization Table Registers (CR40 ~ CR7F) Read Enable

0 = Disable

1 = Enable

Bits 7-5 Reserved

Bit 4 JPEG Clock Enable (Must be enabled before JPEG Q-table access or encoding)

0 = Disable

1 = Enable

Bit 3 JPEG Test (used for test mode only)

Bit 2 JPEG Test Mode Enable

0 = Disable

1 = Enable

Bit 1 JPEG Encoder Enable

0 = Disable

1 = Enable

Bit 0 Reserved

JPEG Image Size Low Register (CR3A)

Read-only Index: 003AH

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JIMG_SIZE[15:0]															

Bits 15-0 JPEG Image Size Low

A 21-bit value specifies the JPEG compressed image size in WORD. This register contains the 16 lower-order bits of the value. Bits 20-16 are located at CR3B_4-0.

JPEG Image Size High Register (CR3B)

Read-only Index: 003BH

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											JIMG_SIZE _SIZE[20:16]				

Bits 15-5 Reserved

Bits 4-0 JPEG Image Size High

This register contains the 4 high-order bits of the JPEG Image Size.

USB FIFO Enable and Threshold Register (CR3C)

Read/Write Index: 003CH

Power-on Default: 0A05H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UEN	Reserved			USB_HT[3:0]				Reserved				USB_LT[3:0]			

Bit 15 USB Isochronous Pipe Transfer Enable

0 = Disable

1 = Enable

Bits 14-12 Reserved

Bits 11-8 USB FIFO High Threshold

Bits 7-4 Reserved

Bits 3-0 USB FIFO Low Threshold

USB Isochronous Transfer Size Low Register (CR3D)

Read/Write Index: 003DH

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISO_SIZE[15:0]															

Bits 15-0 USB Isochronous Transfer Size Low

A 21-bit value specifies the USB Isochronous Transfer Size in WORD for the original video transfer or the still image transfer. It is not used for the JPEG compression video transfer mode (CR39_1 = 1). This register contains the 16 lower-order bits of the value. Bits 20-16 are located at CR3E_4-0.

USB Isochronous Transfer Size High Register (CR3E)

Read/Write Index: 003EH

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											ISO_SIZE[20:16]				

Bits 15-5 Reserved

Bits 4-0 USB Isochronous Transfer Size High

This register contains the 4 high-order bits of the USB Isochronous Transfer Size. It is not used for the JPEG compression video transfer mode (CR39_1 = 1).

JPEG/MCTL Test Data Register (CR3F)

Read/Write Index: 003FH

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JPEG/MCTL Test Data															

Bits 15-0 JPEG/MCTL Test Data (used for test mode only)

JPEG Luminance Quantization Table Registers (CR40 -- CR5F)

Read/Write Index: 0040H - 005FH

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JPEG Luminance Quantization Table															

Bits 15-0 JPEG Luminance Quantization Table

Note. These registers can be read only when CR39 bit 8 is enabled (CR39_8 = 1).

JPEG Chrominance Quantization Table Registers (CR60 -- CR7F)

Read/Write Index: 0060H - 007FH

Power-on Default: XXXXH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JPEG Chrominance Quantization Table															

Bits 15-0 JPEG Chrominance Quantization Table

Note. These registers can be read only when CR39 bit 8 is enabled (CR39_8 = 1).

9 ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

Table 9.1 Absolute Maximum Ratings

Ambient temperature	0° C to 70° C
Storage temperature	-40° C to 125° C
DC supply voltage	-0.5V to 7V
I/O pin voltage with respect to VSS	-0.5V to VDD + 0.5V

9.2 DC Characteristics

9.2.1 USB Transceiver DC Characteristics

Table 9.2 USB Transceiver DC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{DI}	Differential Input Sensitivity	|DP – DM|	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8	2.0	V
V_{OL}	Static Output Low Voltage	RL of 1.5 KΩ to 3.6 V		0.3	V
V_{OH}	Static Output High Voltage	RL of 15 KΩ to VSS	2.8	3.6	V
V_{CRS}	Output Signal Crossover Voltage		1.3	2.0	V
Z_{DRV}	Driver Output Resistance	Steady state drive	28	43	Ω
C_{IN}	Pin Capacitance			20	pF

9.2.2 Digital DC Characteristics

Table 9.3 Digital DC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
VDD5V	5V Power Supply		4.40	5.25	V
VDD	3.3V Power Supply		3.0	3.6	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage			VSS+0.4	V

V_{OH}	Output High Voltage		2.4		V
I_{IL}	Input Low Leakage Current	V_{IN} = 0.4V		+70	µA
I_{IH}	Input High Leakage Current	V_{IN} = 2.4V		-70	µA
I_{UP}	Pull-up Current	V_{IN} = 0V	-133.2	-400.6	µA
C_{IO}	Pin Capacitance			10	pF
I_{PD}	Powerdown Current USB Suspend			200	µA
I_{DD}	Active Current	F_{CLK} = 12 MHz		120	mA

9.3 AC Characteristics

9.3.1 USB Transceiver AC Characteristics

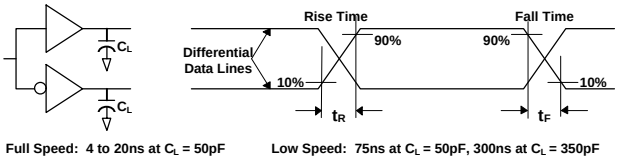


Figure 9.1 Data Signal Rise and Fall Time

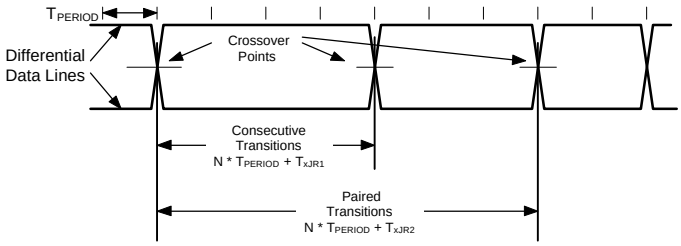


Figure 9.2 Differential Data Jitter

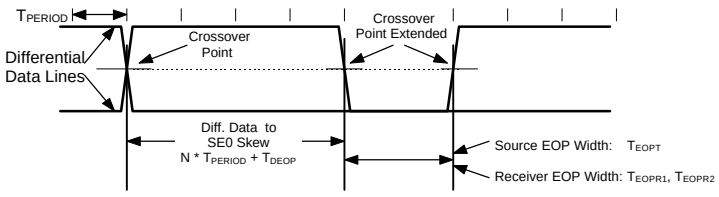


Figure 9.3 Differential to EOP Transition Skew and EOP Width

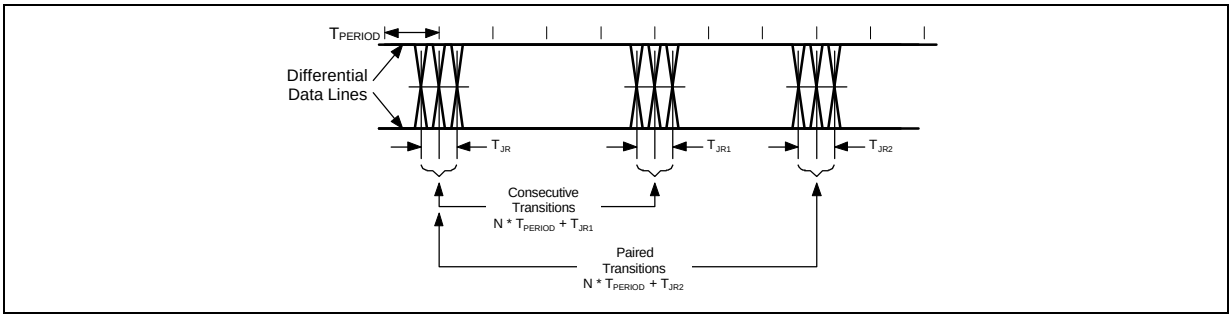


Figure 9.4 Receiver Jitter Tolerance

Table 9.4 USB Transceiver AC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
T_R	Rise Time	CL = 50 pF	4	20	ns
T_F	Fall Time	CL = 50 pF	4	20	ns
T_{RFM}	Rise/Fall Time Matching		90	110	%
T_{DRATE}	Full Speed Data Rate	Average bit rate (12 Mb/s ± 0.25%)	11.97	12.03	Mbps
	Source Differential Driver Jitter				
T_{DJ1}	To Next Transition		-3.5	3.5	ns
T_{DJ2}	For Paired Transitions		-4.0	4.0	ns
T_{EOPT}	Source EOP Width		160	175	ns
T_{DEOP}	Differential to EOP Transition Skew		-2	5	ns
	Receiver Data Jitter Tolerance				
T_{JR1}	To Next Transition		-18.5	18.5	ns
T_{JR2}	For Paired Transitions		-9	9	ns
	EOP Width at Receiver				
T_{EOPR1}	Must Reject as EOP		40		ns
T_{EOPR2}	Must Accept as EOP		82		ns

9.3.2 RESET Timing AC Characteristics

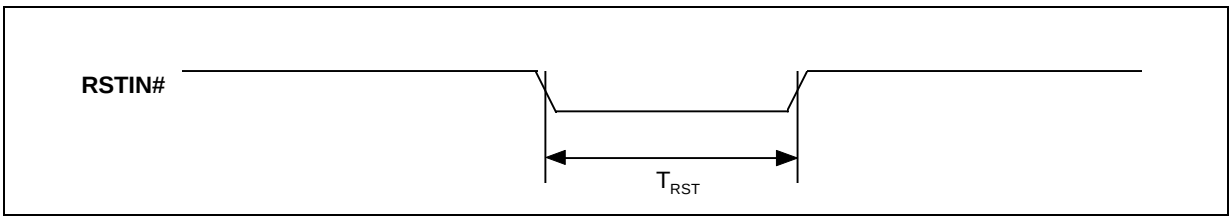


Figure 9.5 RESET Timing

Table 9.5 RESET Timing

Symbol	Parameter	Conditions	Min.	Max.	Unit
T_{RST}	Reset Pulse Width		100		ns

9.3.3 Clock AC Characteristics

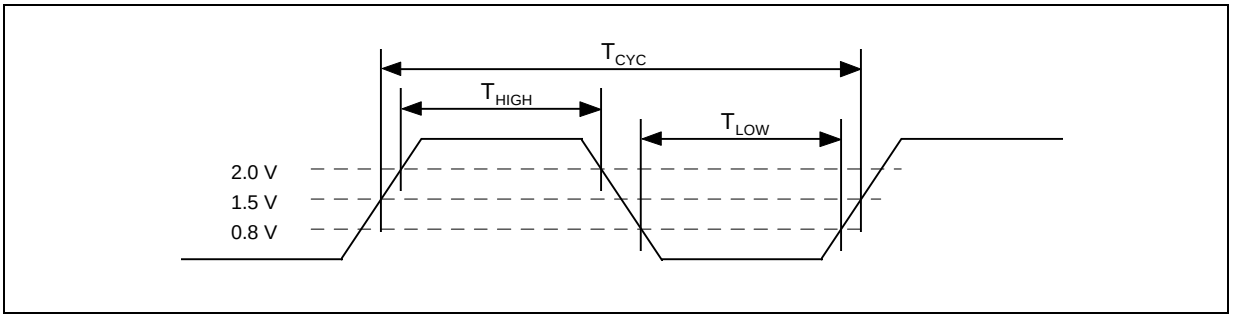


Figure 9.6 Clock Waveform

Table 9.6 Clock AC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
$1/T_{CYC}$	Oscillator Frequency		11.988	12.012	MHz
	VICLK Frequency		5	30	MHz
	SMCLK Frequency		47.88	48.12	MHz
T_{HIGH}	Oscillator Clock High Time		33	50	ns
	VICLK Clock High Time		5		ns
	SMCLK Clock High Time		8.3	12.5	ns
T_{LOW}	Oscillator Clock Low Time		33	50	ns
	VICLK Clock Low Time		5		ns
	SMCLK Clock Low Time		8.3	12.5	ns

9.3.4 Input Video AC Characteristics

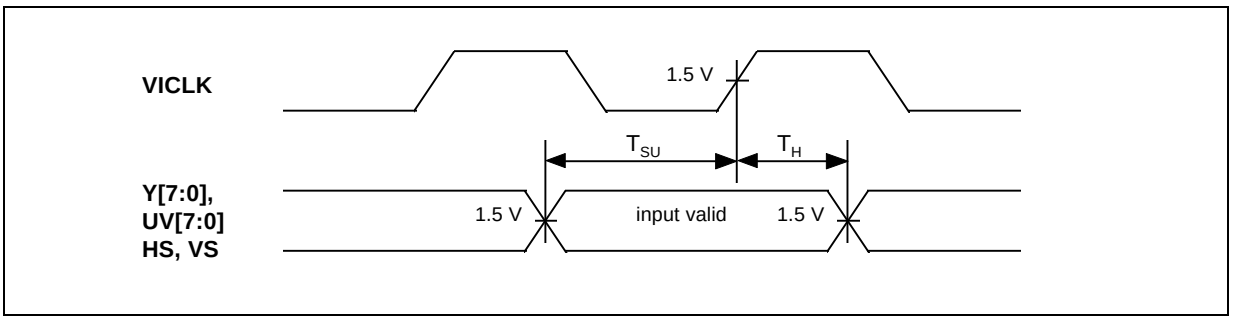


Figure 9.7 Input Video Timing

Table 9.7 Input Video AC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
T_{SU}	Y[7:0], UV[7:0], HS, VS Setup Time		6		ns
T_H	Y[7:0], UV[7:0], HS, VS Hold Time		4		ns

9.3.5 DRAM Interface AC Characteristics

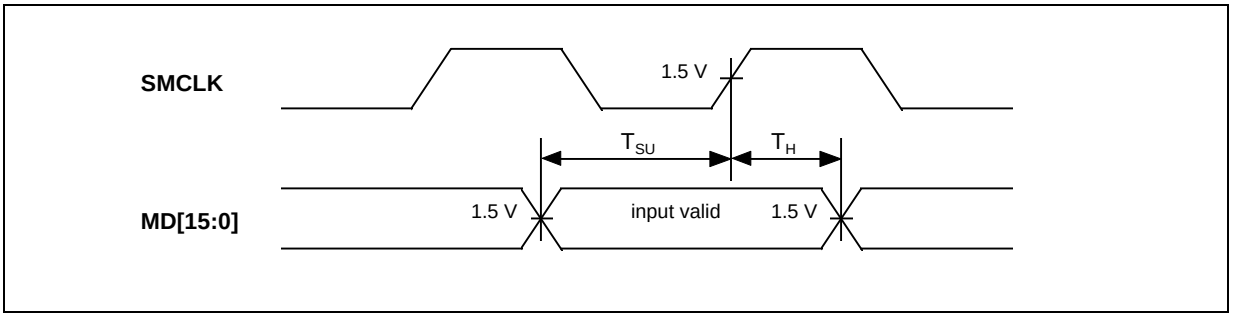


Figure 9.8 DRAM Interface Input Timing

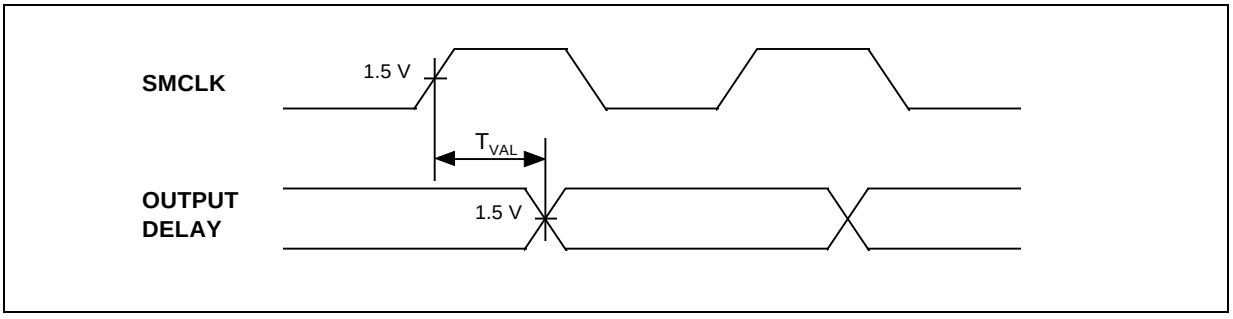


Figure 9.9 DRAM Interface Output Timing

Table 9.8 DRAM Interface AC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
T_{SU}	MD[15:0] Setup Time		0		ns
T_H	MD[15:0] Hold Time		7		ns
T_H	MD[15:0], MA[10:0], BA, RAS[1:0]#/CS[1:0]#, CAS[1:0]#/DQM[1:0], OE#/CKE, WE#, SRAS#, SCAS#		2	7	ns

9.3.6 EEPROM Interface AC Characteristics

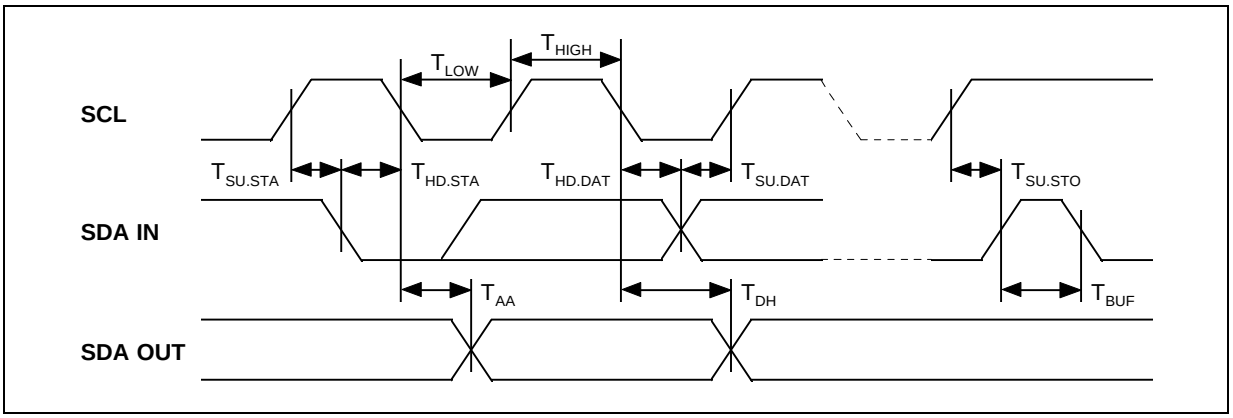
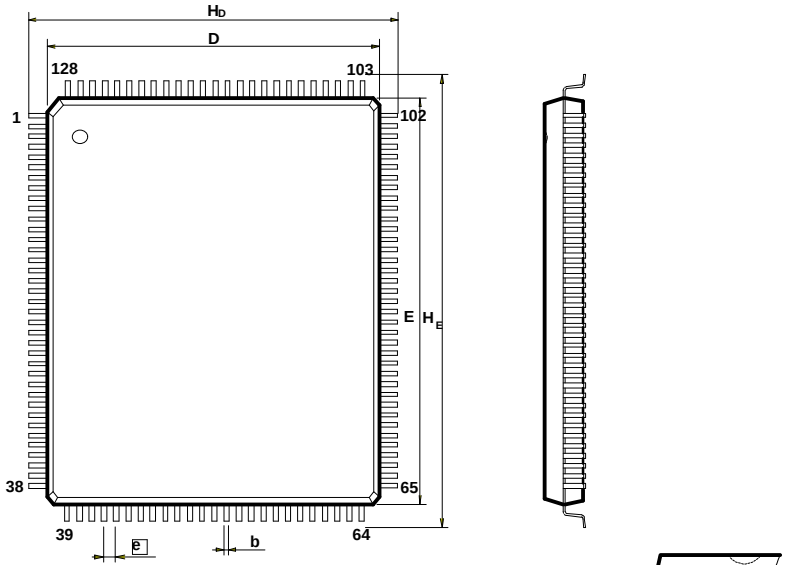


Figure 9.10 EEPROM Interface Timing

Table 9.9 EEPROM Interface AC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
F_{SCL}	SCL Clock Frequency			100	KHz
T_{LOW}	Clock Pulse Width Low		4.7		µs
T_{HIGH}	Clock Pulse Width High		4.0		µs
T_{AA}	Clock Low to Data Out Valid		0.1	4.5	µs
T_{BUF}	Time the bus must be free before a new transmission can start		4.7		µs
$T_{HD.STA}$	Start Hold Time		4.0		µs
$T_{SU.STA}$	Start Set-up Time		4.7		µs
$T_{HD.DAT}$	Data In Hold Time		0		µs
$T_{SU.DAT}$	Data In Set-up Time		200		ns
T_R	Inputs Rise Time			1.0	µs
T_F	Inputs Fall Time			300	ns
$T_{SU.STO}$	Stop Set-up Time		4.7		µs
T_{DH}	Data Out Hold Time		100		ns

10 PACKAGE SPEC.



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.134	—	—	3.40
A_1	0.004	—	—	0.10	—	—
A_2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e		0.020			0.50	
H_D	0.669	0.677	0.685	17.00	17.20	17.40
H_E	0.905	0.913	0.921	23.00	23.20	23.40
L	0.023	0.031	0.039	0.60	0.80	1.00
L_1	0.055	0.063	0.071	1.40	1.60	1.80
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

Figure 10.1 128L QFP (14x20x2.75mm footprint 3.2mm) Dimensions

11 ORDERING INFORMATION

Part Number	Package
W9967CF	128L QFP

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5792647
http://www.winbond.com.tw/
Voice & Fax-on-demand: 886-2-7197006

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.
Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.
2730 Orchard Parkway, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668