HAT3004R

Silicon N and P Channel Power MOS FET

Application

High speed power switching

Features

- Low on–resistance
- Capable of 4V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8DA
EIAJ Code	—
JEDEC Code	MS–012AA

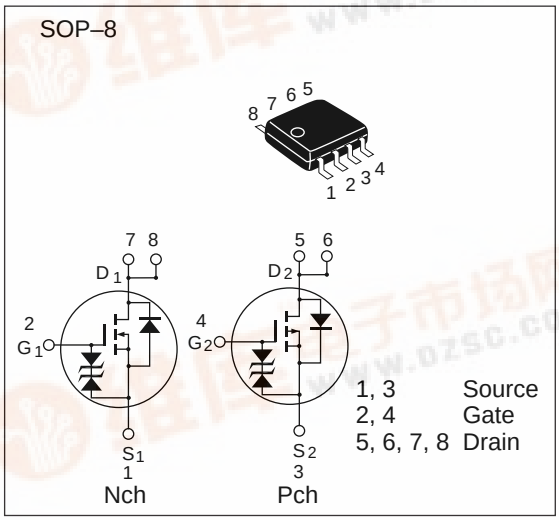


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings Nch	Ratings Pch	Unit
Drain to source voltage	V_{DSS}	30	–30	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	3.5	–2.5	A
Drain peak current	$I_{D(pulse)}$*	14	–10	A
Channel dissipation	Pch***	2.0		W
Channel dissipation	Pch**	1.3		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** 1 Drive operation : *** 2 Drive operation When using surface mounted on FR4 board

Table 2 Electrical Characteristics N Channel (Ta = 25°C)

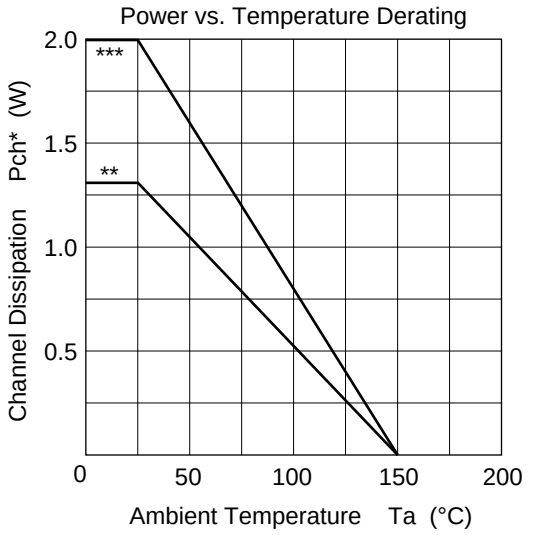
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.08)	0.1	Ω	I_D = 2A V_{GS} = 10V *
		—	(0.11)	0.15	Ω	I_D = 2A V_{GS} = 4V *
Forward transfer admittance	$\|y_{fs}\|$	(2.0)	(3.0)	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	(180)	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	(110)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(45)	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	(10)	—	ns	V_{GS} = 4 V, I_D = 2 A
Rise time	t_r	—	(60)	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$	—	(25)	—	ns	
Fall time	t_f	—	(20)	—	ns	
Body–drain diode forward voltage	V_{DF}	—	(0.8)	—	V	I_F = 3.5A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	(50)	—	ns	I_F = 3.5A, V_{GS} = 0 diF / dt = 20 A / µs

* Pulse Test

Table 2 Electrical Characteristics P Channel (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.13)	0.25	Ω	I_D = –1 A V_{GS} = –10 V *
		—	(0.2)	0.4	Ω	I_D = –1 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	(2.0)	(3.0)	—	S	I_D = –1 A V_{DS} = –10 V *
Input capacitance	Ciss	—	(250)	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	(150)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(60)	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	(10)	—	ns	V_{GS} = –4 V, I_D = –1 A
Rise time	t_r	—	(60)	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	(20)	—	ns	
Fall time	t_f	—	(25)	—	ns	
Body–drain diode forward voltage	V_{DF}	—	(–0.8)	—	V	I_F = –2.5A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	(50)	—	ns	I_F = –2.5A, V_{GS} = 0 diF / dt = 20 A / µs

* Pulse Test

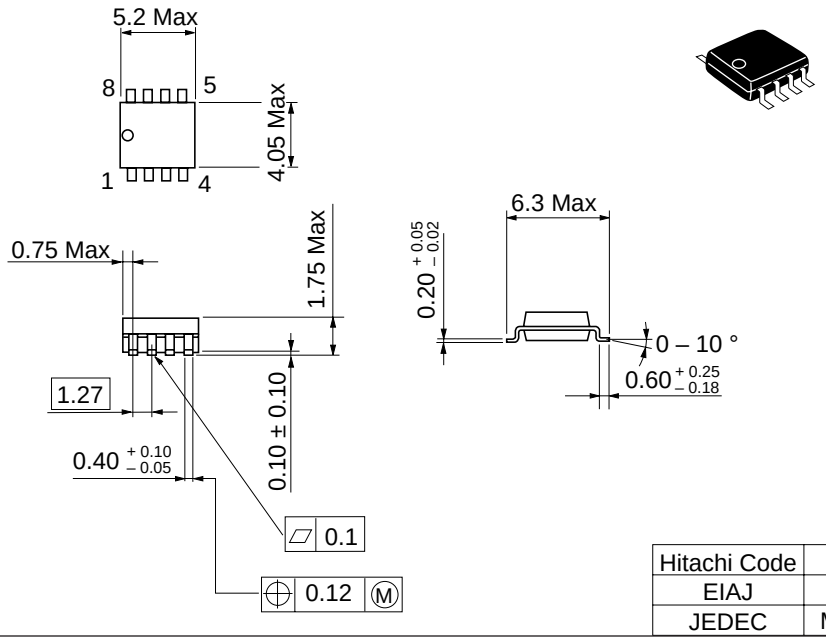


* When using surface mounted on FR4 board
** 1 Drive Operation
*** 2 Drive Operation

Package Dimensions

Unit : mm

• SOP–8



Hitachi Code	FP–8DA
EIAJ	—
JEDEC	MS-012AA