HM671400H Series

4,194,304-words × 1-bit High Speed Static Random Access Memory

HITACHI

ADE-203-086G(Z)
Rev. 8
Aug. 28, 1996

Features

- 4194304-words × 1 bit organization
- Directly TTL compatible input and output
- +5.0 V Single Supply
- Completely static memory
- No clock or timing strobe required
- Super fast access time: 15/20 ns (Max)
- Revolutional Pin Arrangement

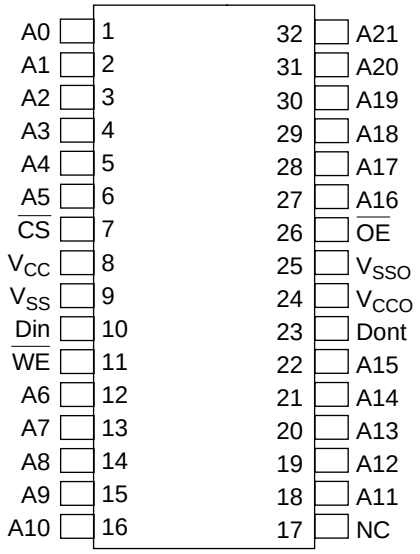
Ordering Information

Type No.	Organization	Access time	Package
HM671400HJP-15		15 ns	400 mil 32 pin
HM671400HJP-20	4M × 1	20 ns	Plastic SOJ (CP-32DB)

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Hitachi

Pin Arrangement

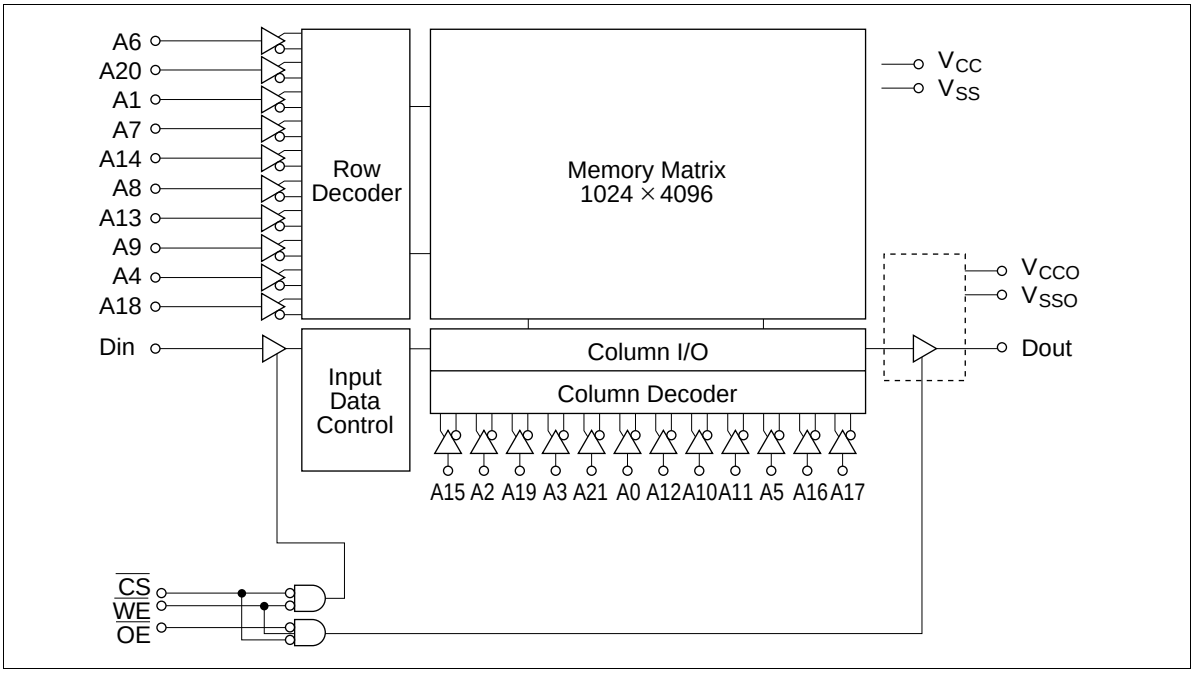


(Top view)

Pin Description

Pin Name	Function
A0 to A21	Address Input
Din	Data Input
Dout	Data Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
V_{cc}	+5 V Power Supply
V_{CCO}	Output Buffer Power Supply
V_{SSO}	Output Buffer Ground
V_{SS}	Ground
NC	Not Connect

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	Output	V_{cc} Current
H	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High Z	I_{CC}, I_{CC1}
L	H	L	Read	Data Out	I_{CC}, I_{CC1}
L	L	H	Write	High Z	I_{CC}, I_{CC1}
L	L	L	Write	High Z	I_{CC}, I_{CC1}

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage *[1]	V_{CC}	–0.5 to + 7.0	V
Voltage on any pin relative to V_{SS} *[1]	V_T	–0.5 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0/1.5 *[2]	W
Operating Temperature Range	Topr	0 to +70	°C
Storage Temperature Range (with bias)	Tstg (Bias)	–10 to + 85	°C
Storage Temperature Range	Tstg	–55 to + 125	°C

Notes: 1. With respect to $V_{SS} = V_{SSO}$
2. P_T = 1.5 W is guaranteed under the minimum air flow exceeding 500 linear feet per minute.

Under the dc and ac specifications shown in the Tables, this device is tested under the minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions (0°C ≤ Ta ≤ 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}, V_{CCO}	4.5	5.0	5.5	V
	V_{SS}, V_{SSO}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	–0.5	—	0.8	V

DC and Operating Characteristics ($V_{CC} = V_{CCO} = 5.0$ V ± 10%, $V_{SS} = V_{SSO} = 0$ V, Ta = 0 to +70°C)

			15		20		
Item	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	—	2	—	2	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL} V_{OUT} = 0 V to V_{CC}	—	10	—	10	µA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{OUT} = 0 mA	—	120	—	120	mA
Average Operating Current	I_{CC1}	Min. cycle, I_{OUT} = 0 mA	—	170	—	150	mA
Standby Power Supply Current	I_{SBAC}	$\overline{CS}$ = V_{IH} Min. cycle	—	100	—	80	mA
	I_{SBDC}	$\overline{CS}$ = V_{IH} All input fixed and V_{IN} = V_{IH} or V_{IL}	—	20	—	20	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} - 0.2 V V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} - 0.2 V	—	10	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –4 mA	2.4	—	2.4	—	V

AC Characteristics (V_{CC} = V_{CCO} = 5.0 V ± 10%, V_{SS} = V_{SSO} = 0 V, Ta = 0°C to 70°C, unless otherwise noted.)

Read Cycle

		15		20		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read Cycle Time	t_{RC}	15	—	20	—	ns
Address Access Time	t_{AA}	—	15	—	20	ns
Chip Select Access Time	t_{ACS}	—	15	—	20	ns
Chip Selection to Output in Low Z	t_{LZ} *1, *2	5	—	5	—	ns
Output Enable to Output Valid	t_{OE}	—	8	—	10	ns
Output Enable to Output in Low Z	t_{OLZ} *1, *2	2	—	2	—	ns
Chip Deselection to Output in High Z	t_{HZ} *1, *2	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns

Notes: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load(B).

Write Cycle

		15		20		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write Cycle Time	t_{WC} *1	15	—	20	—	ns
Chip Selection to End of Write	t_{CW}	12	—	15	—	ns
Address Valid to End of Write	t_{AW}	12	—	15	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	12	—	15	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Data Valid to End of Write	t_{DW}	8	—	10	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Write Enable to Output in High Z	t_{WZ} *2, *3	0	7	0	8	ns
Output Disable to Output in High Z	t_{OHZ} *2, *3	0	7	0	8	ns
Output Active from End of Write	t_{OW} *2, *3	2	—	2	—	ns

Notes: 1. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified with loading Load(B).

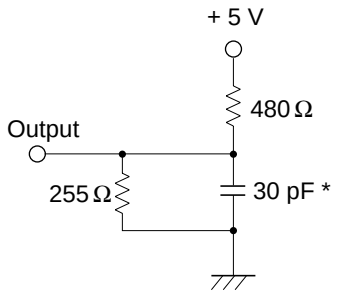
Capacitance (Ta = 25°C, f = 1 MHz)

Item	Symbol	Max	Unit	Test Condition
Input Capacitance	C_{IN} *1	6	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT} *1	8	pF	V_{OUT} = 0 V

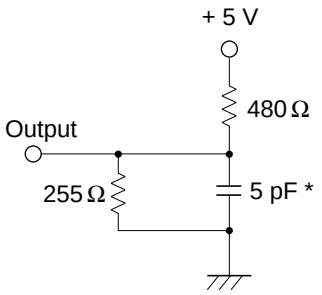
Note: 1. This parameter is sampled and not 100% tested.

AC Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output Load: See figure
- Input rise and fall times: 4 ns
- Output reference levels: 1.5 V



Output Load A



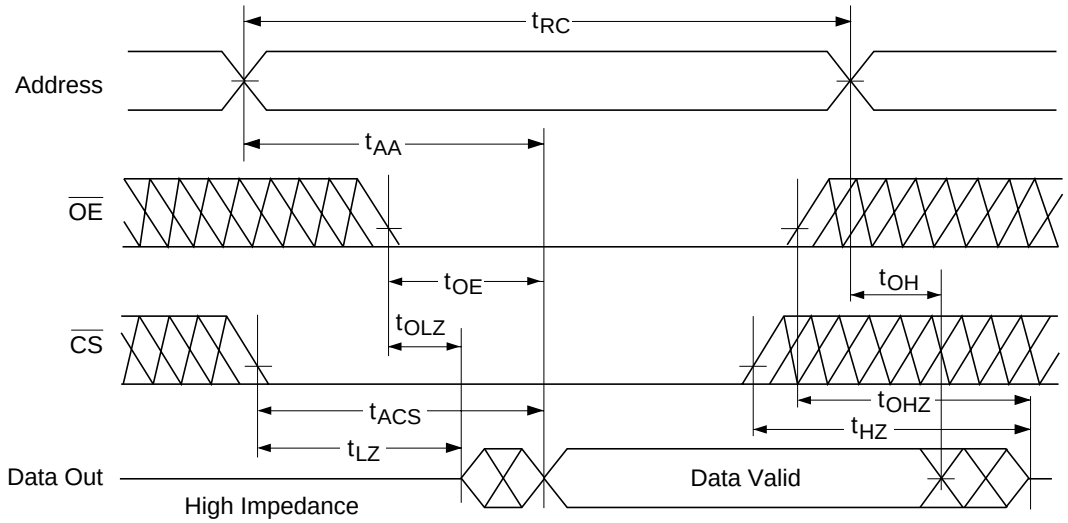
Output Load B

(for t_{HZ}, t_{LZ}, t_{OHZ}, t_{OLZ}, t_{WZ}, & t_{OW})

* including scope and jig capacitance

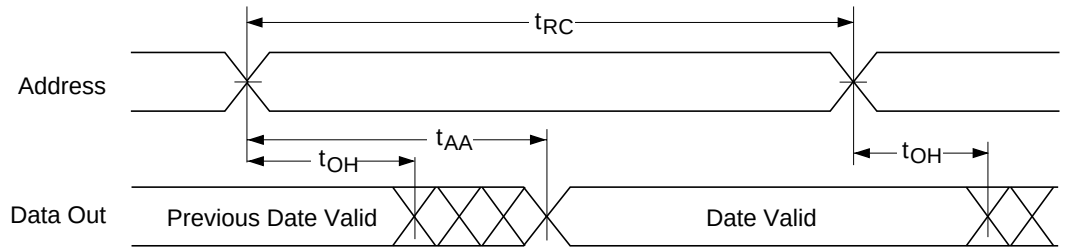
Timing Waveforms

Read Cycle-1 *1



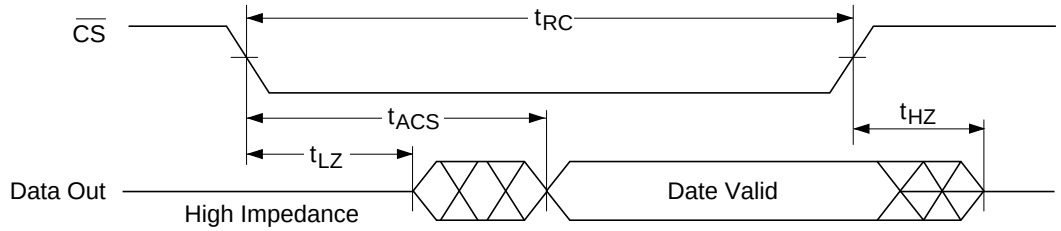
Note: 1. $\overline{WE} = V_{IH}$

Read Cycle-2 *1, *2, *3



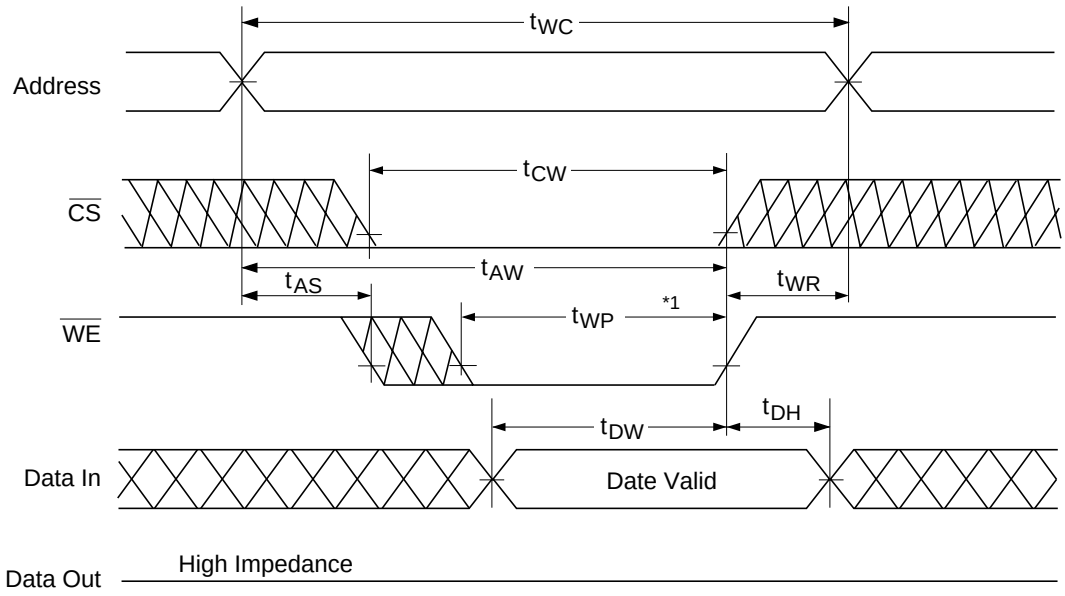
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{CS} = V_{IL}$
3. $\overline{OE} = V_{IL}$

Read Cycle-3 *1, *2, *3



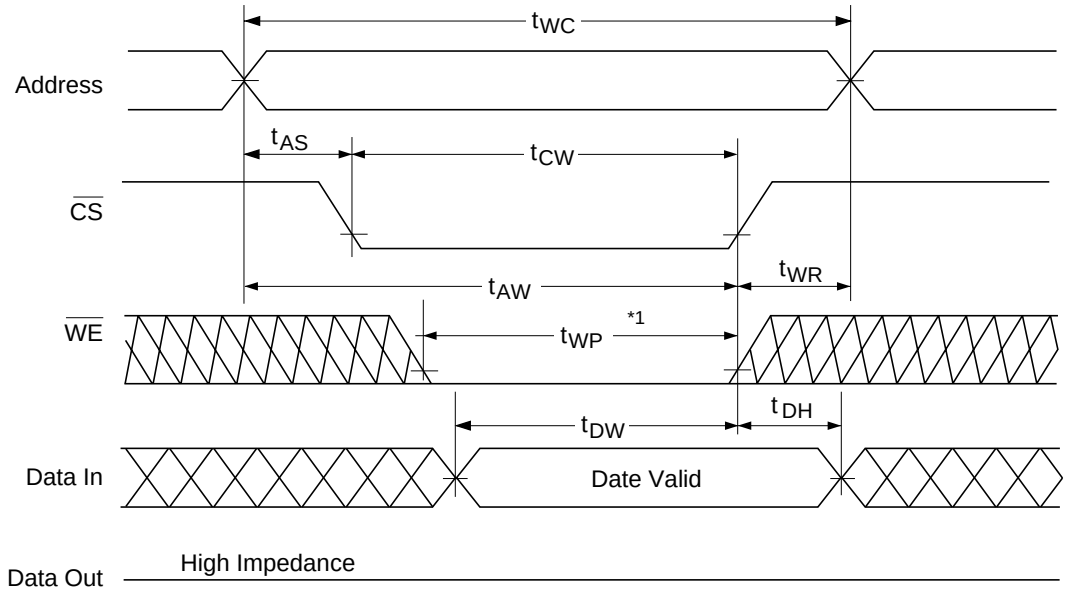
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{CS} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle-1 *1 ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



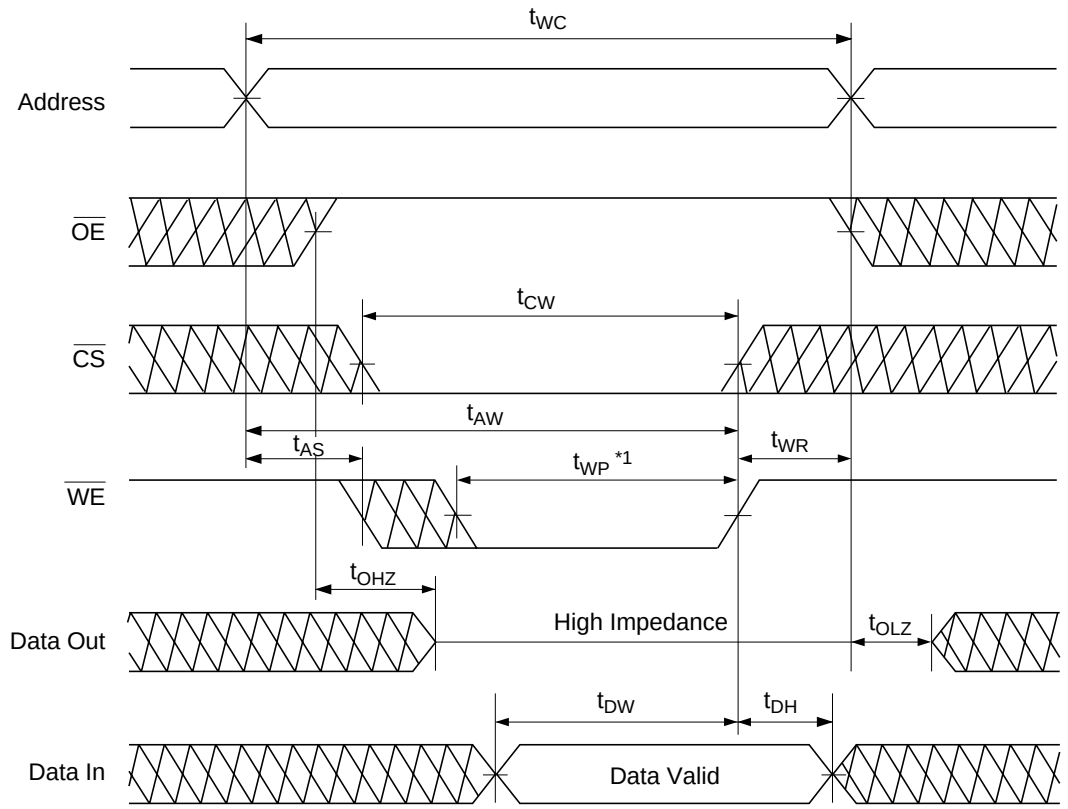
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle-2 *1 ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



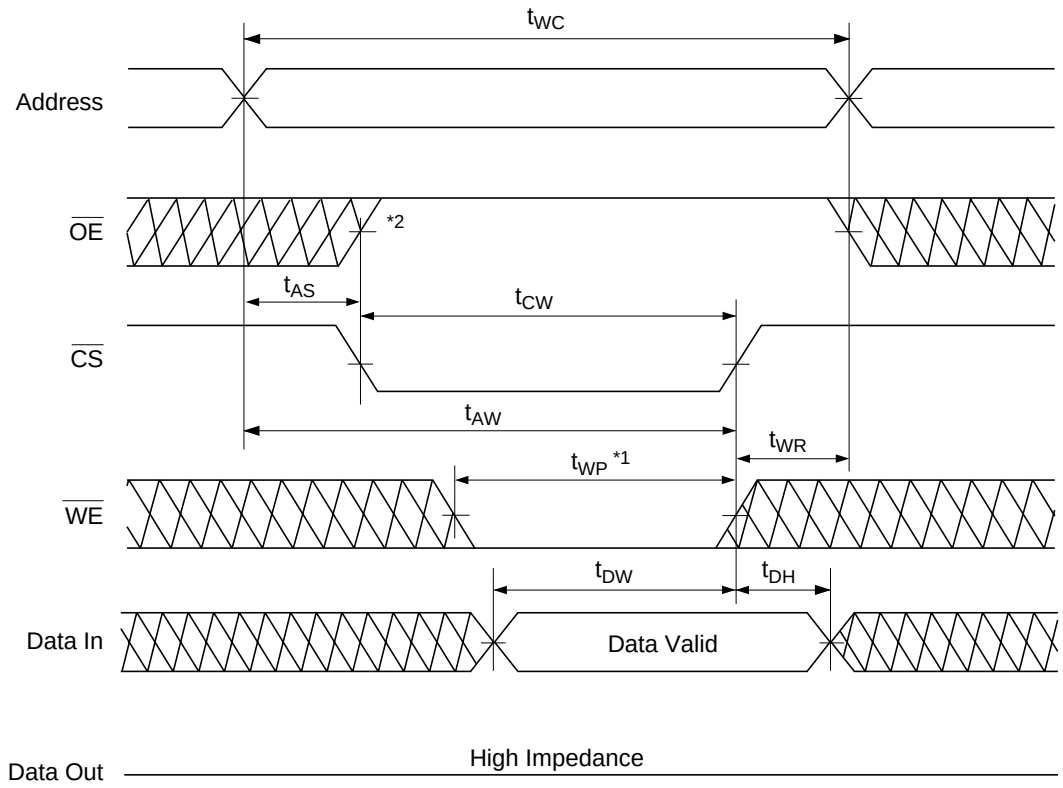
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle-3 *1 ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



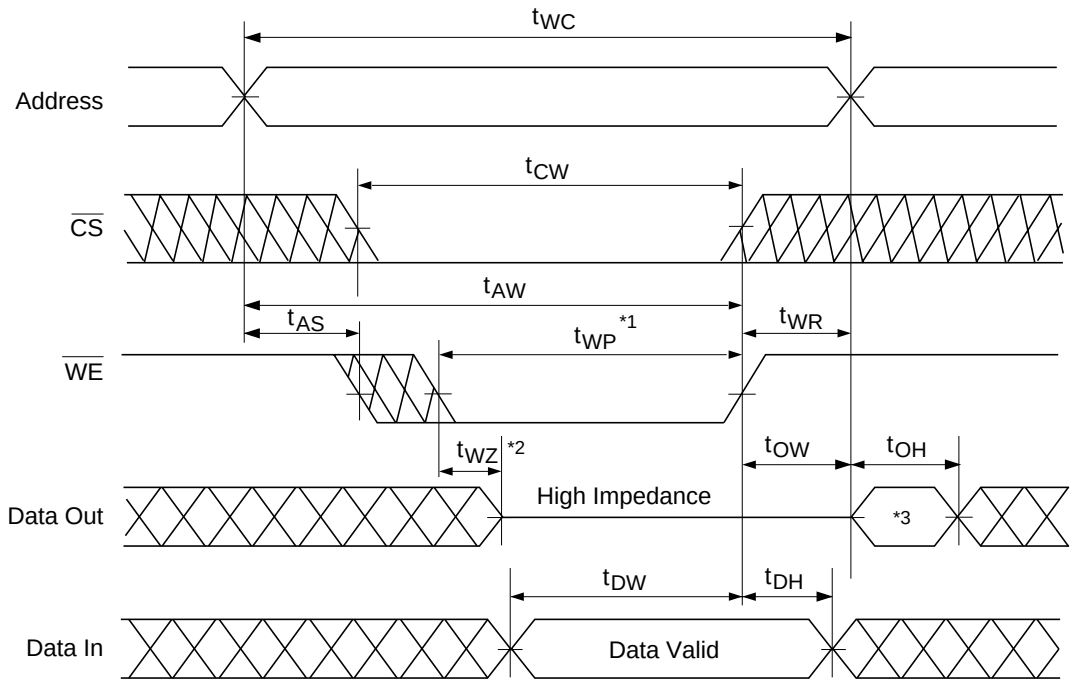
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle-4 *1, *2 ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



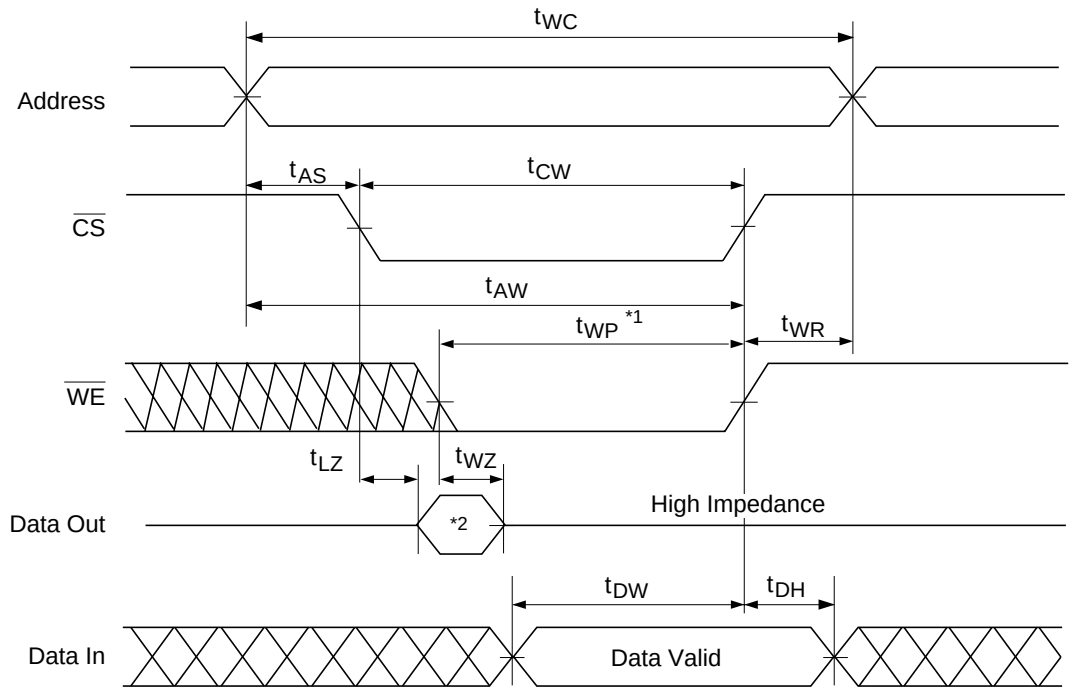
Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in a high impedance state.

Write Cycle-5 *1, *2, *3 ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must nit be applied.
3. Output data is the same phase of write data of this write cycle.

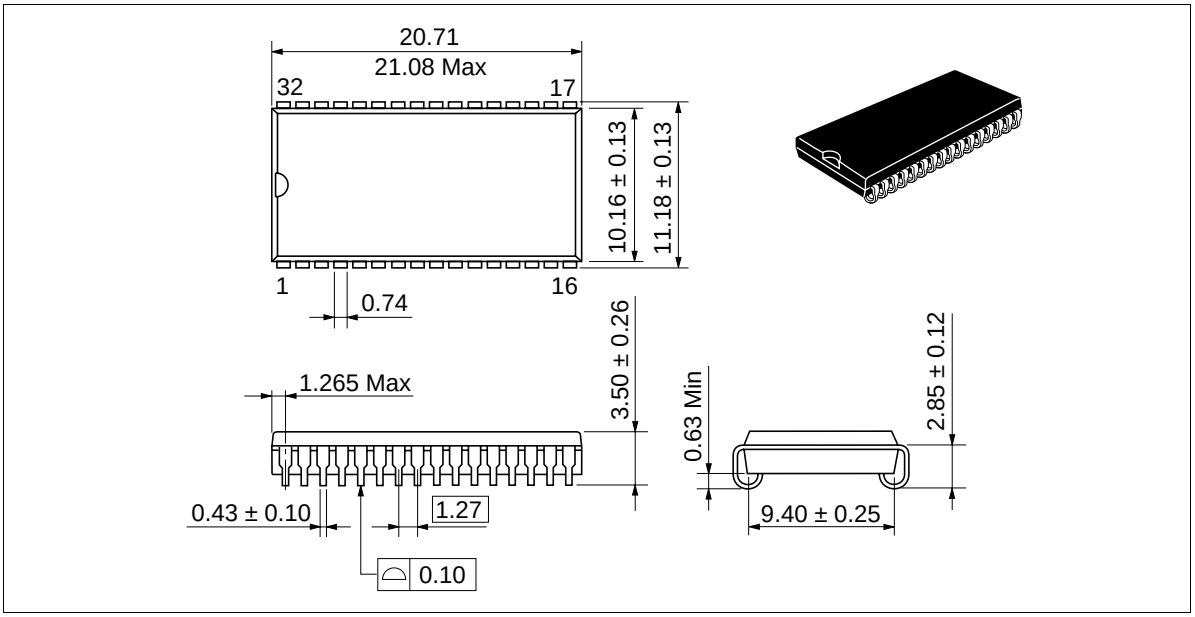
Write Cycle-6 *1, *2 ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

Package Dimension

HM761400HJP Series (CP-32DB) Unit : mm



HM671400H Series

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