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BB201M

Build in Biasing Circuit MOS FET IC
UHF RF Amplifier

HITACHI

ADE-208-713A (Z)
2nd. Edition
Dec. 1998

Features

- Build in Biasing Circuit; To reduce useing parts cost & PC board space.
- Low noise characteristics;
  (NF = 2.0 dB typ. at f = 900 MHz)
- Withstanding to ESD;
  Build in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditins.
- Provide mini mold packages; MPAK-4R(SOT-143 var.)

Outline

MPAK-4R

1. Source
2. Drain
3. Gate2
4. Gate1

Notes: 1. Marking is “AV–”.
2. BB201M is individual type number of HITACHI BBFET.

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Absolute Maximum Ratings (Ta = 25°C)

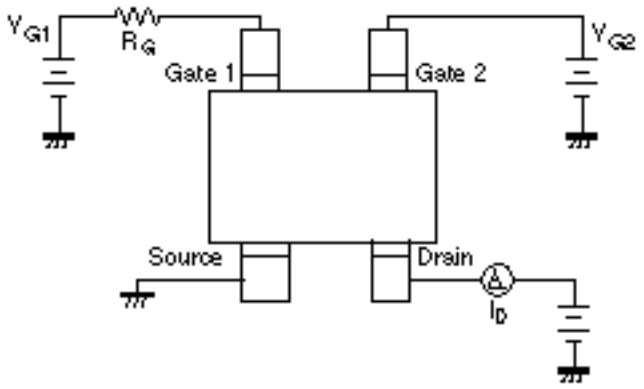
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 – 0	V
Gate 2 to source voltage	V_{G2S}	±6	V
Drain current	I_D	25	mA
Channel power dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Electrical Characteristics (Ta = 25°C)

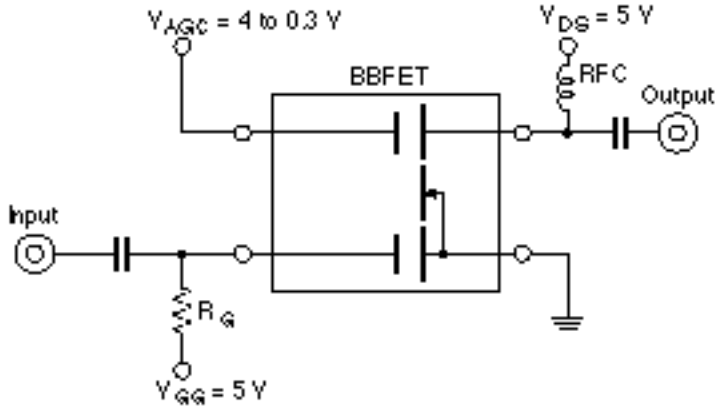
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200µA, V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	±6	—	—	V	I_{G2} = ±10µA, V_{G1S} = V_{DS} = 0
Gate1 to cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5V, V_{G2S} = V_{DS} = 0
Gate2 to cutoff current	I_{G2SS}	—	—	±100	nA	V_{G2S} = ±5V, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.2	0.45	0.8	V	V_{DS} = 5V, V_{G2S} = 4V I_D = 100µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.4	0.7	1.0	V	V_{DS} = 5V, V_{G1S} = 5V I_D = 100µA
Drain current	$I_{D(op)}$	10	15	20	mA	V_{DS} = 5V, V_{G1} = 5V, V_{G2S} = 4V R_G = 220kΩ
Forward transfer admittance	$\|y_{fs}\|$	16	22	—	mS	V_{DS} = 5V, V_{G1} = 5V, V_{G2S} =4V R_G = 220kΩ, f = 1kHz
Input capacitance	c_{iss}	1.2	1.7	2.2	pF	V_{DS} = 5V, V_{G1} = 5V
Output capacitance	c_{oss}	0.7	1.1	1.5	pF	V_{G2S} =4V, R_G = 220kΩ
Reverse capacitance	c_{rss}	—	0.012	0.03	pF	f = 1MHz
Power gain	PG	16	20	—	dB	V_{DS} = 5V, V_{G1} = 5V, V_{G2S} =4V
Noise figure	NF	—	2.0	3.0	dB	R_G = 220kΩ, f = 900MHz

Main Characteristics

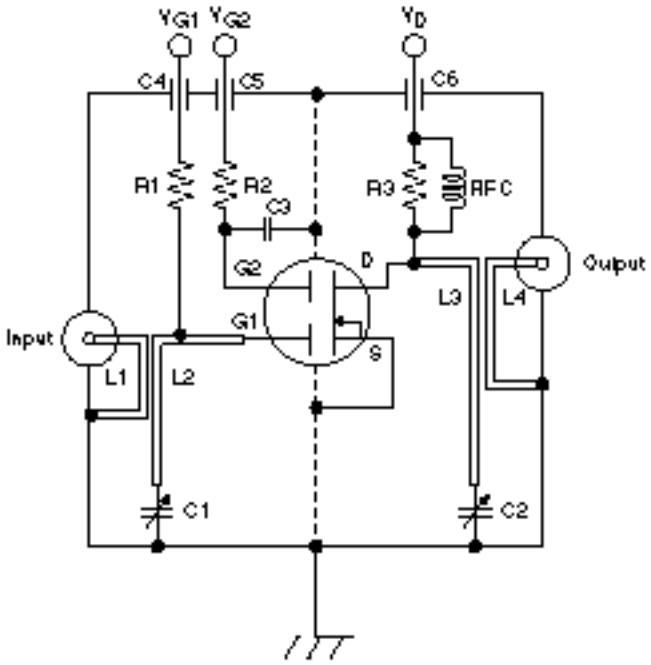
Test Circuit for Operating Items ($I_{D(op)}$, |yfs|, Ciss, Coss, Crss, NF, PG)



Application Circuit

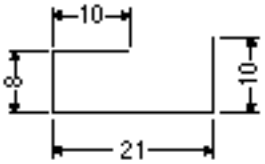


900MHz Power Gain, Noise Test Circuit

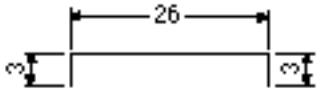


C1, C2 : Variable Capacitor (10pF MAX)
C3 : Disk Capacitor (1000pF)
C4 to C6 : Air Capacitor (1000pF)
R1 : 220 kΩ
R2 : 47 kΩ
R3 : 4.7 kΩ

L1 :

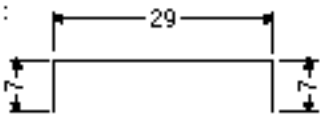


L2 :

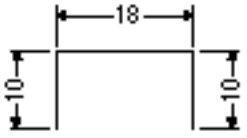


(ϕ 1mm Copper wire)
Unit : mm

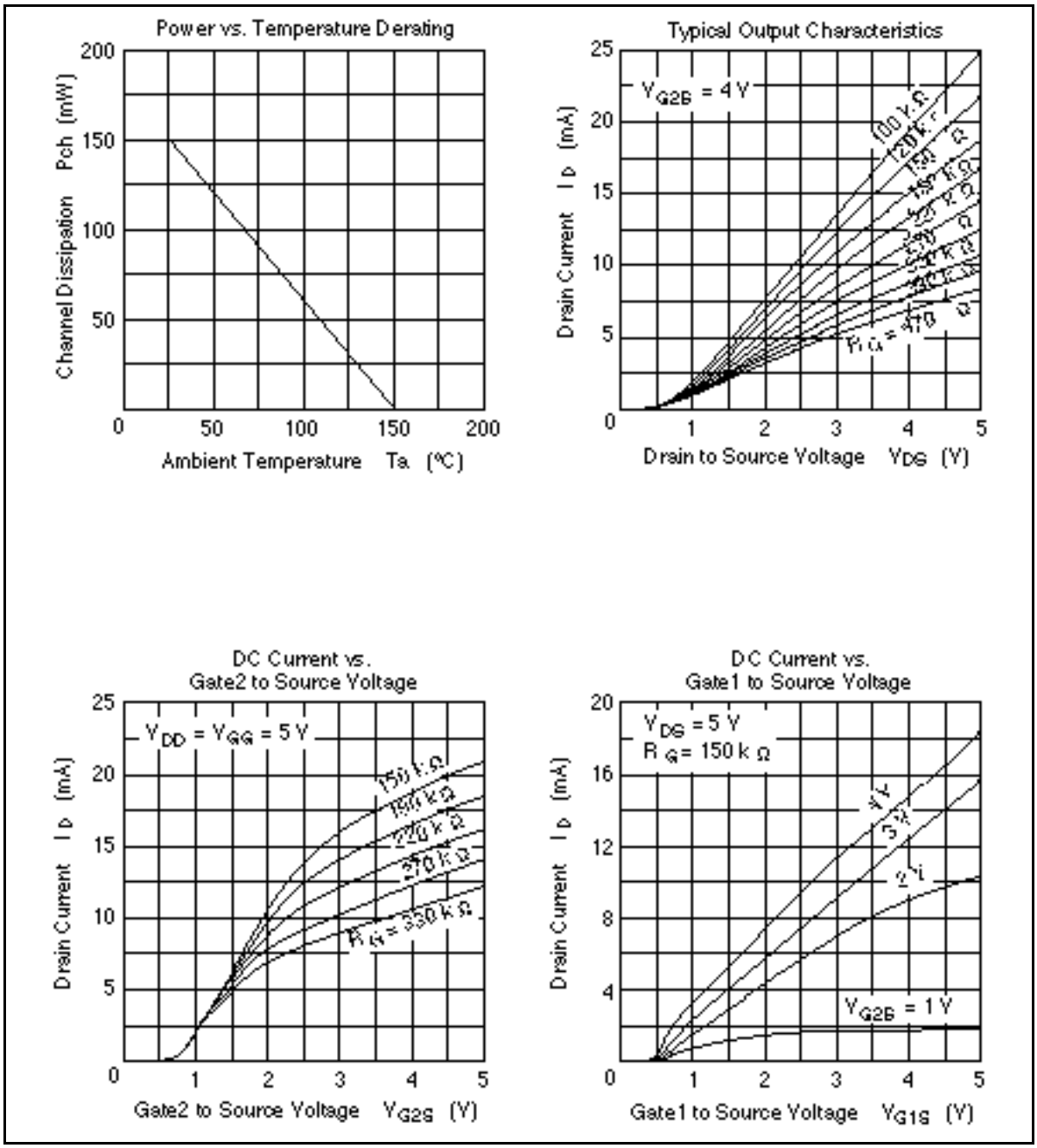
L3 :

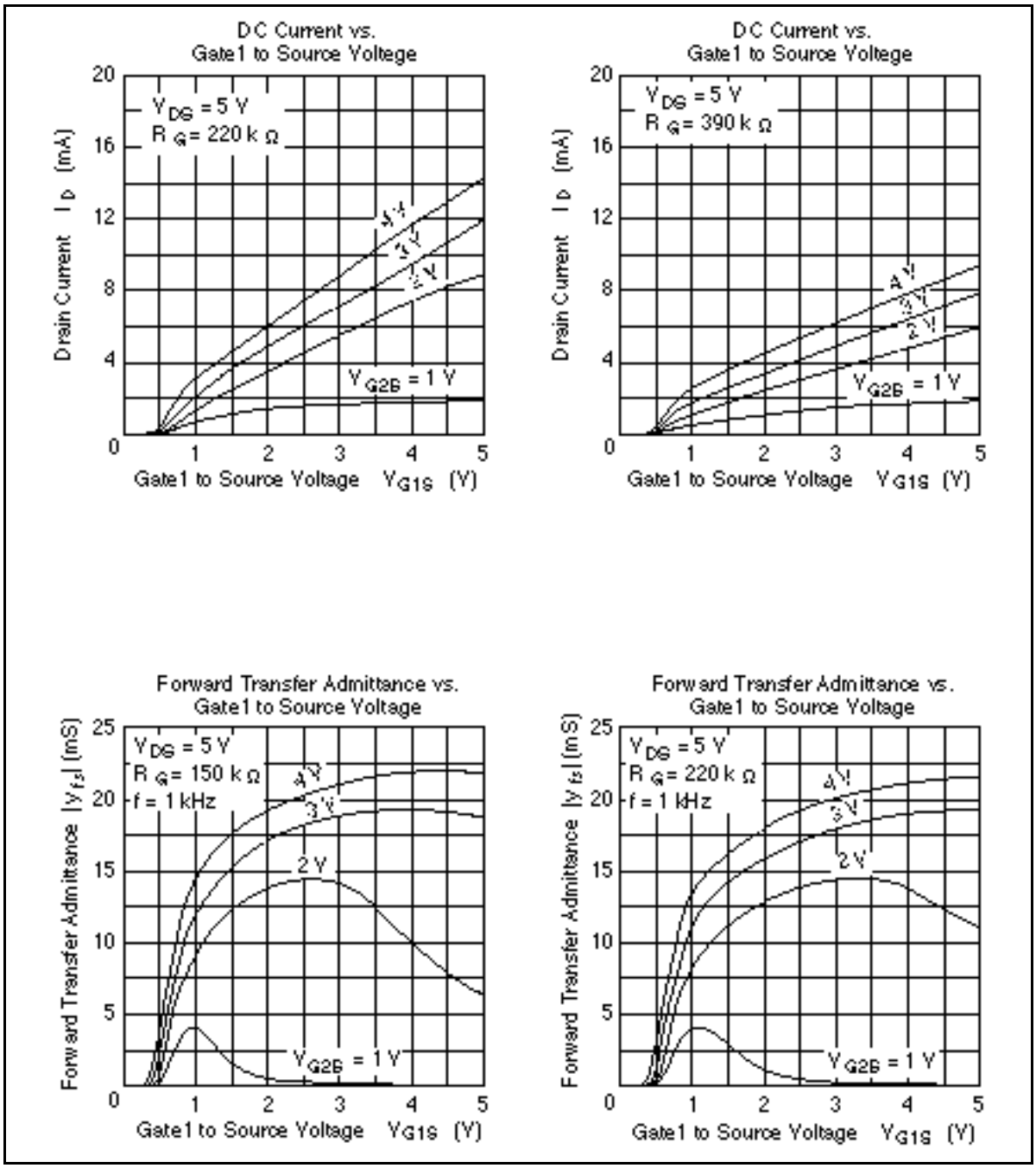


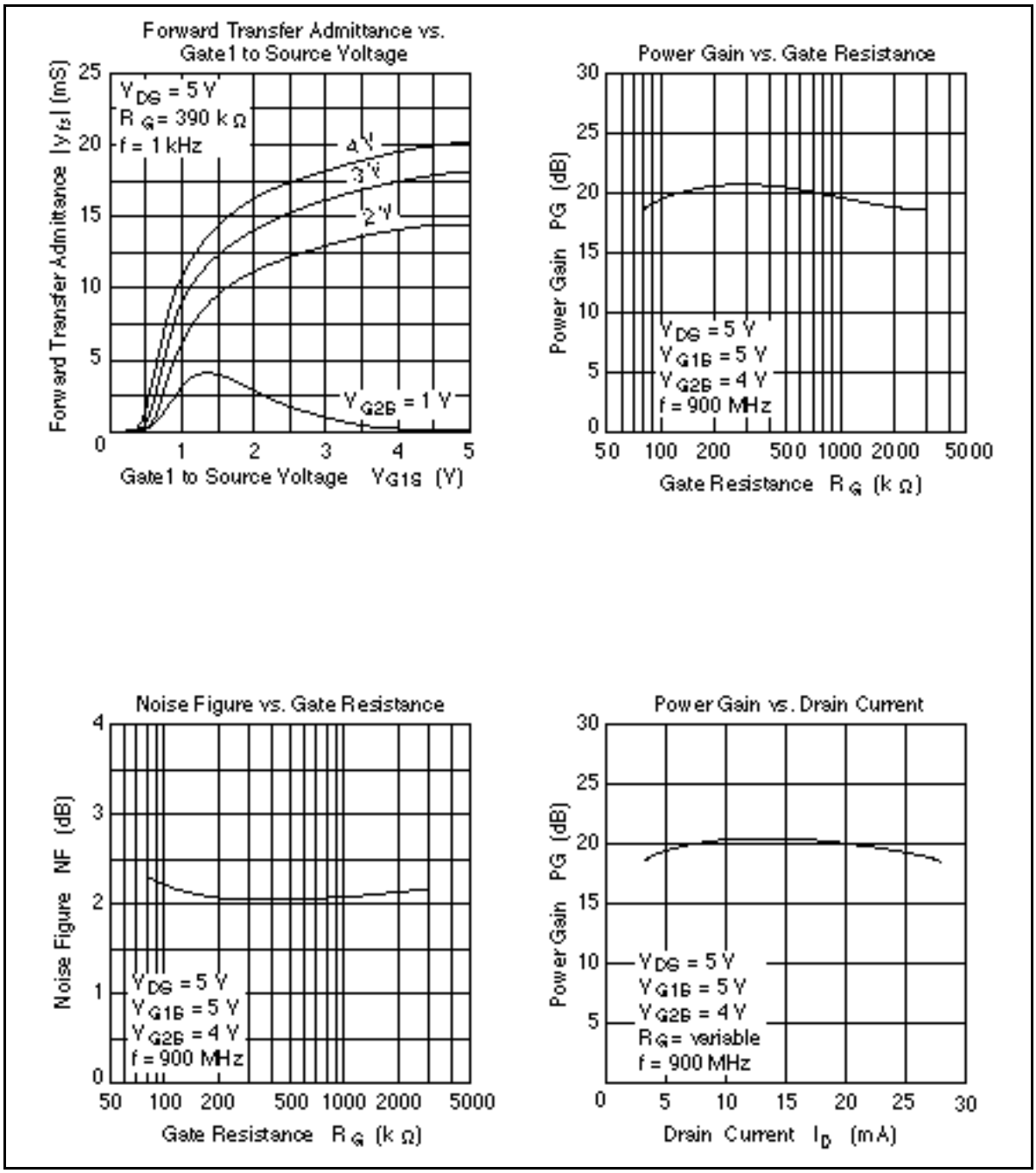
L4 :

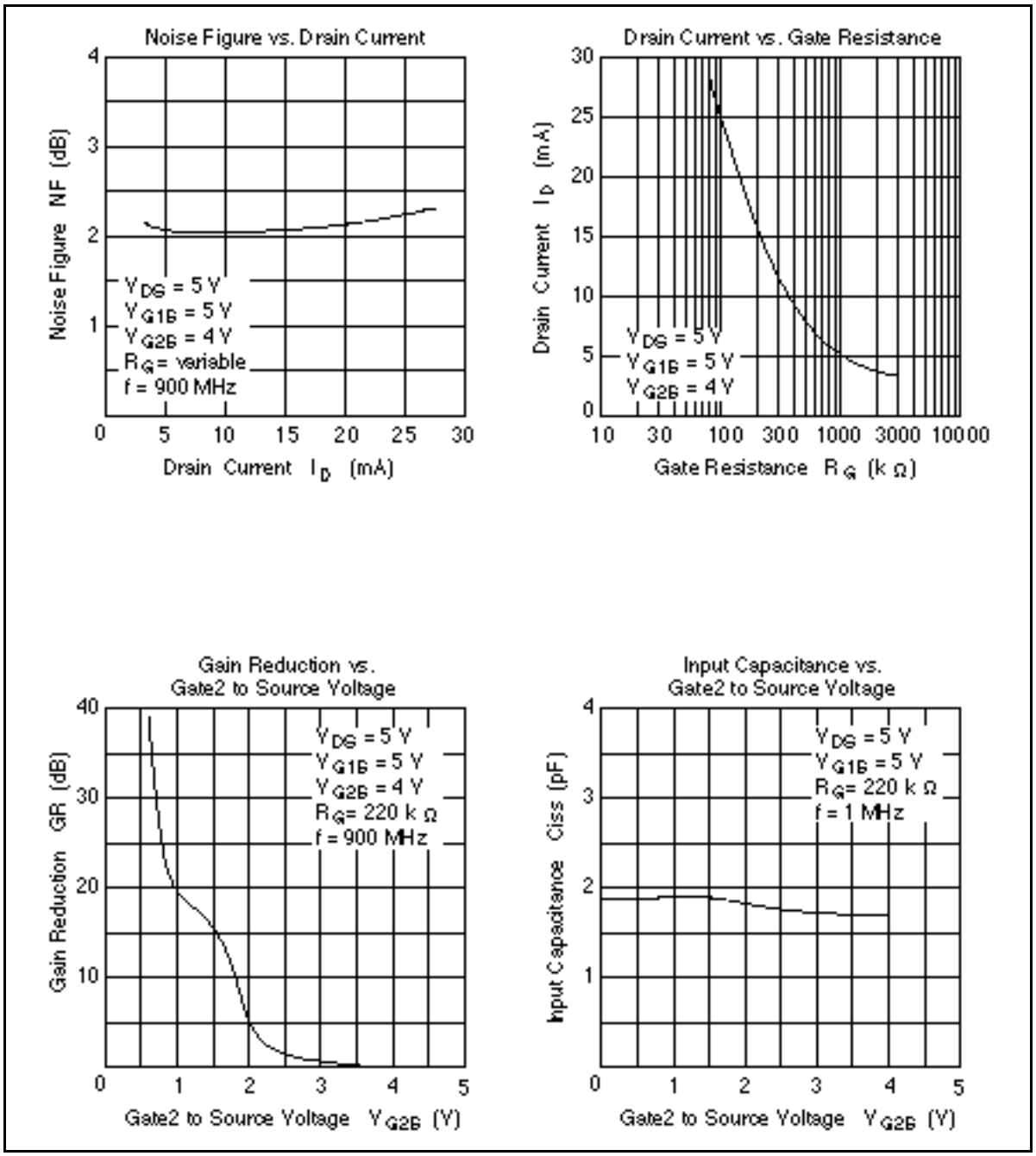


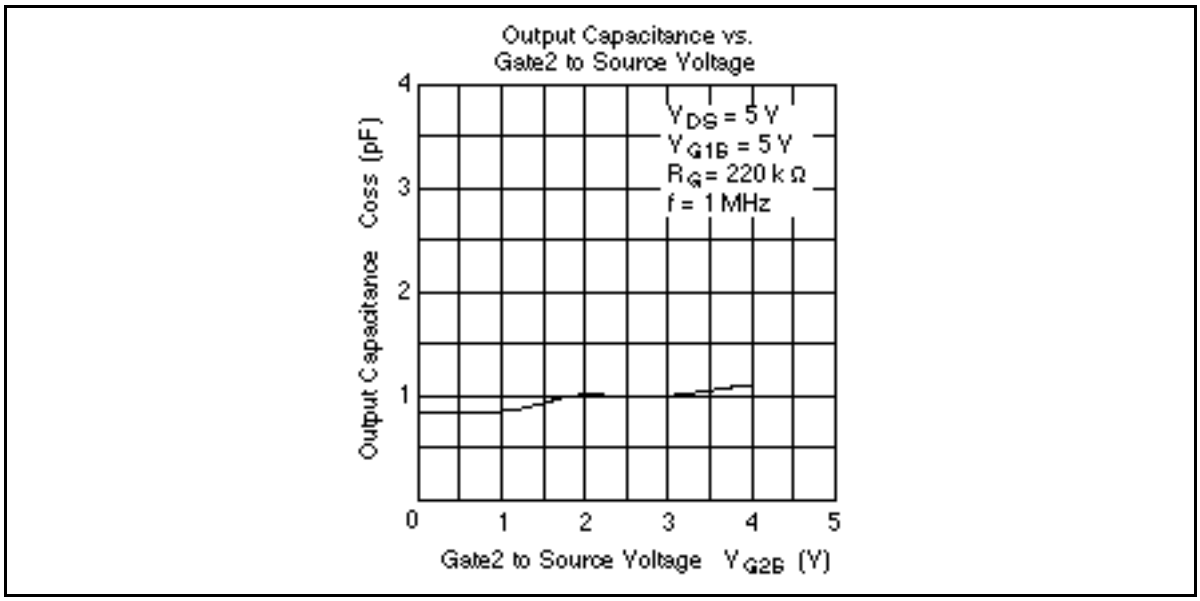
RFC : ϕ1mm Copper wire with enamel 4turns inside dia. 6mm


Power vs. Temperature Derating
Channel Dissipation Pch (mW)
200
150
100
50
0
50
100
150
200
Ambient Temperature Ta (°C)
Typical Output Characteristics
V_{G2S} = 4 V
Drain Current I_D (mA)
25
20
15
10
5
0
1
2
3
4
5
Drain to Source Voltage V_{DS} (V)
DC Current vs.
Gate2 to Source Voltage
V_{DD} = V_{GG} = 5 V
Drain Current I_D (mA)
25
20
15
10
5
0
1
2
3
4
5
Gate2 to Source Voltage V_{G2S} (V)
DC Current vs.
Gate1 to Source Voltage
V_{DS} = 5 V
R_G = 150 kΩ
Drain Current I_D (mA)
20
16
12
8
4
0
1
2
3
4
5
V_{G2S} = 1 V
Gate1 to Source Voltage V_{G1S} (V)


DC Current vs.
Gate1 to Source Voltage
V_{DS} = 5 V
R_G = 220 kΩ
Drain Current I_D (mA)
Gate1 to Source Voltage V_{G1S} (V)
V_{G2S} = 1 V
DC Current vs.
Gate1 to Source Voltage
V_{DS} = 5 V
R_G = 390 kΩ
Drain Current I_D (mA)
Gate1 to Source Voltage V_{G1S} (V)
V_{G2S} = 1 V
Forward Transfer Admittance vs.
Gate1 to Source Voltage
V_{DS} = 5 V
R_G = 150 kΩ
f = 1 kHz
Forward Transfer Admittance $|y_{fs}|$ (mS)
Gate1 to Source Voltage V_{G1S} (V)
4 V
3 V
2 V
V_{G2S} = 1 V
Forward Transfer Admittance vs.
Gate1 to Source Voltage
V_{DS} = 5 V
R_G = 220 kΩ
f = 1 kHz
Forward Transfer Admittance $|y_{fs}|$ (mS)
Gate1 to Source Voltage V_{G1S} (V)
4 V
3 V
2 V
V_{G2S} = 1 V


Forward Transfer Admittance vs. Gate1 to Source Voltage
Forward Transfer Admittance |yfs| (mS)
VDS = 5 V
RG = 390 kΩ
f = 1 kHz
4 V
3 V
2 V
VG2S = 1 V
Gate1 to Source Voltage VG1S (V)
Power Gain vs. Gate Resistance
Power Gain PG (dB)
VDS = 5 V
VG1S = 5 V
VG2S = 4 V
f = 900 MHz
Gate Resistance RG (kΩ)
Noise Figure vs. Gate Resistance
Noise Figure NF (dB)
VDS = 5 V
VG1S = 5 V
VG2S = 4 V
f = 900 MHz
Gate Resistance RG (kΩ)
Power Gain vs. Drain Current
Power Gain PG (dB)
VDS = 5 V
VG1S = 5 V
VG2S = 4 V
RG = variable
f = 900 MHz
Drain Current ID (mA)


Noise Figure vs. Drain Current
Noise Figure NF (dB)
Drain Current I_D (mA)
V_{DS} = 5 V
V_{G1S} = 5 V
V_{G2S} = 4 V
R_G = variable
f = 900 MHz
Drain Current vs. Gate Resistance
Drain Current I_D (mA)
Gate Resistance R_G (k Ω)
V_{DS} = 5 V
V_{G1S} = 5 V
V_{G2S} = 4 V
Gain Reduction vs.
Gate2 to Source Voltage
Gain Reduction GR (dB)
Gate2 to Source Voltage V_{G2S} (Y)
V_{DS} = 5 V
V_{G1S} = 5 V
V_{G2S} = 4 V
R_G = 220 k Ω
f = 900 MHz
Input Capacitance vs.
Gate2 to Source Voltage
Input Capacitance Ciss (pF)
Gate2 to Source Voltage V_{G2S} (Y)
V_{DS} = 5 V
V_{G1S} = 5 V
R_G = 220 k Ω
f = 1 MHz


Output Capacitance vs.
Gate2 to Source Voltage
V_{DS} = 5 V
V_{G1S} = 5 V
R_G = 220 kΩ
f = 1 MHz
Output Capacitance Coss (pF)
0
1
2
3
4
5
Gate2 to Source Voltage V_{G2S} (V)

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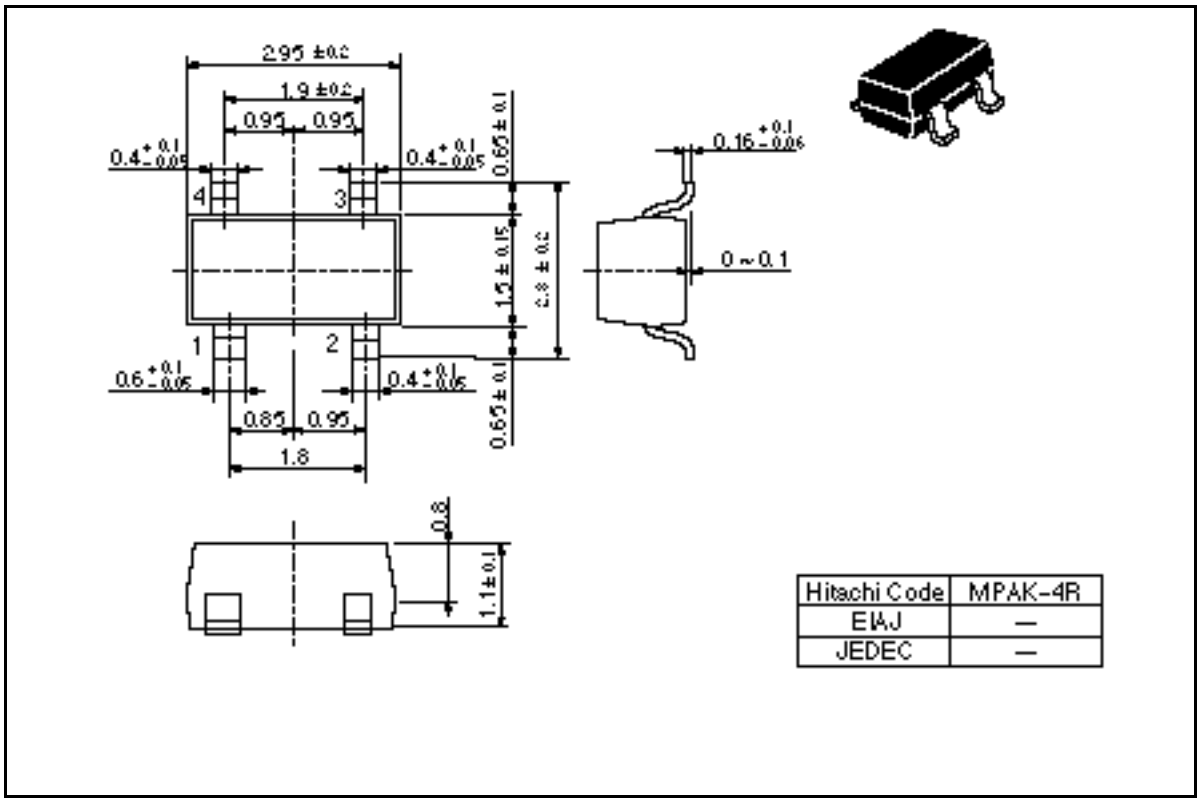
Package Dimensions

Unit: mm



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