PM5050J

Silicon N-Channel Power MOS FET Module

HITACHI

Application

High Speed Power Switching

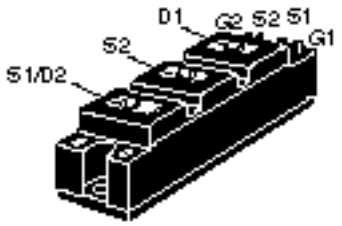
Features

- Equipped with Power MOS FET
- Low on-resistance
- High speed switching
- Low drive current
- Wide area of safe operation
- Inherent parallel diode between source and drain
- Isolated base from Terminal
- Suitable for motor driver, switching regulator and etc.

PM5050J

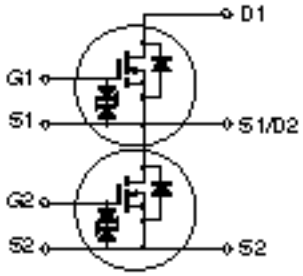
Outline

LF-J



No	Electrode	Terminale	Remarke
S1	Source 1	M5 screw	Power terminal
D1	Drain 1	M5 screw	
S2	Source 2	M5 screw	
D2	Drain 2	M5 screw	
G1	Gate 1	#110	Signal terminale
S1	Source 1	#110	
G2	Gate 2	#110	
S2	Source 2	#110	

EquivalentCircuit



Absolute Maximum Ratings (Ta = 25°C) (Per FET chip)

Item	Symbol	Rating	Unit
Drain source voltage	$V_{(BR)DSS}$	500	V
Gate source voltage	$V_{(BR)GSS}$	±30	V
Drain current	I_D	50	A
Drain peak current	$I_{D(peak)}$	120	A
Body to drain diode reverse drain current	I_{DR}	50	A
Body to drain diode reverse peak current	$I_{DR(peak)}$	120	A
Channel dissipation	Pch*[1]	250	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–45 to +125	°C
Insulation dielectric	Viso*[2]	2000	Vrms

Notes: 1. Value at Ta = 25°C
2. Base to terminals AC minute

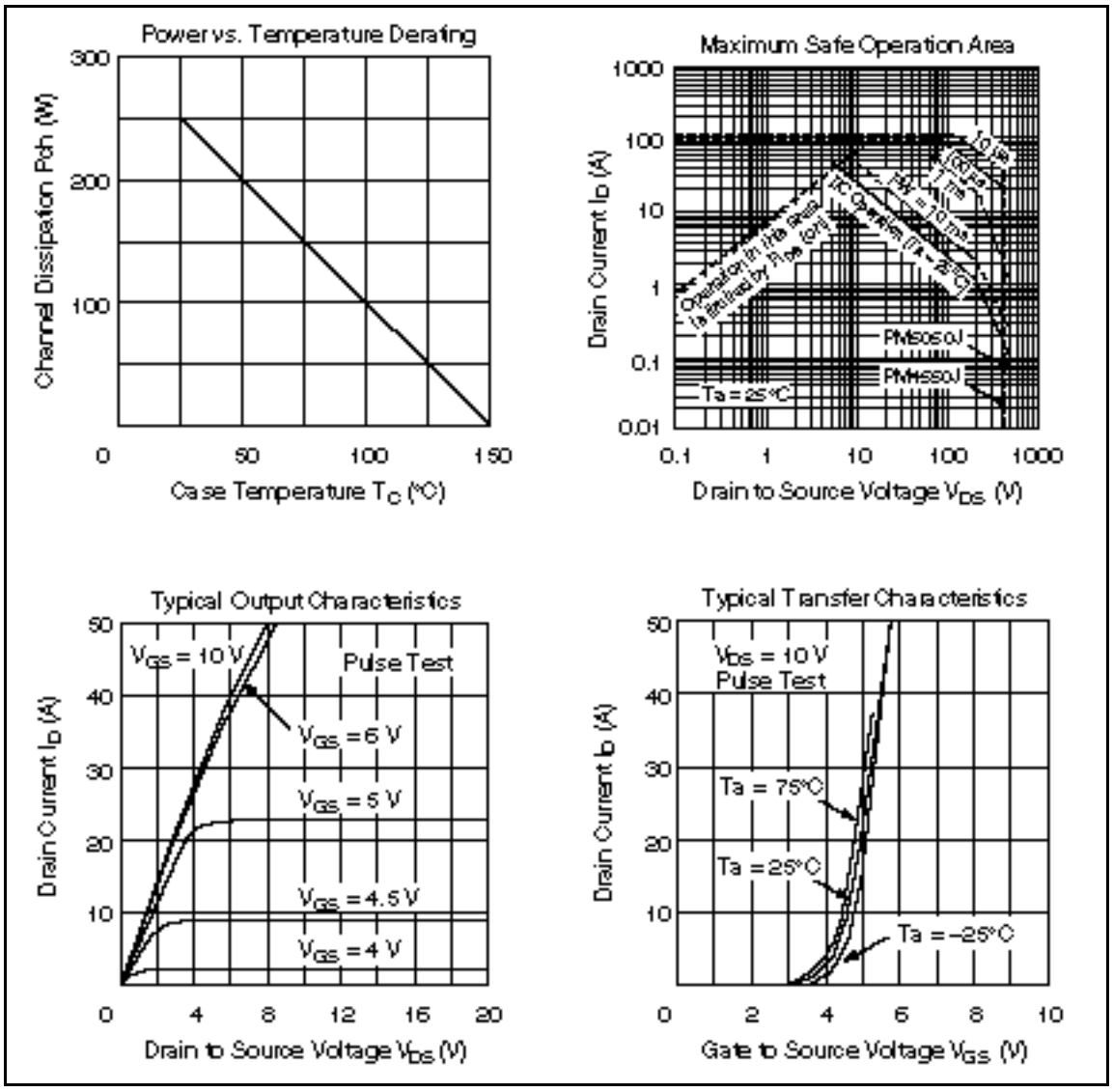
Electrical Characteristics (Ta = 25°C) (Per FET chip)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	I_D = 10 mA, V_{GS} = 0 V
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ± 25 V, V_{DS} = 0 V
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0 V
Drain leak current	I_{DSS}	—	—	500	µA	V_{DS} = 400 V, V_{GS} = 0 V
Gate to source threshold voltage	$V_{GS(th)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Drain to source saturation voltage	$V_{DS(on)}$	—	3.5	4.5	V	I_D = 25 A, V_{GS} = 10 V*[1]
Static drain to source on state resistance	$R_{DS(on)}$	—	0.14	0.18	Ω	I_D = 25 A, V_{GS} = 10 V*[1]
Forward transfer admittance	$\|y_{fs}\|$	—	30	—	S	I_D = 25 A, V_{DS} = 10 V*[1]
Input capacitance	Ciss	—	6600	—	pF	V_{DS} = 10 V, V_{GS} = 0 V
Output capacitance	Coss	—	1550	—		f = 1 MHz
Reverse transfer capacitance	Crss	—	250	—		
Turn-on delay time	$t_{d(on)}$	—	45	—	ns	I_D = 25 A, V_{GS} = 10 V
Rise time	t_r	—	270	—		Rg = 50 Ω
Turn-off delay time	$t_{d(off)}$	—	250	—		R_L = 1.2 Ω
Fall time	t_f	—	140	—		
Body to drain diode forward voltage	V_{DF}	—	1.6	—	V	I_F = 50 A, V_{GS} = 0 V
Body to drain diode reverse recovery time	t_{rr}	—	130	—	ns	I_F = 50 A, V_{GS} = 0 V di/dt = 100 A/µs

Note: 1. Pulse Test

Mechanical Characteristics

Item	Symbol	Condition	Rating	Unit
Fixing strength	—	Mounting into main-terminal with M4 screw	1.45 to 1.95	N-m
	—	Mounting into heat sink with M5 screw	1.95 to 2.9	N-m
Weight	—	Typical value	200	g


Power vs. Temperature Derating
Channel Dissipation Pch (W)
300
200
100
0
50
100
150
Case Temperature T_C (°C)
Maximum Safe Operation Area
Drain Current I_D (A)
1000
100
10
1
0.1
0.01
0.1
1
10
100
1000
Drain to Source Voltage V_{DS} (V)
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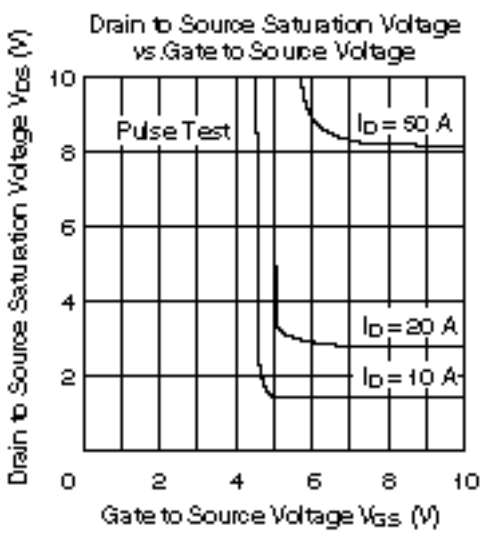
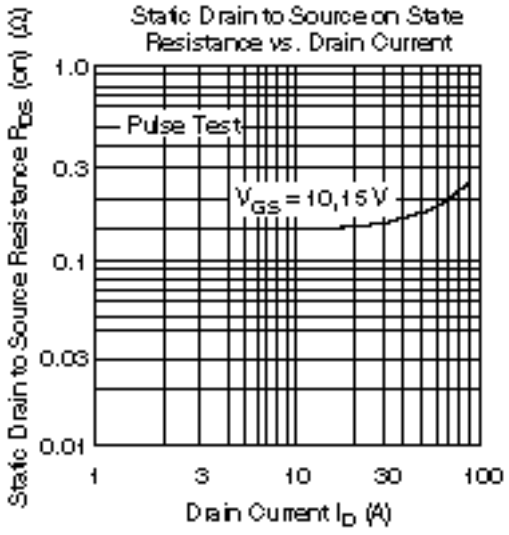
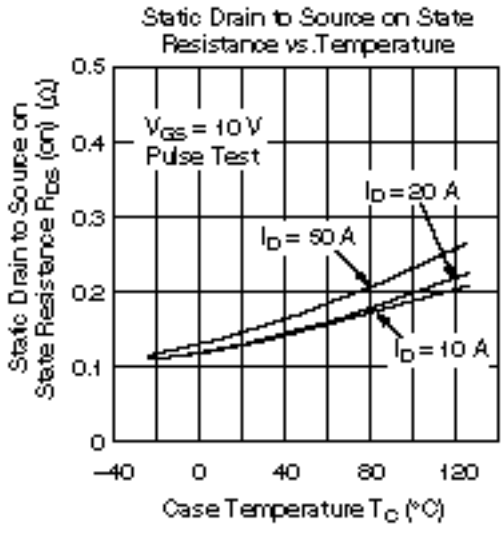
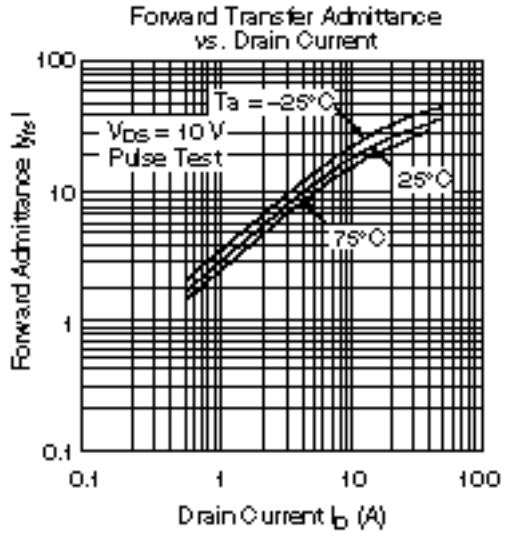
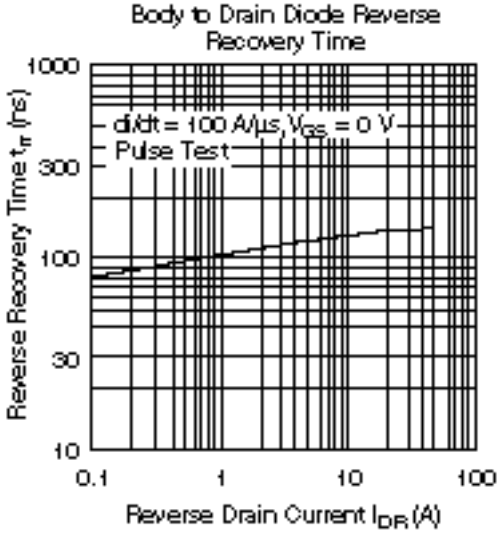
Ta = 25°C
Typical Output Characteristics
Drain Current I_D (A)
50
40
30
20
10
0
4
8
12
16
20
Drain to Source Voltage V_{DS} (V)
V_{GS} = 10 V
Pulse Test
V_{GS} = 6 V
V_{GS} = 5 V
V_{GS} = 4.5 V
V_{GS} = 4 V
Typical Transfer Characteristics
Drain Current I_D (A)
50
40
30
20
10
0
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)
V_{DS} = 10 V
Pulse Test
Ta = 75°C
Ta = 25°C
Ta = –25°C

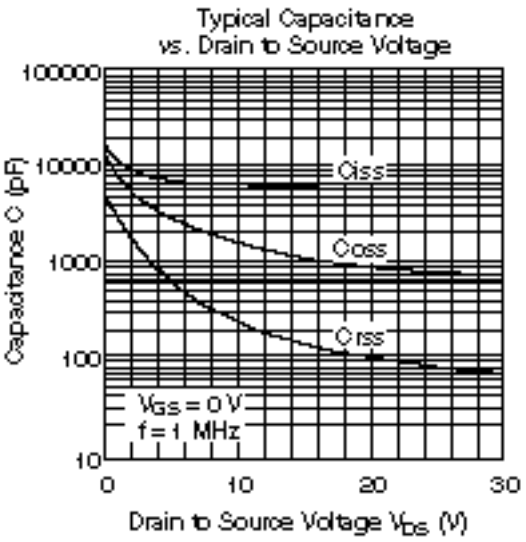

Drain to Source Saturation Voltage vs.Gate to Source Voltage
Drain to Source Saturation Voltage V_{DS} (V)
Pulse Test
I_D = 50 A
I_D = 20 A
I_D = 10 A
Gate to Source Voltage V_{GS} (V)

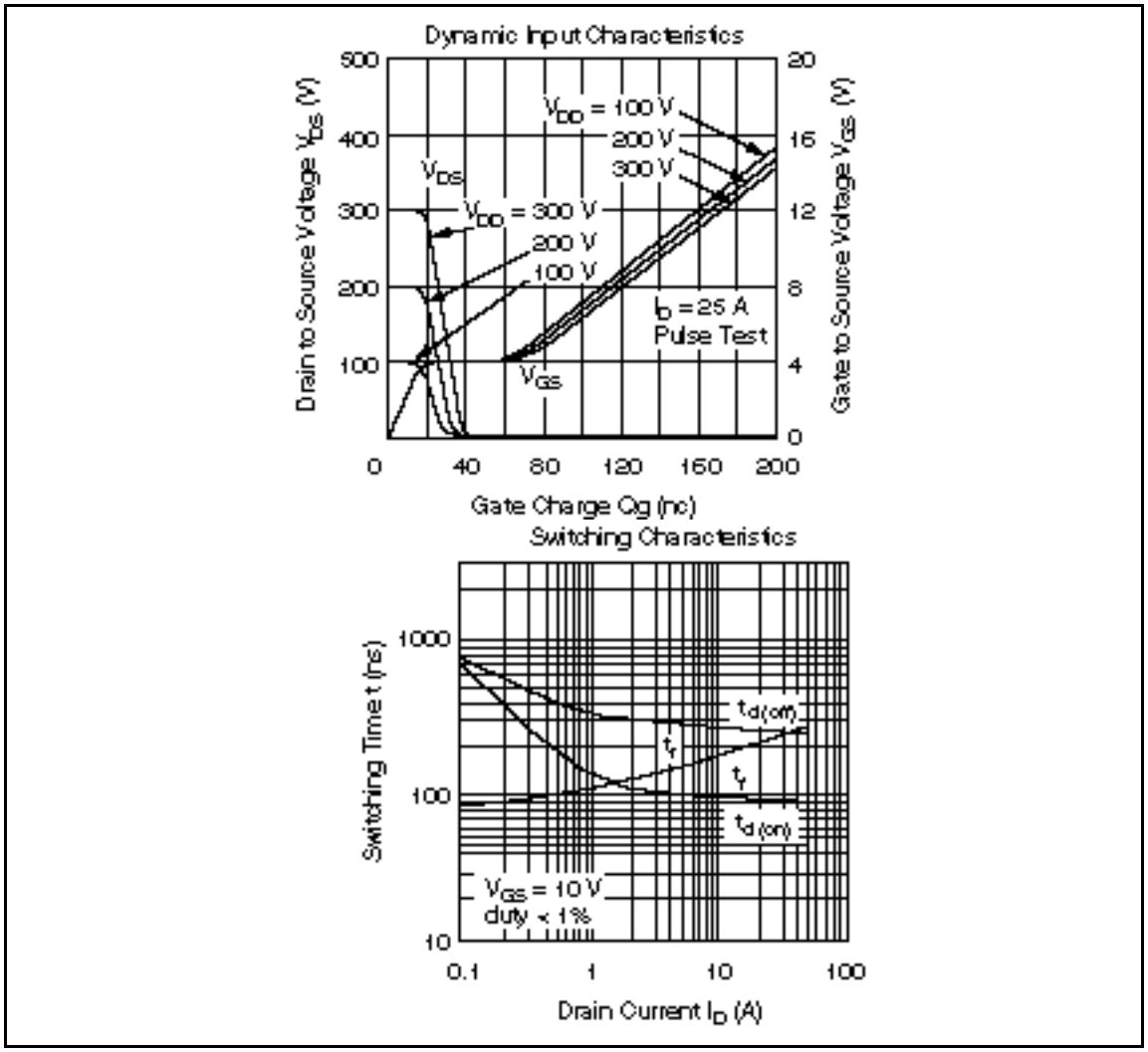

Static Drain to Source on State Resistance vs. Drain Current
Static Drain to Source Resistance R_{DS} (on) (Ω)
Pulse Test
V_{GS} = 10, 15 V
Drain Current I_D (A)

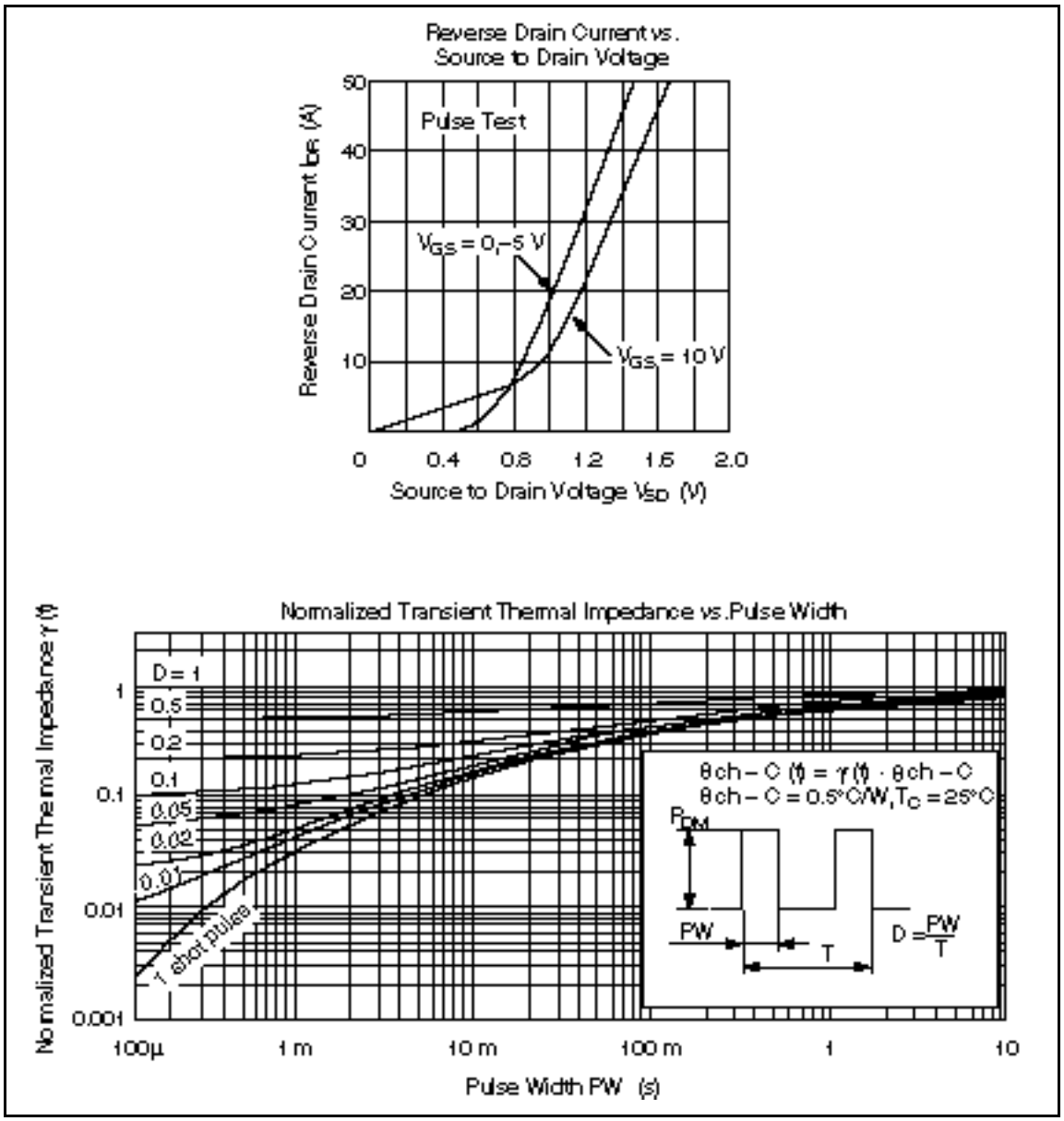

Static Drain to Source on State Resistance vs.Temperature
Static Drain to Source on State Resistance R_{DS} (on) (Ω)
V_{GS} = 10 V
Pulse Test
I_D = 20 A
I_D = 50 A
I_D = 10 A
Case Temperature T_C (°C)


Forward Transfer Admittance vs. Drain Current
Forward Admittance |y_{fs}|
Ta = −25°C
V_{DS} = 10 V
Pulse Test
25°C
75°C
Drain Current I_D (A)

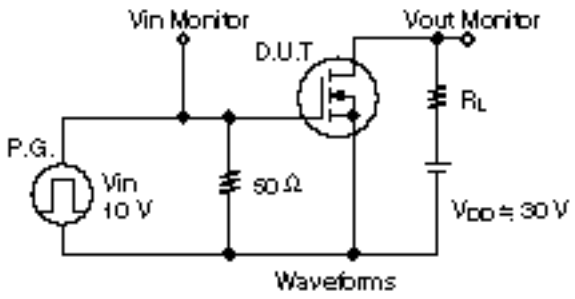

Body to Drain Diode Reverse Recovery Time
Reverse Recovery Time t_{rr} (ns)
1000
300
100
30
10
di/dt = 100 A/µs, V_{GS} = 0 V
Pulse Test
0.1
1
10
100
Reverse Drain Current I_{DR} (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
100000
10000
1000
100
10
Ciss
Coss
Crss
V_{GS} = 0 V
f = 1 MHz
0
10
20
30
Drain to Source Voltage V_{DS} (V)

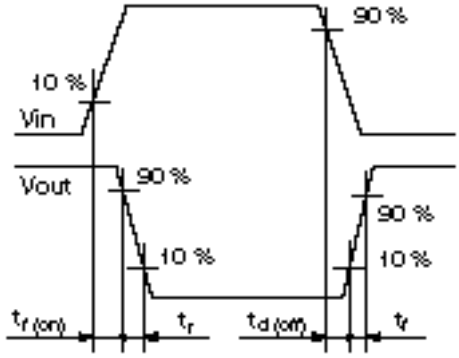

Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
V_{DD} = 100 V
200 V
300 V
V_{DS}
V_{DD} = 300 V
200 V
100 V
I_D = 25 A
Pulse Test
V_{GS}
Gate Charge Qg (nc)
Switching Characteristics
Switching Time t (ns)
$t_{d(off)}$
t_f
t_r
$t_{d(on)}$
V_{GS} = 10 V
duty < 1%
Drain Current I_D (A)


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 0, −5 V
V_{GS} = 10 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
50
40
30
20
10
0
0.4
0.8
1.2
1.6
2.0
Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ (t)
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot pulse
1
0.1
0.01
0.001
100µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)
θch − C (t) = γ (t) · θch − C
θch − C = 0.5°C/W, T_C = 25°C
P_{DM}
PW
T
D = PW/T

Switching Time Test Circuit



Waveforms



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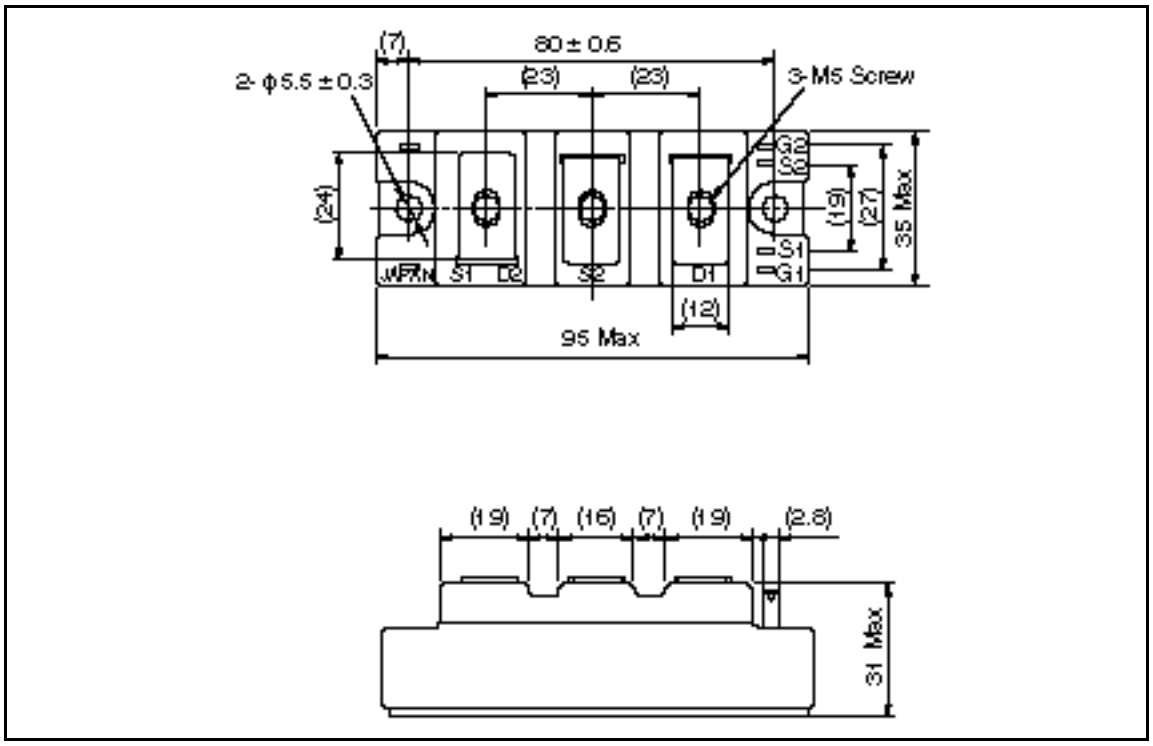
Package Dimensions

Unit: mm



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