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# PF0231A

MOS FET Power Amplifier Module for ADC Handy Phone

HITACHI

ADE-208-378A (Z)
2nd. Edition
July 1996

## Application

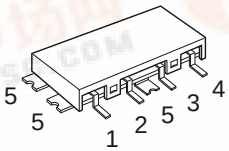
For ADC class3 824 to 849 MHz

## Features

- Low voltage operation 4.8 V
- High efficiency: 42% Typ for CW
  34% Typ for π/4-DQPSK
- Simple Pout control: Controllable by VAPC
- Low power control current: 600 µA Typ.

## Pin Arrangement

• RF-E




1: Pin
2: $V_{APC}$
3: $V_{DD}$
4: Pout
5: GND

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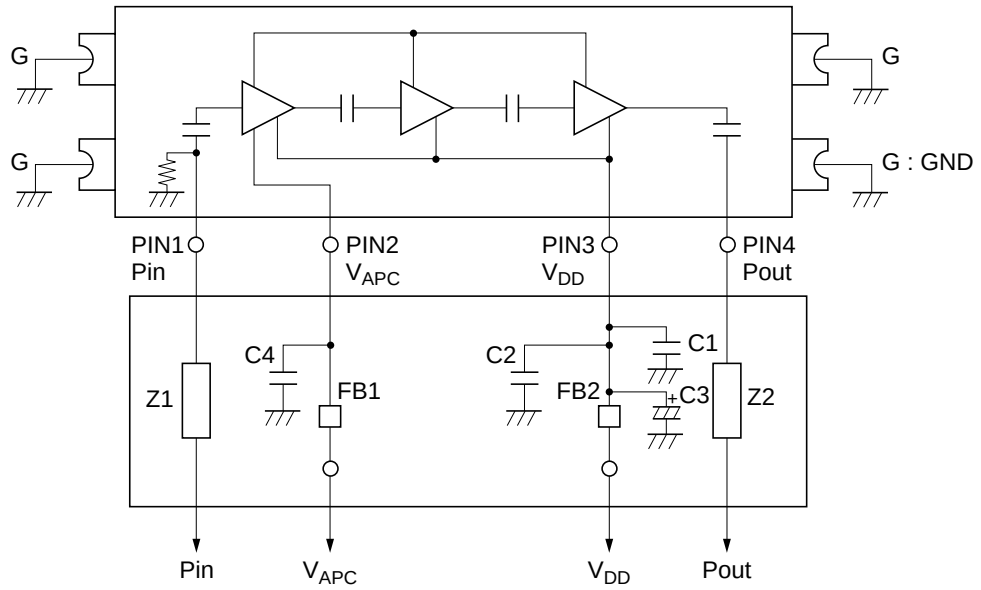
## Internal Diagram and External Circuit




C1 = C4 = 0.01 µF (Ceramic chip)
C2 = 4.7 µF (Tantalum)
C3 = 220 µF (Aluminum electrolyte)
FB = Ferrite bead BL01RN1-A62-001 (Manufacturer: MURATA) or equivalent
Z1 = Z2 = 50 Ω (Micro strip line)

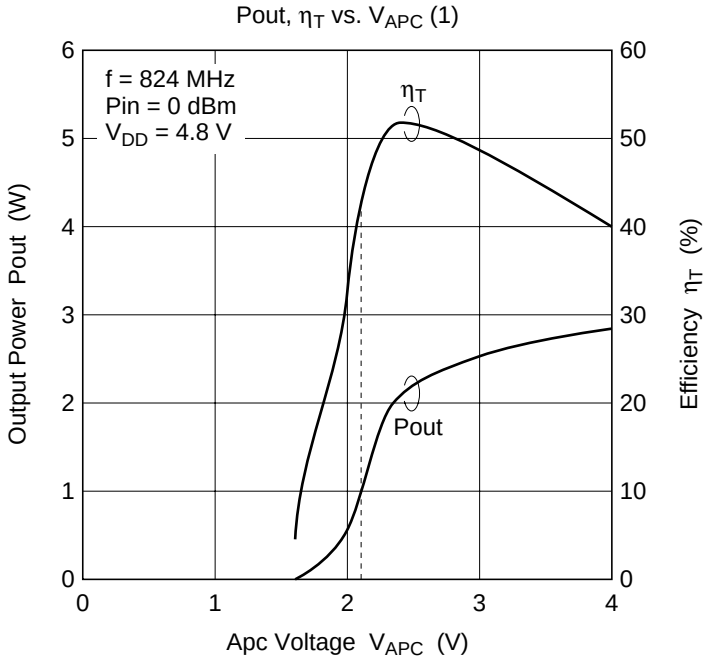
## Absolute Maximum Ratings (Tc = 25°C)

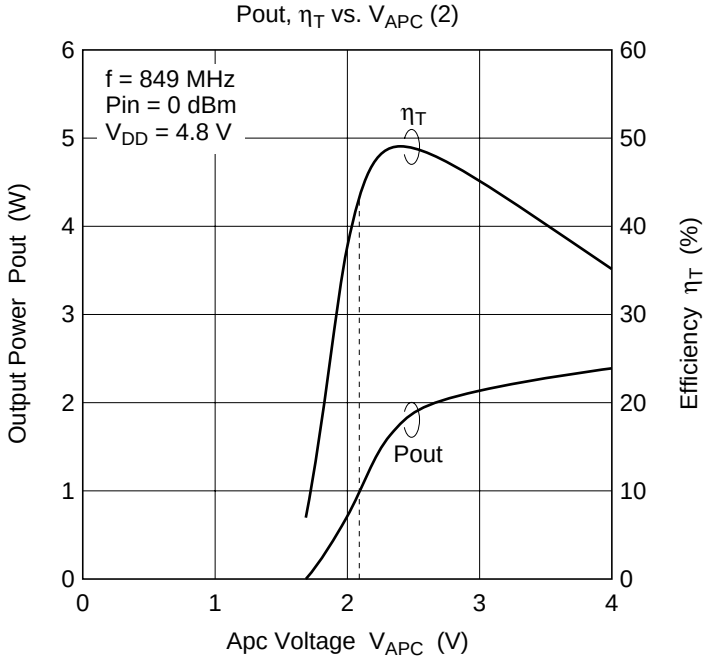
| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | VDD | 10 | V |
| Supply current | IDD | 1.5 | A |
| VAPC voltage | VAPC | 4.5 | V |
| Input power | Pin | 20 | mW |
| Operating case temperature | Tc (op) | –30 to +100 | °C |
| Storage temperature | Tstg | –30 to +100 | °C |

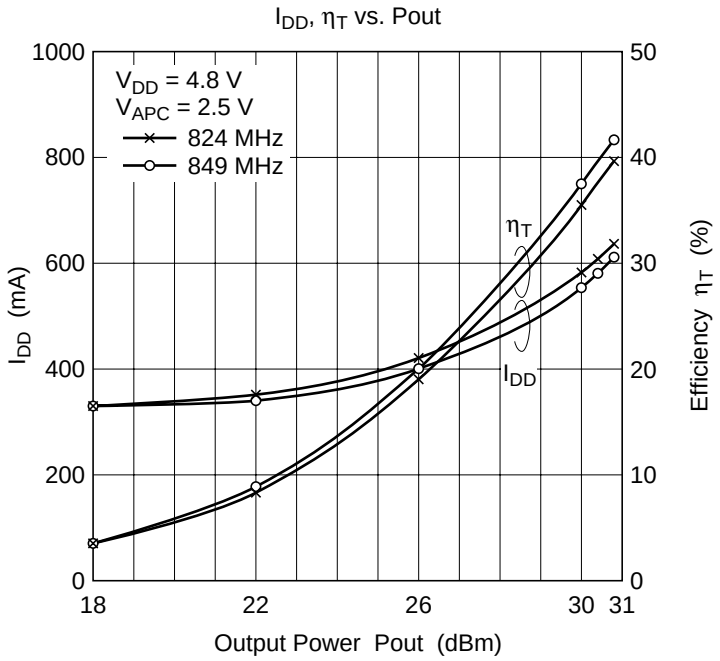
## **Electrical Characteristics** (Tc = 25°C)

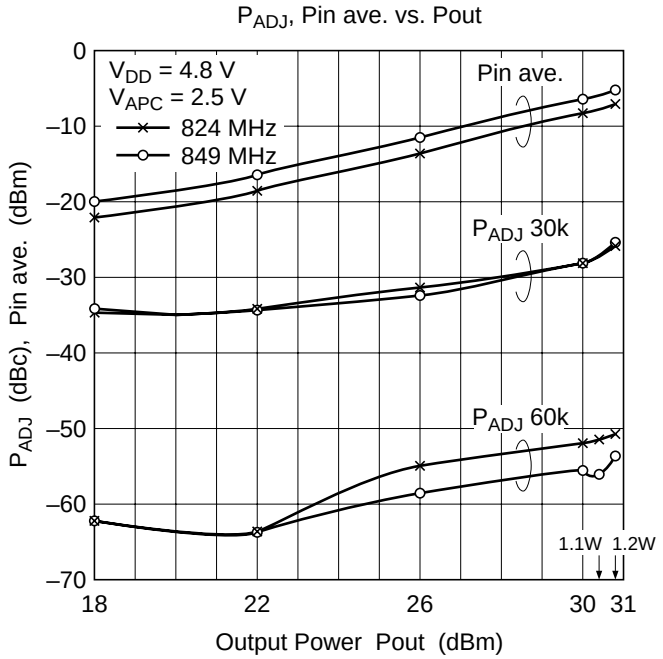
| Item | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Frequency range | f | 824 | — | 849 | MHz | — |
| Drain cutoff current | IDS | — | — | 100 | μA | VDD = 10 V, VAPC = 0 V |
| Total efficiency(1) | ηT (1) | 37 | 42 | — | % | Pin = 1 mW, VDD = 4.8 V, |
| 2nd harmonic distortion | 2nd H.D. | — | –35 | –30 | dBc | Pout = 1.2 W (at VAPC controlled), |
| 3rd harmonic distortion | 3rd H.D. | — | –40 | –30 | dBc | RL = Rg = 50 Ω |
| Input VSWR | VSWR (in) | — | 1.5 | 3 | — | |
| Output power | Pout | 1.6 | 2.1 | — | W | Pin = 1 mW, VDD = 4.8 V,<br>VAPC = 4.0 V, RL = Rg = 50 Ω |
| Isolation | — | — | –40 | –35 | dBm | Pin = 1 mW, VDD = 4.8 V,<br>VAPC = 0.5 V, RL = Rg = 50 Ω |
| Total efficiency(2) | ηT (2) | 30 | 34 | — | % | Pin = controlled (p/4-DQPSK, √α = |
| Adjacent channel | PADJ (30k) | — | –30 | –27 | dBc | 0.35, 48.6kbps), BW = 24.3 kHz with |
| leakage power | PADJ (60k) | — | –55 | –47 | dBc | R-NYQT, Pout = 1.0 W ave.,<br>VDD = 4.8 V, VAPC = 2.5 V |
| Load VSWR tolerance | — | No degradation | | | — | Pin = 1 mW, VDD = 6 V,<br>Pout ≤ 1.4 W,<br>t = 10 sec., Output VSWR = 20:1<br>All phases |
| Stability | — | No parasitic oscillation | | | — | Pin = 1 mW, VDD = 4 to 6 V,<br>Pout ≤ 1.4 W,<br>Output VSWR = 3:1 All phases,<br>Rg = 50 Ω |

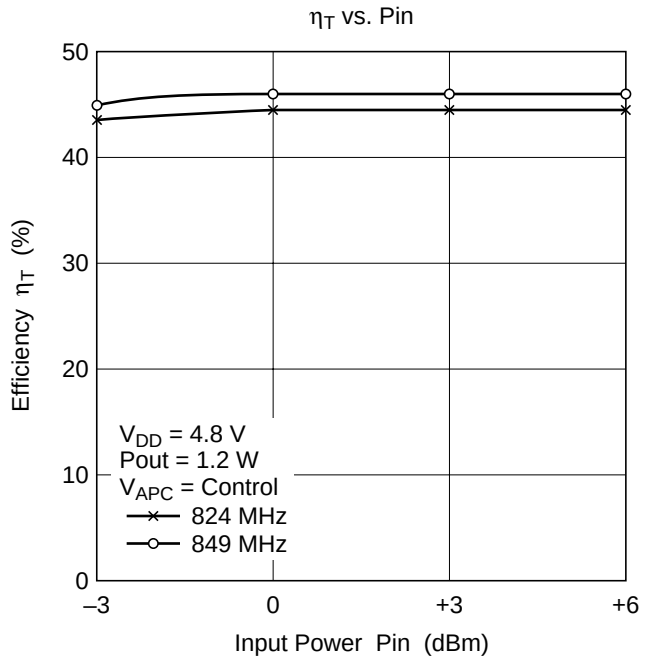
## Characteristics Curve

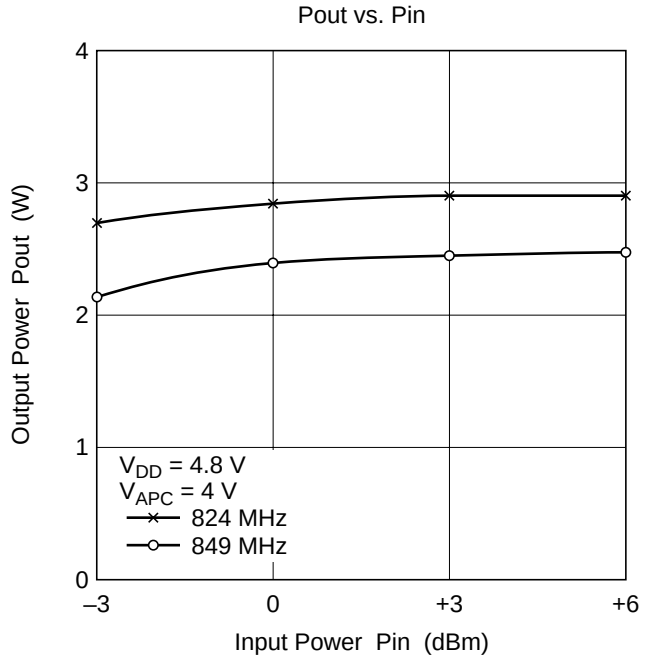


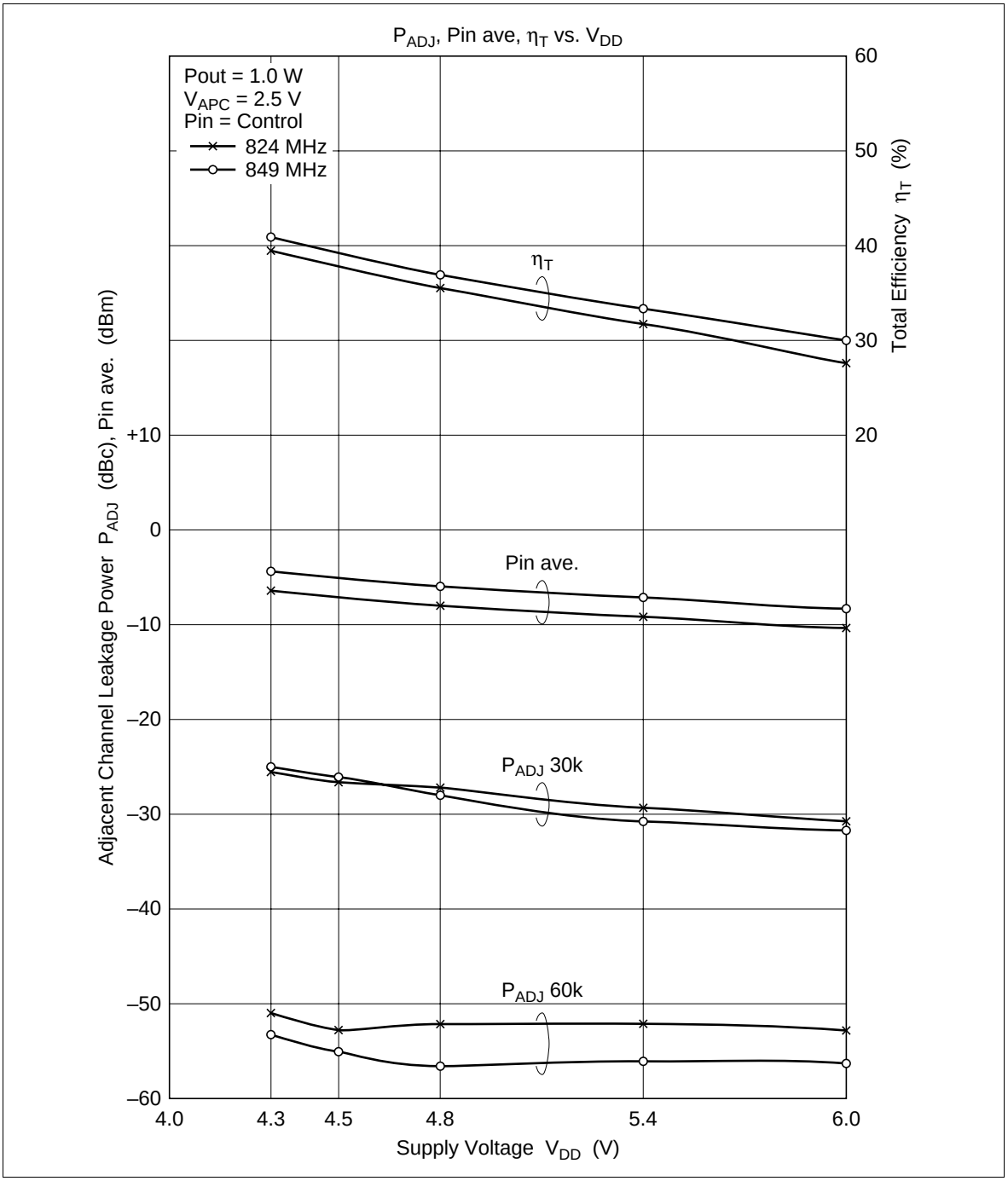



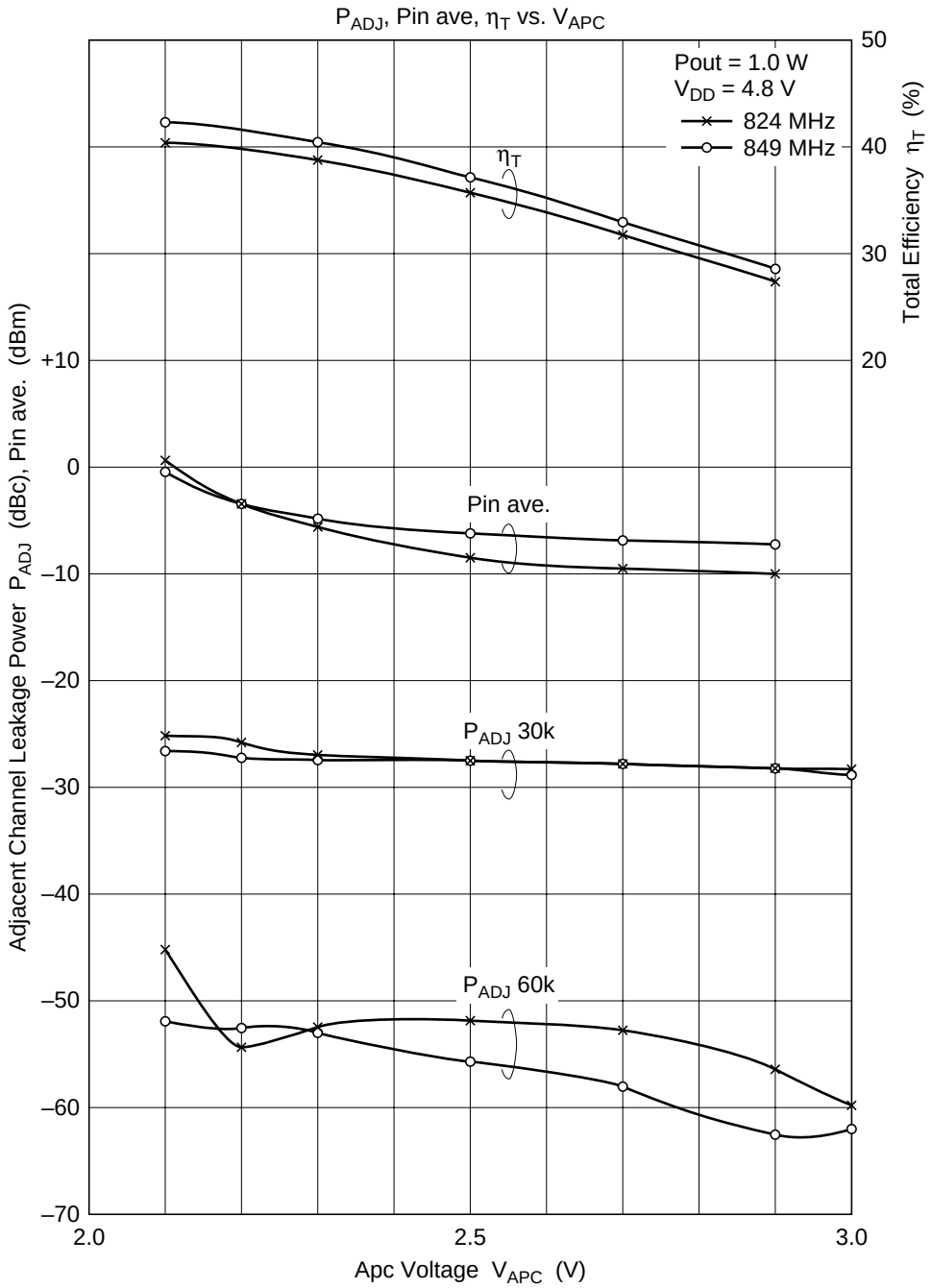

$I_{DD}$, $\eta_T$ vs. Pout
$V_{DD}$ = 4.8 V
$V_{APC}$ = 2.5 V
824 MHz
849 MHz
$\eta_T$
$I_{DD}$
$I_{DD}$ (mA)
Efficiency $\eta_T$ (%)
Output Power Pout (dBm)
1000
800
600
400
200
0
50
40
30
20
10
0
18
22
26
30
31


$P_{ADJ}$, Pin ave. vs. Pout
$V_{DD}$ = 4.8 V
$V_{APC}$ = 2.5 V
824 MHz
849 MHz
Pin ave.
$P_{ADJ}$ 30k
$P_{ADJ}$ 60k
1.1W
1.2W
$P_{ADJ}$ (dBc), Pin ave. (dBm)
Output Power Pout (dBm)
0
–10
–20
–30
–40
–50
–60
–70
18
22
26
30
31


ηT vs. Pin
50
40
30
20
10
0
Efficiency ηT (%)
VDD = 4.8 V
Pout = 1.2 W
VAPC = Control
824 MHz
849 MHz
–3
0
+3
+6
Input Power Pin (dBm)

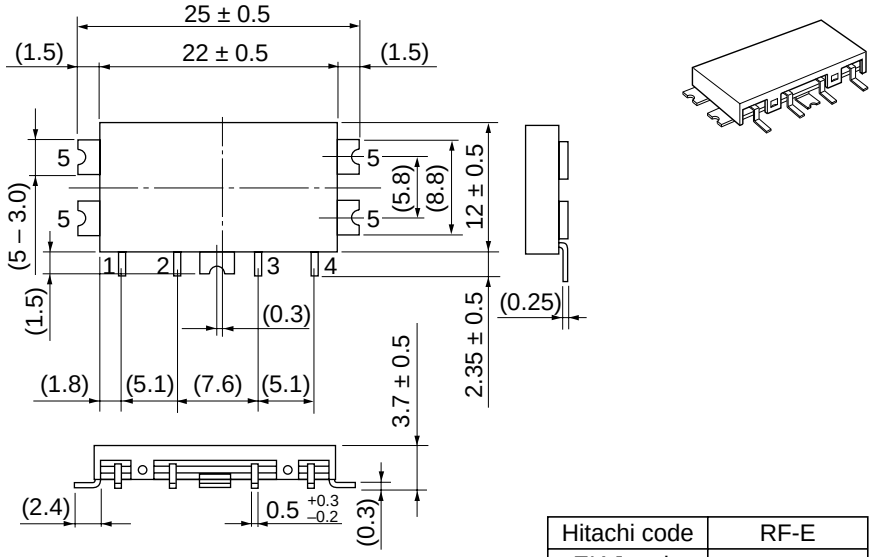

Pout vs. Pin
4
3
2
1
0
Output Power Pout (W)
VDD = 4.8 V
VAPC = 4 V
824 MHz
849 MHz
–3
0
+3
+6
Input Power Pin (dBm)


$P_{ADJ}$, Pin ave, $\eta_T$ vs. $V_{DD}$
Pout = 1.0 W
$V_{APC}$ = 2.5 V
Pin = Control
824 MHz
849 MHz
$\eta_T$
Pin ave.
$P_{ADJ}$ 30k
$P_{ADJ}$ 60k
Adjacent Channel Leakage Power $P_{ADJ}$ (dBc), Pin ave. (dBm)
Total Efficiency $\eta_T$ (%)
Supply Voltage $V_{DD}$ (V)
+10
0
–10
–20
–30
–40
–50
–60
60
50
40
30
20
4.0
4.3
4.5
4.8
5.4
6.0


$P_{ADJ}$, Pin ave, $\eta_T$ vs. $V_{APC}$
Pout = 1.0 W
$V_{DD}$ = 4.8 V
824 MHz
849 MHz
$\eta_T$
Pin ave.
$P_{ADJ}$ 30k
$P_{ADJ}$ 60k
Adjacent Channel Leakage Power $P_{ADJ}$ (dBc), Pin ave. (dBm)
Total Efficiency $\eta_T$ (%)
Apc Voltage $V_{APC}$ (V)
+10
0
–10
–20
–30
–40
–50
–60
–70
50
40
30
20
2.0
2.5
3.0

## Package Dimensions

Unit: mm




| | |
|---|---|
| Hitachi code | RF-E |
| EIAJ code | — |
| JEDEC code | — |