



## M5701

### DVD-ROM Controller

#### *Product Brief*

#### INTRODUCTION

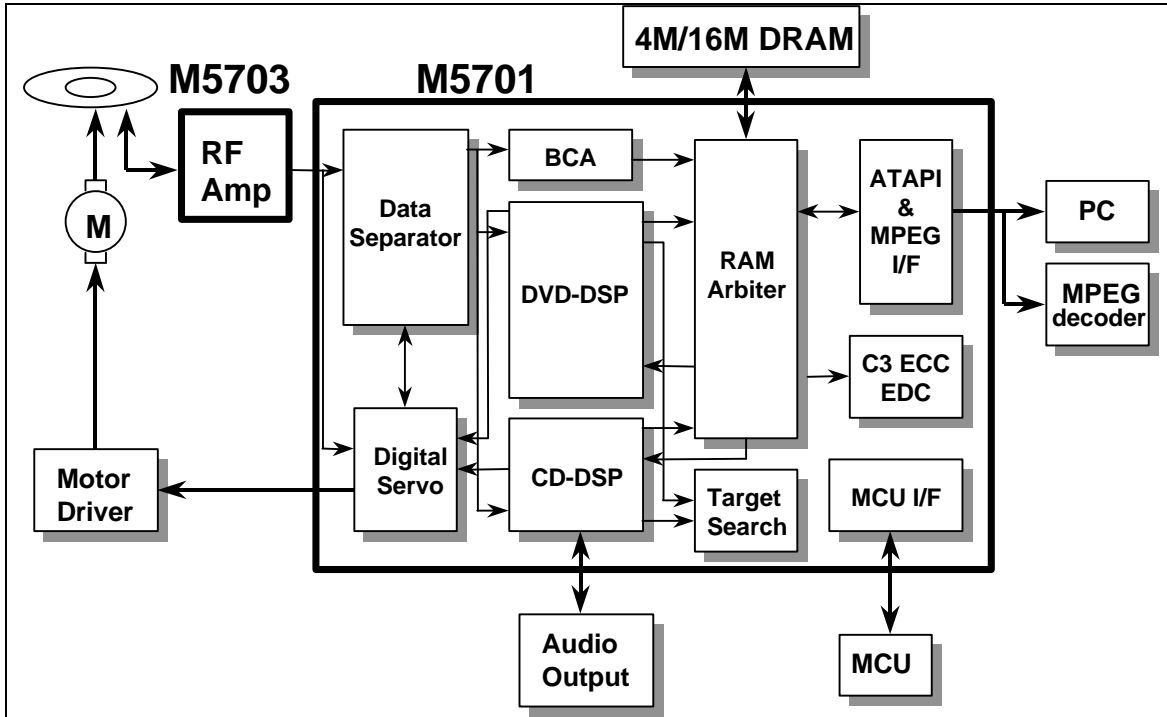
The M5701 is ALi's solution for DVD-ROM systems. The M5701 is a single chip that consists of DVD-Decoder, CD/CD-ROM Decoder, RAM buffer I/F, microcontroller I/F, ATAPI I/F and digital servo controller. The M5701 can work with M5703 - an RF signal processor, to do servo control and playback from CD/CD-ROM or DVD-ROM. The M5701 chip can support up to 8X DVD-ROM and 48X CD-ROM. This highly integrated chip supports not only the standard format of DVD-ROM disc, but also all the various CD-ROM disk types such as CD-DA, VCD, CDI, Photo CD, Karaoke CD, CD-plus, Enhanced CD, CD-R etc. This chipset can allow simplified, adjustment-free structuring of CD/DVD.

The microcontroller I/F supports a variety of microprocessors such as those of Intel's and Motorola's. The ATA interface can transfer data in Programmed I/O (PIO), DMA, ATA33 and ATA66 modes. It has a data transfer rate of up to 66 MB/sec (ATA66 timing). The RAM buffer I/F can support up to 16M bits EDO DRAM that has 16-bit data bus.

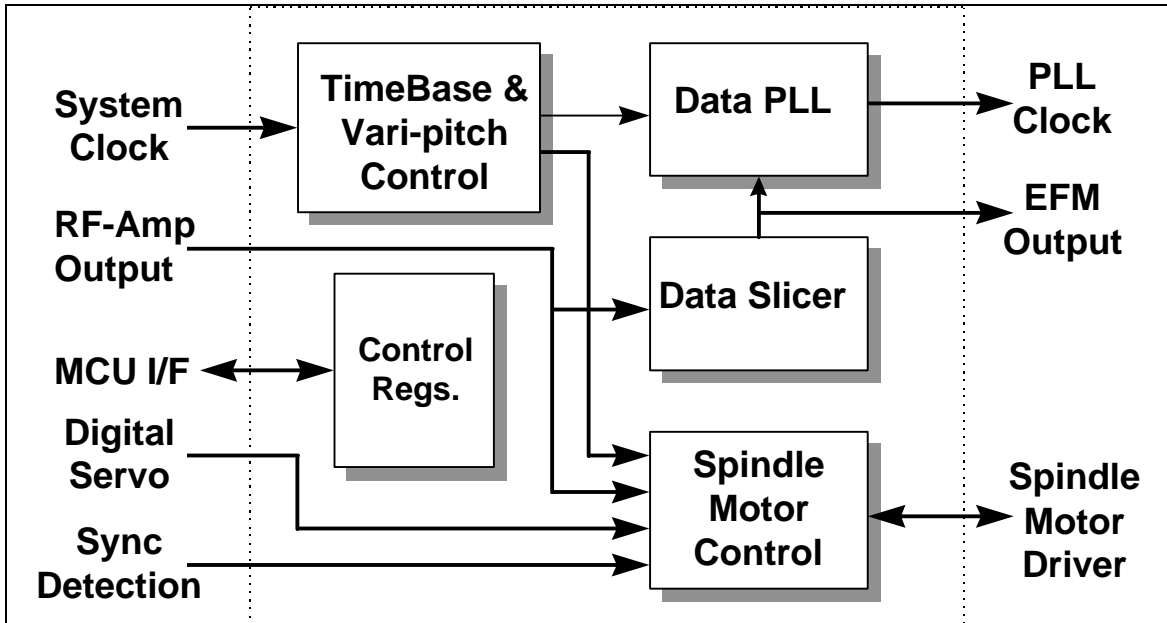
Furthermore, the M5701 is packed in a 208-pin (\*1) PQFP 0.35  $\mu$  CMOS process.

**\*1 : This is just the primary specification. They may be modified in the interval of development.**

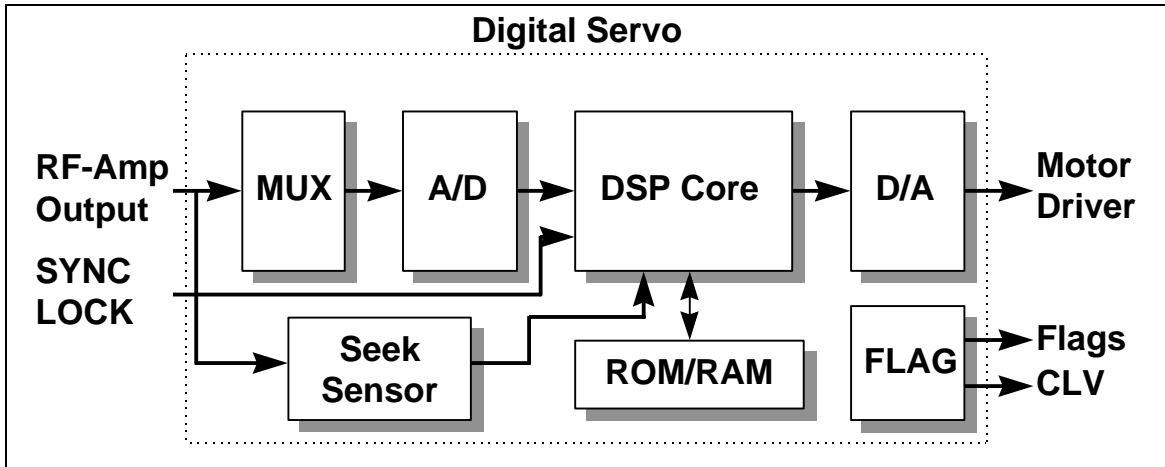
DVD-ROM System Diagram Integrated with M5701/M5703



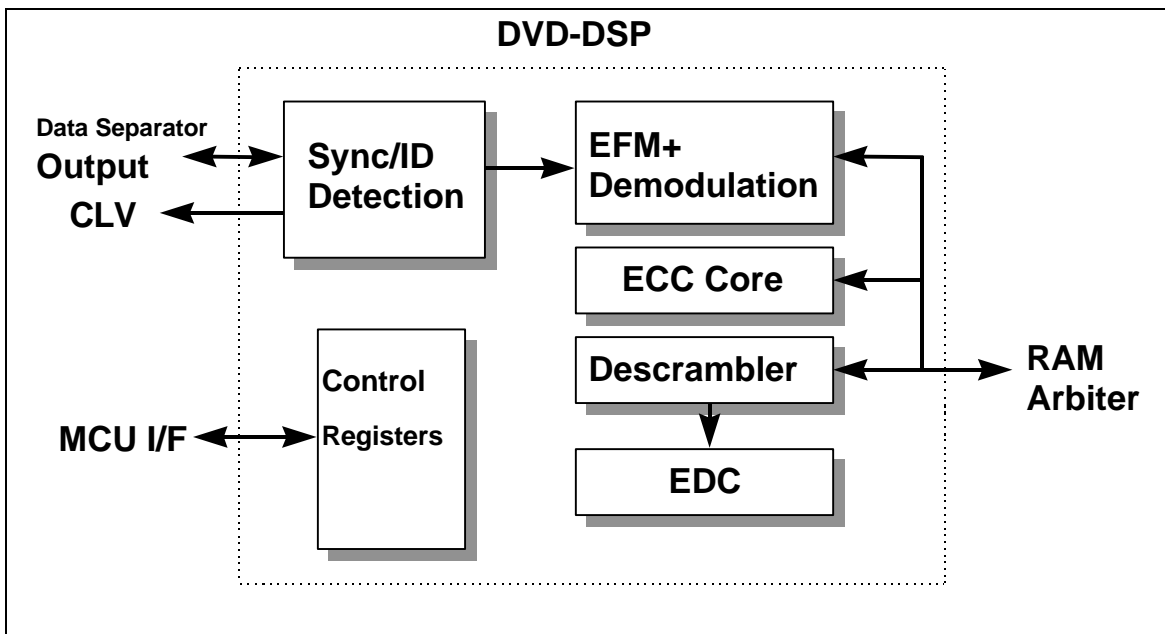
Data Separator Block Diagram



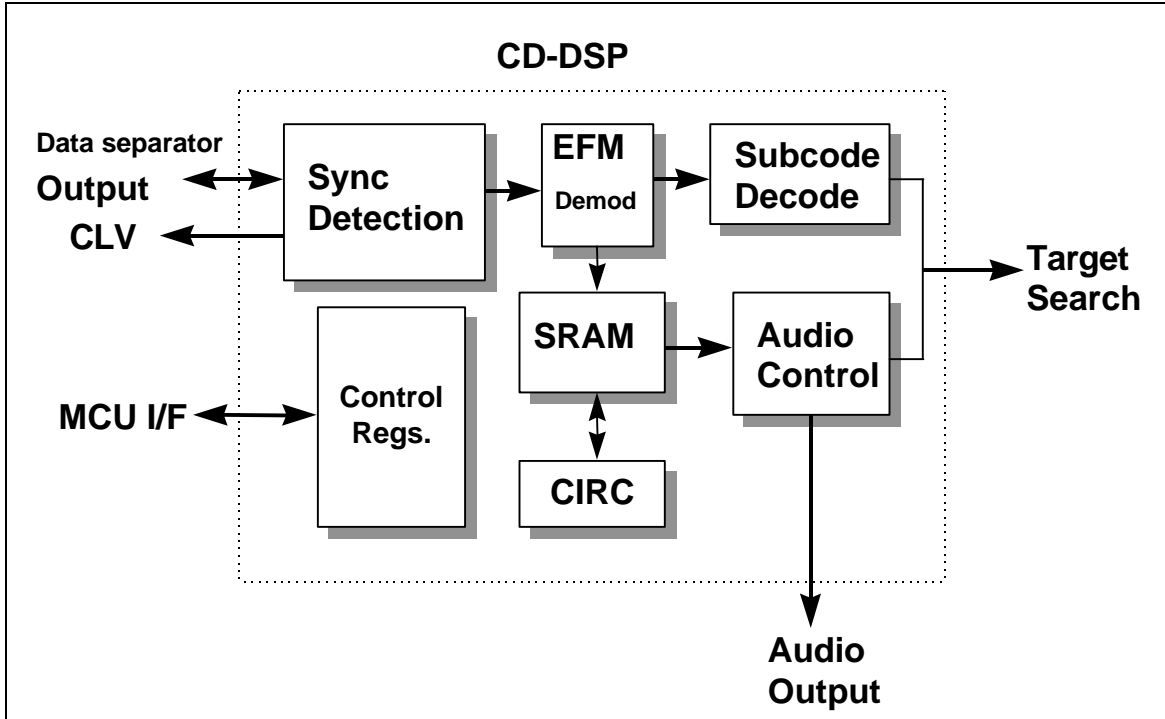
Digital Servo Block Diagram



DVD-DSP Block Diagram



CD-DSP Block Diagram



## Section 1 : Features list

### Data Separator

- Built in data slicer and data PLL.
- Built in clock synthesizer for various clock sources for servo control and data decoding part.
- Built in A/D and D/A converters for servo control signals processing.
- Built in "Seek Sensor" circuit for seek control.
- Built in CLV/CAV auxiliary circuit for servo control.

### DVD-DSP

- Built in synchronous pattern/ID detection /protection/separation.
- Built in EFM+ (8 to 16) demodulation circuit.
- Built in RSPC ECC circuit.
- Support up to 8X DVD-ROM system with ECC correcting "on the fly".
- Built in descrambler/EDC circuit.

### CD-DSP

- Synchronous pattern detection, protection and interpolation.
- Built in EFM demodulation circuit, subcode demodulation circuit.
- Capable of dual C1 correction and quadruple C2 correction using the CIRC correction theoretical format.
- Jitter absorbing capacity  $\pm 8$  frames.
- Built in 16k bits SRAM.
- Built in IEC-958 digital audio output circuit.
- Built in variable speed playback system.
- Built in L/R independent digital attenuator.
- Audio output responds to bilingual function.
- Read timing free subcode Q data and capable of synchronous output with audio data.
- Built in 8 times oversampling 1-bit DA converter.
- Built in analog filter for 1-bit DA converter.

### Digital Servo

- Capable of automatic adjustment of focus servo and tracking servo, for loop gain, offset and balance.
- Built in RF gain automatic adjustment circuit.
- Built in focus, tracking servo control DSP.
- Built in AFC circuit and APC circuit for CLV servo of disc motor.
- Built in anti-defect and anti-shock circuit.

### RAM Arbitrator

- Supports up to 16 Mb EDO DRAM and SDRAM.
- Supports 16 bits DRAM data width for ATA66 data bandwidth demands.
- Programmable DRAM page mode burst lengths for bandwidth optimization.
- Separate buffer address pointers and automated address calculation that save firmware effort.
- Read-ahead cache scheme supported for isochronous transfer required by multimedia.
- Protection logic preventing uncorrected sectors being released to the host.
- Direct subcode retrieval.

## Target Search

- Built in target sector searching circuit for auto-searching the target sector that is requested by host.
- Automatic data buffering after the target sector is searched.

## C3 ECC/EDC

- Programmable Reed-Solomon Product Code (RSPC) that allows different error correction schemes for CD-ROM.
- Built in On-chip EDC function.
- Supports up to 48X CD-ROM system with ECC correcting 'on the fly'.

## Host Interface

- Supports up to ATA PIO mode 4 timing that actually eliminates the assertion of IORDY even on ATA PIO mode 4 timing.
- Supports up to Multiword DMA mode 2 timing
- Supports up to Ultra DMA/33 mode 2 timing.
- Supports up to Ultra DMA/66 mode 2 timing.
- Compliant with SFF-8020(ATAPI) 2.5, ATA3 (Overlapping feature), and SFF-8090(ATAPI for DVD) standard
- High current drivers with slew rate control for direct connecting to the ATA bus and noise immunity
- Automatic Read Control Circuit to streamline the transfer required by host
  
- Automatic wake up from power down on host reset or command write
- Automatic sequence for packet command receiving and Automatic updating of the host task file registers
- Supports ATAPI write command that can let user download firmware from PC
- Built in authentication circuit for copy protection.
- Built in MPEG decoder interface for connecting with MPEG decoder when this chip is used in DVD-player.

## Microprocessor Interface

- Supports Intel 8032 series, Motorola MCUs, and the two stage (indexing) access method that fits most MCUs
- The polarity of chip select can be programmed to save customer's TTLs on the drive
- High speed register (buffer RAM) access to meet the requirement of high performance system
- Supports Direct mapped access to the buffer RAM using ready bit handshaking

## Process/Packaging

- 3.3V/5V CMOS process
- M5701 is packed in 208-pin PQFP