NIPPON PRECISION CIRCUITS LTD.

SM5807

4-Time Oversampling Digital Filter for CD System

■ GENERAL DESCRIPTION

The SM5807 digital filter is manufactured using MOLYGATE (モリゲート®) CMOS technology developed by NPC and is implemented in 4 times oversampling scheme with the stopband (above 24.1 kHz) attenuation of more than 50 dB and the passband ripple of less than +0.05 dB. Two channel filters are provided and the 4 times oversampled output signal of each channel can be independently obtained. Because of this 4 times oversampling, the requirement of the analog filter can be greatly relaxed, and also the serious data format reduces the size of hardware required in the system design. Two types, D and E are available in different characteristics.

■ FEATURES

- Filter Structure
  - 4 times oversampling
  - 2 channel filters
  - 2 stages linear phase FIR filter (61 + 13 taps)
  - Overflow limiter
  - Internal crystal oscillator circuit
  - Clock buffer
- Filter Characteristics

	SM5807DP,DS	SM5807EP,ES
Passband ripple(0~20kHz)	<±0.05dB	<±0.05dB
Stopband attenuation (above 24.1kHz)	>50dB	>45dB
Group delay time	Constant linear phase	

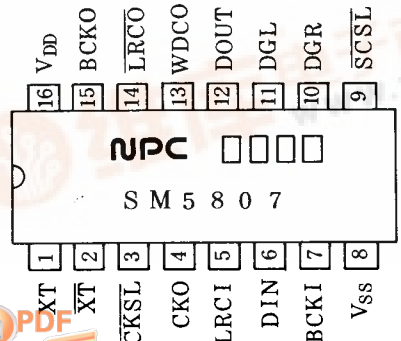
- Input/Output
  - 16-bit serial data input and output (2's complement, MSB first)
  - TTL compatible
- Power Supply 5±0.5V
- 16-Pin plastic DIP/SOP
- Molygate CMOS technology

■ PRODUCT SELECT LIST

Part Number	PACKAGE
SM5807DP, EP	16-Pin DIP
SM5807DS, ES	16-Pin SOP

■ PIN CONFIGURATION

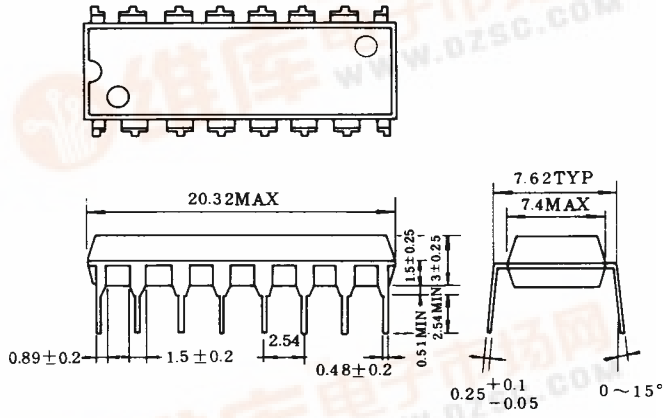
(Top View)



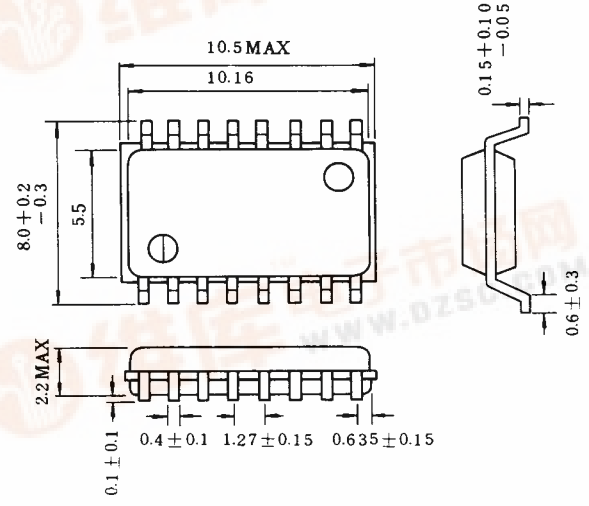
■ PACKAGE DIMENSIONS

All dimensions in millimeters

16-Pin DIP



16-Pin SOP



■ THEORETICAL FILTER CHARACTERISTICS

1. SM5807DP,DS (0~88.2kHz)

Parameter	Characteristic
Passband	0~20kHz
Stopband	Above 24.1 kHz
Passband Ripple	±0.05dB
Stopband Attenuation (above 24.1 kHz)	50dB(minimum)

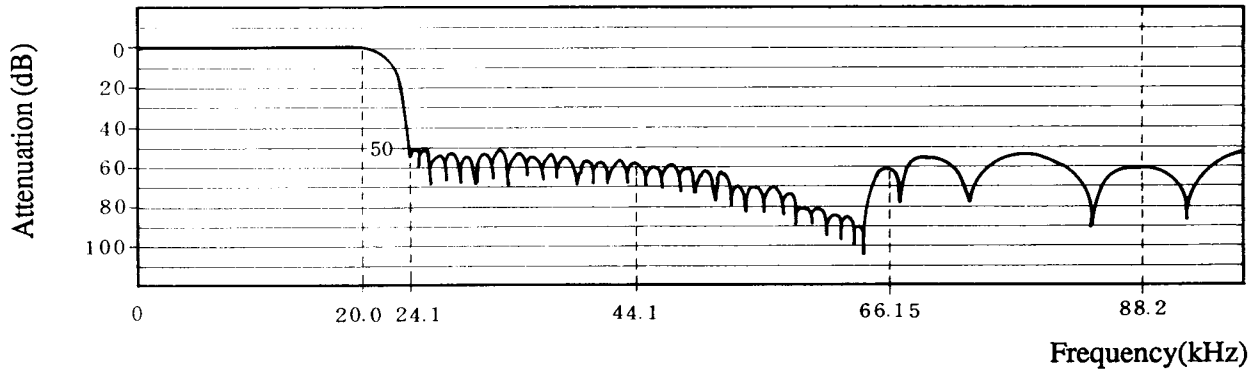


Figure 1 SM5807DP,DS Filter Transfer Characteristics

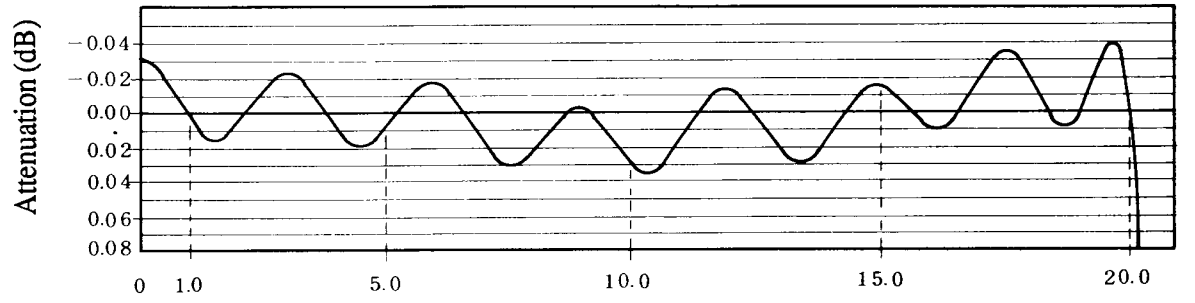


Figure 2 SM5807DP,DS Passband Frequency Response

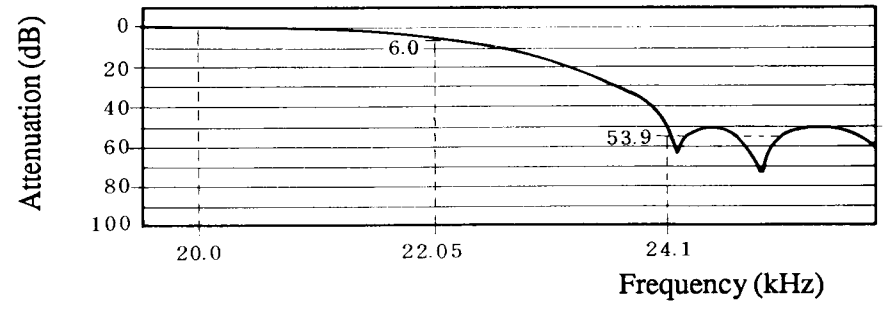


Figure 3 SM5807OP,DS Transitionband Frequency Response

2. SM5807EP, ES

(0~88.2kHz)

Parameter	Characteristics
Passband	0~20kHz
Stopband	Above 24.1kHz
Passband Ripple	±0.05dB
Stopband Attenuator	
(24.1~40.0kHz)	45dB (minimum)
(40.0kHz)	50dB (minimum)

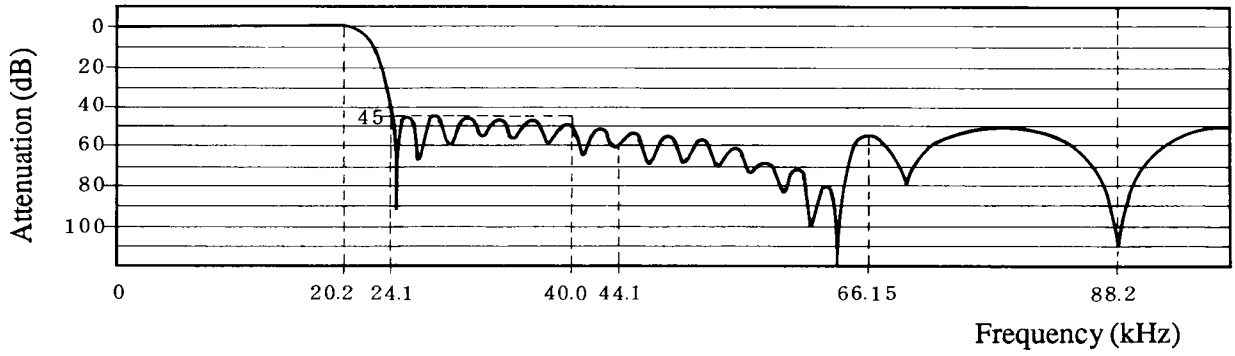


Figure 4 SM5807EP,ES Filter Transfer Characteristics

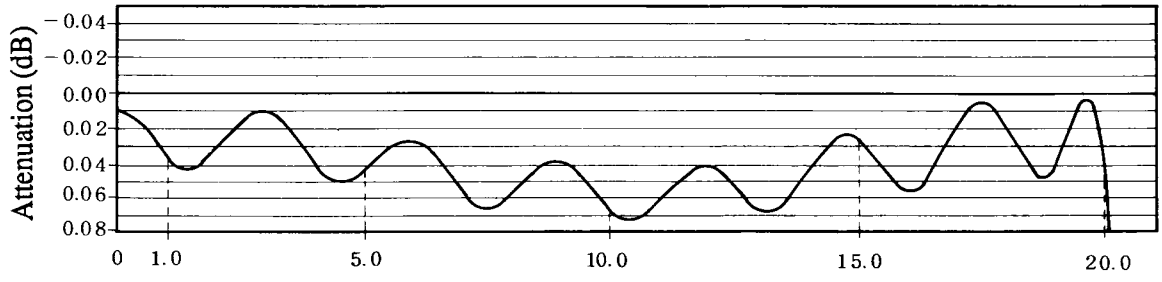


Figure 5 SM5807EP,ES Passband Frequency Response

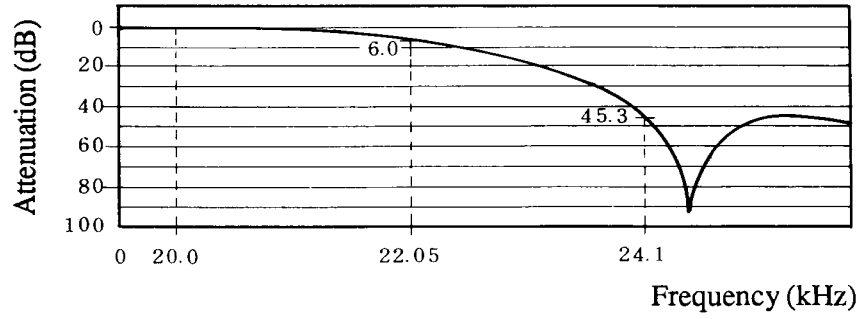
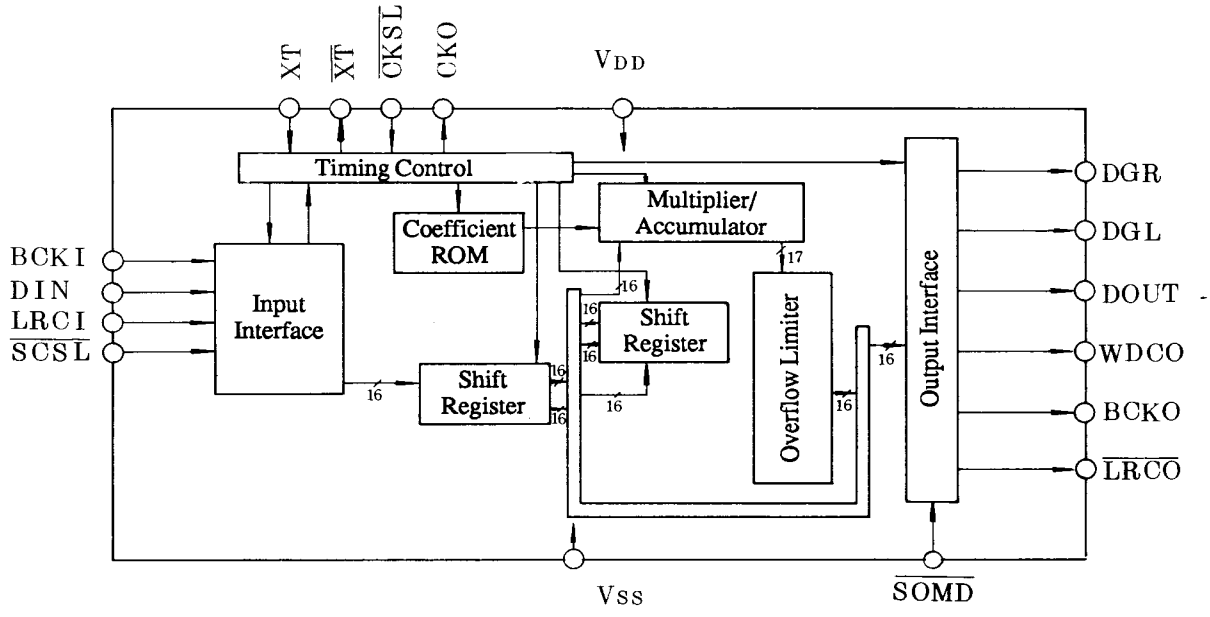


Figure 6 SM5807EP,ES Transitionband Frequency Response

■ BLOCK DIAGRAM



■ PIN DESCRIPTION

Pin No.	Pin Name	I/O	Function/Descriptions
1	XT	I	Crystal oscillator or clock input
2	$\overline{XT}$	o	Oscillator output when $\overline{CKSL}$=H Open, when CKSL=L
3	$\overline{CKSL}$	Ip	$\overline{CKSL}$=H : 16.9349 MHz ~ 17.2872MHz Crystal Osc.or Clock to XT pin CKSL=L : 8.4672MHZ or 8.6436 MHz Clock to XT pin
4	CKO	o	Clock output (XT clock buffered output)
5	LRCI	Ip	Clock input (synchronized 44.1 kHz)
6	DIN	Ip	Serial data input
7	BCKI		Bit clock input
8	V_{ss}	Ip	Ground, 0^V
9	$\overline{SCSL}$	Ip	$\overline{SCSL}$=H : System Clock = 192fs $\overline{SCSL}$=L : System Clock =196fs (fs:sampling frequency)
10	DGR	o	Rch deglitch signal (176.4 kHz)
11	DGL	o	Lch deglitch signal (176.4 kHz)
12	DOUT	o	Serial data output
13	WDCO	o	Output Control Clock (352.8 kHz)
14	$\overline{LRCO}$	o	Output Control Clock (176.4 kHz)
15	BCKO	o	Serial Output Bit Clock (8.4672 MHz or 8.6436 MHz)
16	V_{DD}		Power Supply (5V)

I : Input
o : Output
Ip: Input with pull-up resistor

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Rating	Units
Supply Voltage	V_{DD}	-0.3~7.0	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Storage Temperature	T_{STG}	-40~125	°C
Power Dissipation	P_W	250	mW
Soldering Temperature	T_{SLD}	255	°C
Soldering Time	t_{SLD}	10	Sec.

■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Conditions	Unit
Supply Voltage	V_{DD}	4.5~5.5	V
Operating Temperature	T_{OPR}	-20~70	°C

■ DC ELECTRICAL CHARACTERISTICS

Ta=-20~70°C, V_{DD}=4.5~5.5V, V_{SS}=0V unless otherwise noted

Parameter	Pin	Symbol	Condition	Limit			Unit
				MIN	TYP	MAX	
Supply Current	V_{DD}	I_{DD}	V_{DD}=5V		10	20	mA
Input Voltage (1)	XT	V_{IH1}		0.7V_{DD}			V
		V_{IL1}				0.3V_{DD}	V
Input Voltage (2)	(*1)	V_{IH2}		2.4			V
		V_{IL2}				0.5	V
Output Volage	(*2)	V_{OH}	I_{OH}=-0.4mA	2.5			V
		V_{OL}	I_{OL}=1.6mA			0.4	V
Input Leakage Current	(*3)	I_{LL}	V_{IN}=0V			1.0	μA
	(*4)	I_{LH}	V_{IN}=V_{DD}			1.0	μA
Input Current	(*1)	I_{IL}	V_{IN}=0V		10	20	μA

Pin-Group List

*1	$\overline{CKSL}$, LRCI, DIN, BCKI, $\overline{SCSL}$
*2	CKO, $\overline{LRCO}$, BCKO, WDCO, DOUT, DGL, DGR
*3	(XT, at $\overline{CKSL}$=L)
*4	$\overline{CKSL}$,, LRCI, DIN, BCKI, $\overline{SCSL}$, (XT, at $\overline{CKSL}$=L)

■ AC ELECTRICAL CHARACTERISTICS

1.XT

a. Crystal Oscillator (Ta=-20~70°C, VDD=4.5~5.5V, V_{SS}=0V)

Parameter	Symbol	Limit			Unit
		MIN	TYP	MAX	
Frequency	fosc			20	MHz

b.External Clock

(Ta=-20~70°C, V_{DD}=4.5~5.5V, V_{SS}=OV)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
Clock Pulse Width	tcw	50			nSec	$\overline{CKSL}$=L
		25			nSec	$\overline{CKSL}$=H
Clock Pulse Period	tcy	100			nSec	$\overline{CKSL}$=L
		50			nSec	$\overline{CKSL}$=H

XT

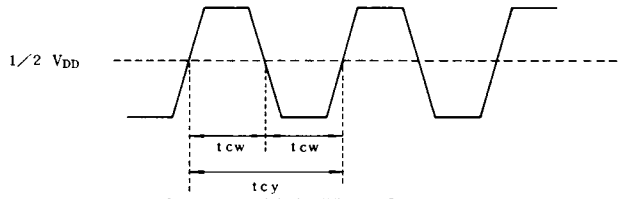


Figure 7 XT Waveform

2. Serial Input Timing (DIN, BCKI, LRCI)

(Ta=-20~70°C, V_{DD}=4.5~5.5V, V_{SS}=OV)

Parameter	Symbol	Limit			Unit
		MIN	TYPE	MAX	
BCKI Pulse Width	t_{BCW}	100			nsec
BCKI Pulse Period	t_{BCY}	200			nsec
DIN, LRCZ set-up time	t_S	75			nsec
DIN, LRCZ holding time	t_H	75			nsec

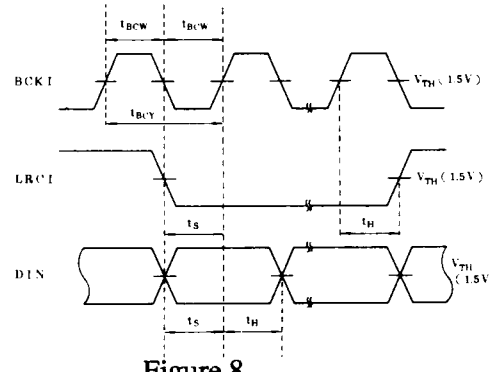


Figure 8
Input Timing Waveform

3.Serial Output Timing

(Ta=-20~70°C, V_{DD}=4.5V, V_{SS}=OV)

Parameter	Symbol	Limit			Unit	Remarks
		MIN	TYP	MAX		
BCKO Pulse Width	t_{OBCW}	40			nSec	
BCKO Pulse Period	t_{OBCY}	100			nSec	
Output Delay Time	t_{DHL}	0		25	nSec	$\overline{LRCO}$, WDCO, DOUT, DGL, DGR outputs
	t_{DLH}			25	nSec	

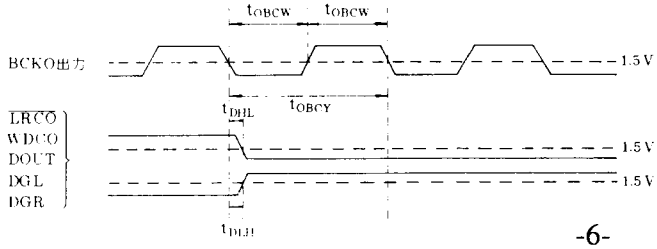


Figure 9 Output Timing Waveform

■ INTRODUCTION

Basic Filter Structure
The SM5807 consists of two channel filters implemented in two times oversampling two stages cascaded linear phase FIR filter as shown in Fig 10. The 44.1KHz sampled signal.is two times oversampled in the 61-tap first filter stage and is converted to a 88.2KHz sample signal. It is further two times oversampled in the 13-tap second filter stage and becomes 176.4KHz sampled signal which is 4 times oversampled as compared with that at the input. Fig.11 illustrates sampled signal spectrum of the output of channel filter (see Fig.10). Fig.11(a) shows the output spectra of the first filter which provides -50dB or -45dB attenuation at and above 24.1KHz. However, the input signal spectrum of ±24.1KHz centered on 88.2KHz sampling frequency still exists. The second filter which further doubles the sampling frequency for filtering the output of the first filter provides -50dB or -45dB for the signal band between 64.1KHz and 112.3KHz as shown in Fig.11(b). The combined filter characteristics are illustrated in Fig.11(c).The SM5807 was designed based on this oversampling technique and their filter characteristics are illustrated in page 2 through 3.

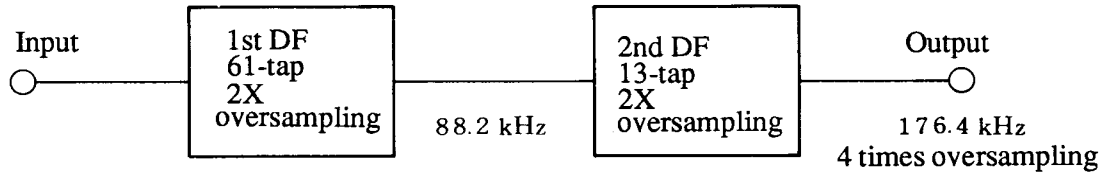


Figure 10 Block Diagram of the Channel Filter.

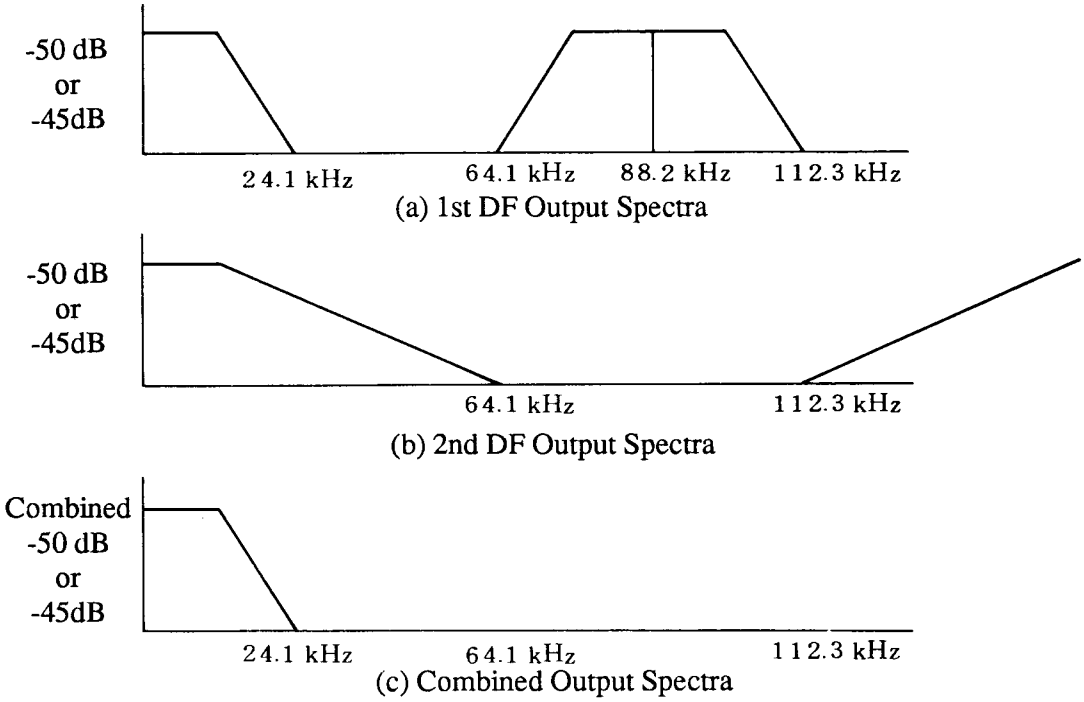


Figure 11 Signal Spectra

■ FUNCTIONAL DESCRIPTION

1.System Clock

The system clock frequency, 8.4672 MHz (=192fs) or 8.6436MHz(=196fs) is selected by $\overline{SCSL}$ logic level. $\overline{SCSL}$=H (or open), fsc=192fs where fs=44.1kHz
$\overline{SCSL}$=L, fsc=196fs where fs=44.1kHz

Clock Generation

$\overline{SCSL}$	H (or open)		L	
$\overline{CKSL}$	H (or open)	L	H	L
Clock Source	Crystal oscillator or external clock	Crystal Oscillator or System Clock	Crystal Oscillator or External Clock	Crystal Oscillator or External Clock
XT/XT Input Frequency	384fs=16.9344MHz	192fs=8.4672MHz	392fs=17.2872MHz	196fs=8.6436MHz
CKO Clock Output	384fs=16.9344MHz	192fs=8.4672MHz	392fs=17.2872MHz	196fs=8.6436MHz
System Clock (Internal)	192fs=8.4672MHz	192fs=8.4672MHz	196fs=8.6436MHz	196fs=8.6436MHz

2. Serial Input (data and bit clock)

The serial input data is entered at at the rising edge of serial input bit clock, BCKI. The data can be changed at the falling edge of BCKI. After the 16 bits data have been entered, they are latched in the internal register by the LRCI clock.

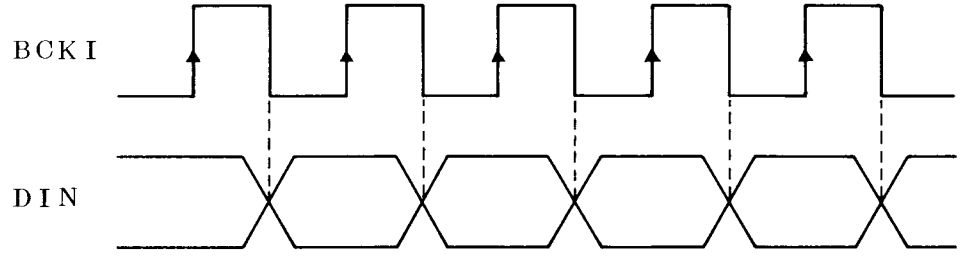


Figure 12 DCKI and DIN Waveforms

3. Input Data Format

The format is 2's complement, MSB first.

4. Starting of Data Process

The data process starts at the rising edge of LRCI clock.

5. Serial Output (data and bit clock)

The Lch and Rch serial data are delivered to pin DOUT alternately and therefore using one DAC for conversion is implementable. For using two DAC's, additional gates are required (see Fig.15,b). The serial output bit clock is available at pin BCKO.

BCKO=8.4672MHz ($\overline{SCSL}$=H or open system clock: 192fs)
BCKO=8.6436MHz ($\overline{SCSL}$=L system clock: 196fs)

6.Output Data Format

The format is 2's complement, MSB first.

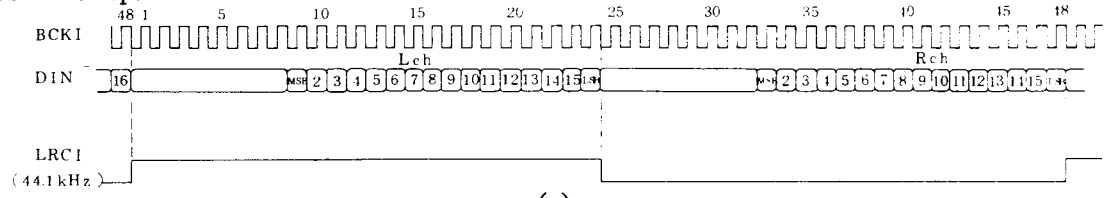
7. Deglitch Signals

The 176.4kHz, 25% duty cycle deglitch signals are available at pins DGL and DGR for Lch and Rch respectively.

■ TIMING DIAGRAMS

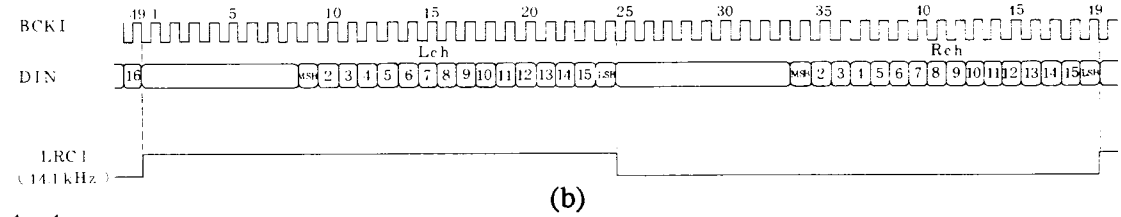
• Input

(1) $\overline{\text{SCSL}}$=H or Open



(a)

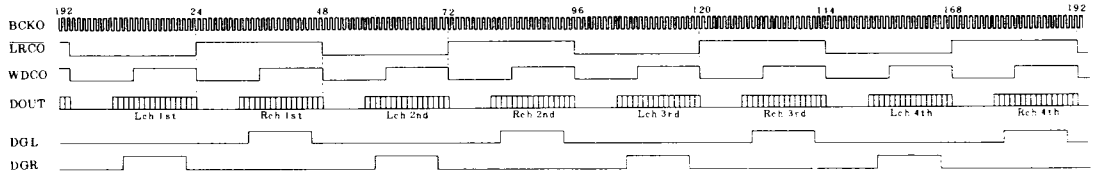
(2) $\overline{\text{SCSL}}$=L



(b)

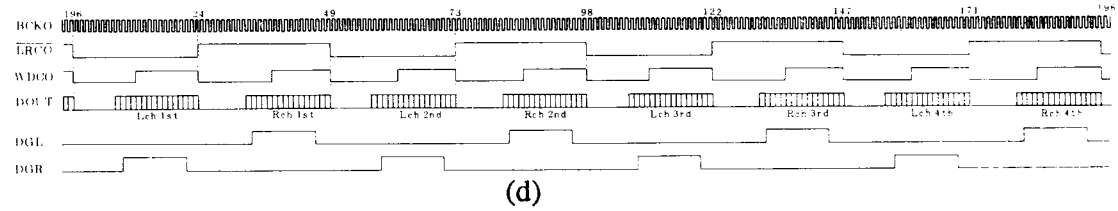
• Output

(1) SCSL=H or Open



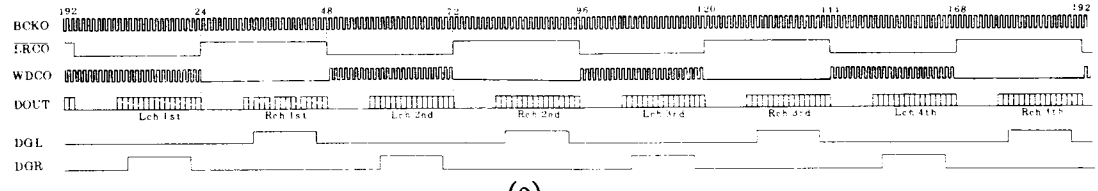
(c)

(2) SCSL=L



(d)

(3) $\overline{\text{SOMD}}$=L

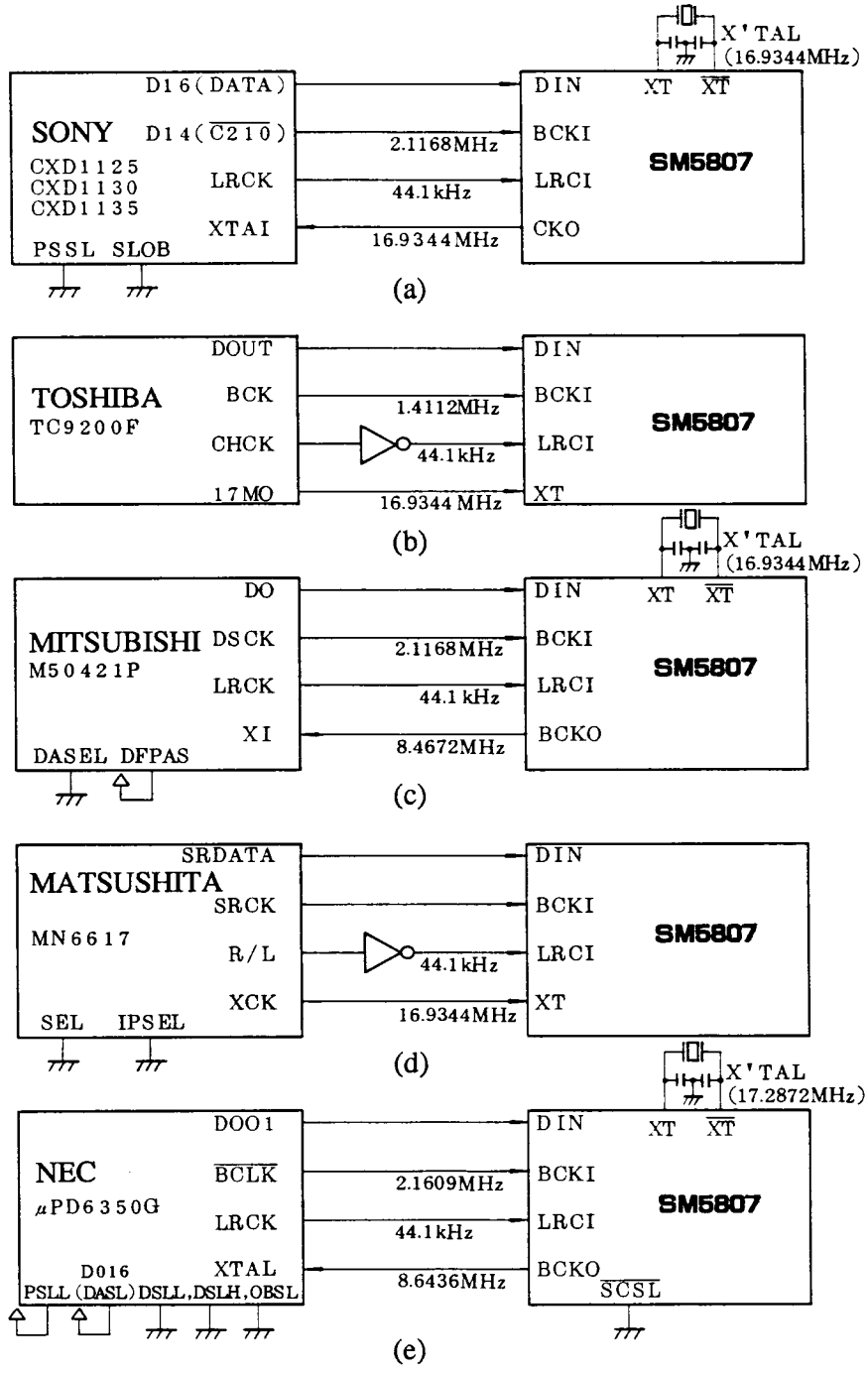


(e)

Figure 13 Serial Input and Output Timing Diagrams

■ APPLICATION DIAGRAMS

1. Input Connection

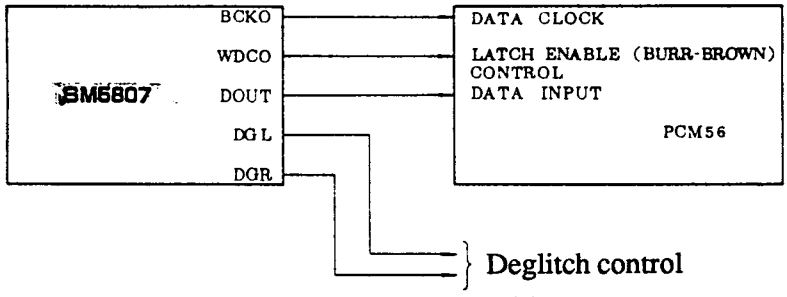


⊠14.1 ⊠14.2 ⊠14.3 ⊠14.4 ⊠14.5

Figure 14 Application Circuits - Input Connection

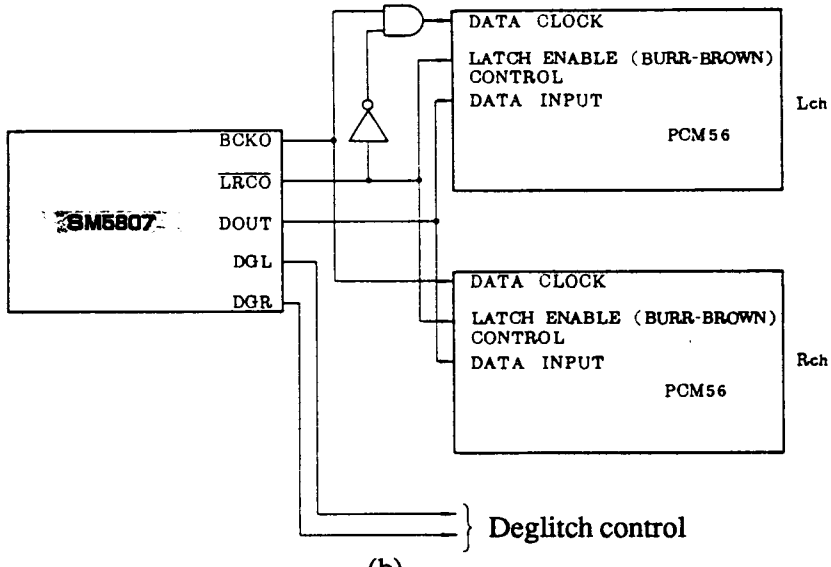
2. Output Connection

a.1DAC

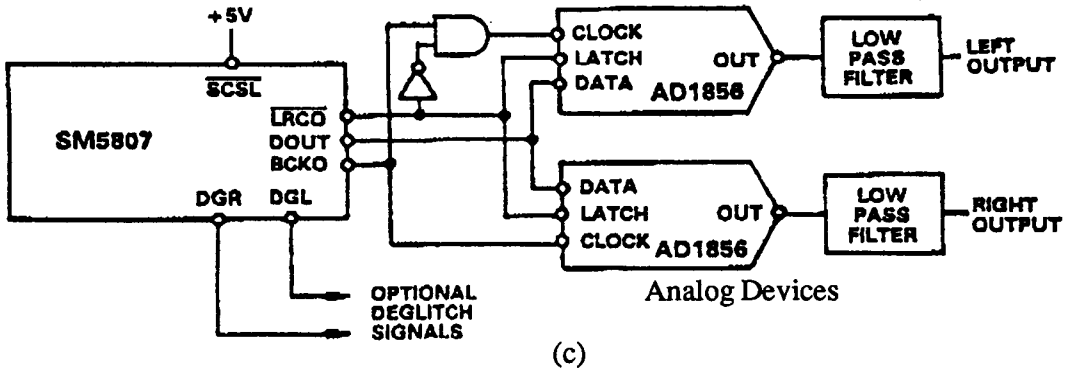


(a)

b. 2 DAC's



(b)



(c)

Figure 15 Application Circuit - Output connections