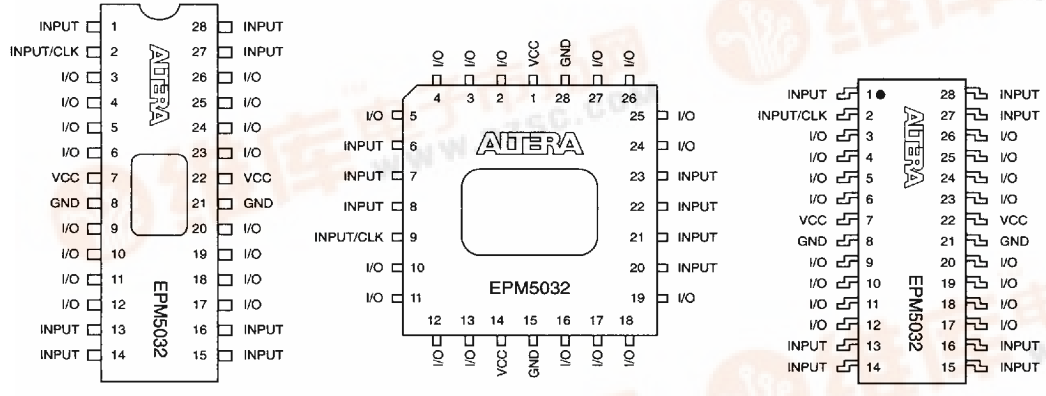
Features

- High-speed, single-LAB MAX 5000 EPLD
  - t_{PD} as fast as 10 ns
  - Counter frequencies up to 125 MHz
  - Pipelined data rates up to 83 MHz
- 32 individually configurable macrocells
- 64 shareable expander product terms ("expanders") allowing 68 product terms on a single macrocell
- Programmable I/O architecture allowing up to 24 inputs or 16 outputs
- Available in 28-pin windowed ceramic and plastic one-time-programmable (OTP) packages (see Figure 8):
  - Dual in-line (CerDIP and PDIP)
  - J-lead chip carrier (JLCC and PLCC)
  - Small-outline integrated circuit (plastic SOIC only)
- Military devices available. For information, refer to the *Military Products Data Sheet* in this data book.

Figure 8. EPM5032 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



28-Pin DIP | 28-Pin J-Lead | 28-Pin SOIC

General Description

Altera EPM5032 EPLDs are MAX 5000 EPLDs optimized for speed. They can integrate multiple SSI, MSI TTL, or SSI and MSI TTL as well as CMOS logic devices. In addition, the EPM5032 can replace multiple 20-pin PAL or PLA devices and have logic left over for further integration. EPM5032 EPLDs contain 32 macrocells; the expander product-term array provides 64 expanders. The I/O control block contains 16 bidirectional I/O pins that can be configured for dedicated input, dedicated output, or bidirectional operation. All I/O pins feature dual feedback for maximum pin flexibility. See Figure 9.

Figure 9. EPM5032 Block Diagram

Numbers without parentheses are for DIP and SOIC packages. Numbers in parentheses are for J-lead packages.

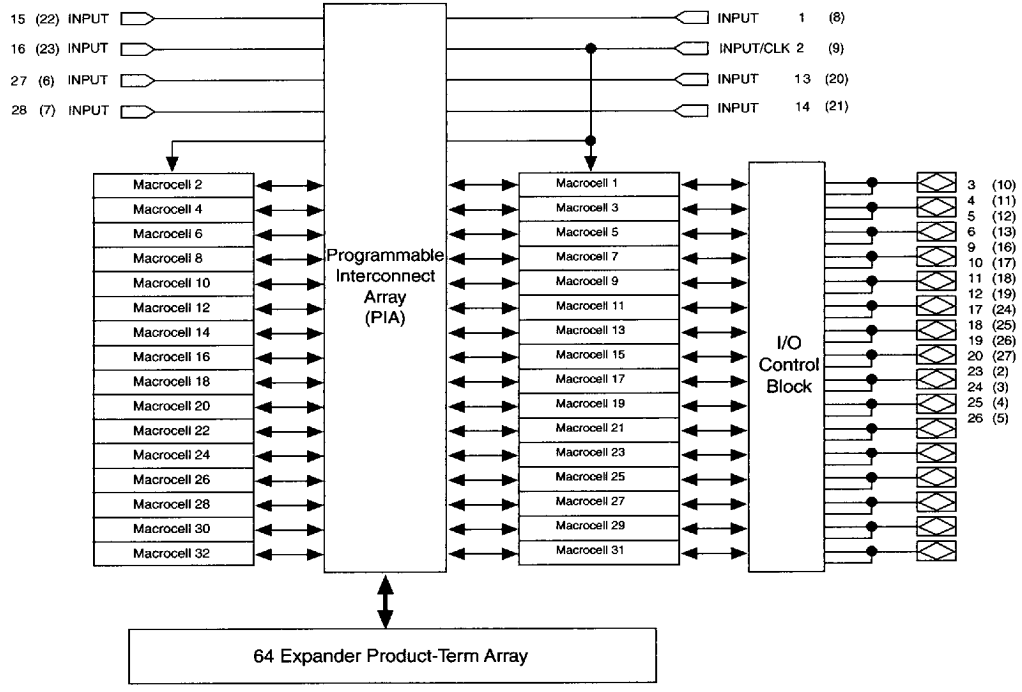
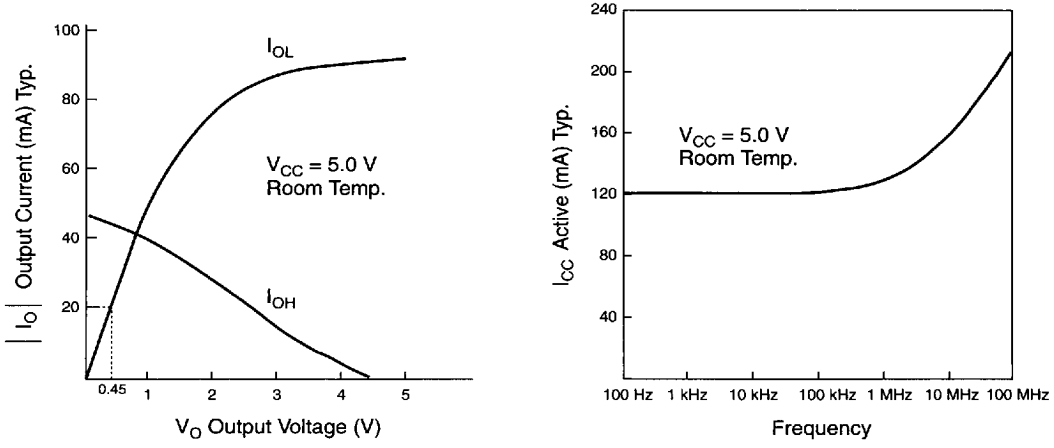


Figure 10 shows the output drive characteristics of EPM5032 I/O pins and typical supply current (I_{CC}) versus frequency.

Figure 10. Typical Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias, *Note (2)*	–65 [–55]	150 [125]	° C
T_J	Junction temperature	Under bias, *Note (2)*		150 [175]	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Notes (3), (4)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0 [2.2]		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Notes (3), (7)*		120	150 (200)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, no load, f = 1.0 MHz, *Notes (3), (7)*		125	155 (225)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (6)*

External Timing Parameters			EPM5032A-10		EPM5032A-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		10		12	ns
t_{PD2}	I/O input to non-registered output			10		12	ns
t_{SU}	Global clock setup time		7		8		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		6		7	ns
t_{CH}	Global clock high time		4		4.5		ns
t_{CL}	Global clock low time		4		4.5		ns
t_{ASU}	Array clock setup time		3		3		ns
t_{AH}	Array clock hold time		4		4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		10		12	ns
t_{ACH}	Array clock high time		4		4.5		ns
t_{ACL}	Array clock low time		4		4.5		ns
t_{CNT}	Minimum global clock period			8		9	ns
f_{CNT}	Max. internal global clock frequency	*Note (7)*	125		111.1		MHz
t_{ACNT}	Minimum array clock period			8		9	ns
f_{ACNT}	Max. internal array clock frequency	*Note (7)*	125		111.1		MHz
f_{MAX}	Maximum clock frequency	*Note (9)*	125		111.1		MHz

Internal Timing Parameters *Note (10)*			EPM5032A-10		EPM5032A-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2.5		2.5	ns
t_{IO}	I/O input pad and buffer delay			2.5		2.5	ns
t_{SEXP}	Expander array delay			6		8	ns
t_{LAD}	Logic array delay			4		5	ns
t_{LAC}	Logic control array delay			4		4	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		4	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		7		7	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7		7	ns
t_{SU}	Register setup time		3		3		ns
t_{LATCH}	Flow-through latch delay			1		1	ns
t_{RD}	Register delay			0.5		0.5	ns
t_{COMB}	Combinatorial delay			0.5		0.5	ns
t_{H}	Register hold time		4		4		ns
t_{IC}	Array clock delay			4		5	ns
t_{ICS}	Global clock delay			0		0	ns
t_{FD}	Feedback delay			0.5		0.5	ns
t_{PRE}	Register preset time			5		5	ns
t_{CLR}	Register clear time			5		5	ns

AC Operating Conditions *Note (6)*

External Timing Parameters			EPM5032-15		EPM5032-17		EPM5032-20		EPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		17		20		25	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		15		17		20		25	ns
t_{SU}	Global clock setup time		9		10		12		15		ns
t_{H}	Global clock hold time		0		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		10		10		12		15	ns
t_{CH}	Global clock high time		6		6		7		8		ns
t_{CL}	Global clock low time		6		6		7		8		ns
t_{ASU}	Array clock setup time		5		5		6		8		ns
t_{AH}	Array clock hold time		5		5		6		8		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		15		18		22	ns
t_{ACH}	Array clock high time	*Note (8)*	6		6		7		9		ns
t_{ACL}	Array clock low time		7		8		9		11		ns
t_{CNT}	Minimum global clock period			13		14		16		20	ns
f_{CNT}	Max. internal global clock frequency	*Note (7)*	76.9		71.4		62.5		50		MHz
t_{ACNT}	Minimum array clock period			13		14		16		20	ns
f_{ACNT}	Max. internal array clock frequency	*Note (7)*	76.9		71.4		62.5		50		MHz
f_{MAX}	Maximum clock frequency	*Note (9)*	83.3		83.3		71.4		62.5		MHz

Internal Timing Parameters *Note (10)*			EPM5032-15		EPM5032-17		EPM5032-20		EPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		3		5		7	ns
t_{IO}	I/O input pad and buffer delay			3		3		5		7	ns
t_{SEXP}	Expander array delay			8		8		10		15	ns
t_{LAD}	Logic array delay			7		9		10		13	ns
t_{LAC}	Logic control array delay			4		4		4		4	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4		4		4		4	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		7		7		7		7	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7		7		7		7	ns
t_{SU}	Register setup time		4		3		4		5		ns
t_{LATCH}	Flow-through latch delay			1		1		1		1	ns
t_{RD}	Register delay			1		1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1		1	ns
t_{H}	Register hold time		5		7		8		10		ns
t_{IC}	Array clock delay			7		7		8		10	ns
t_{ICS}	Global clock delay			2		2		2		3	ns
t_{FD}	Feedback delay			1		1		1		1	ns
t_{PRE}	Register preset time			5		5		6		9	ns
t_{CLR}	Register clear time			5		5		6		9	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in brackets are for MIL-STD-883-compliant versions only.
(3) Numbers in parentheses are for military- and industrial-temperature-range versions, as well as for MIL-STD-883-compliant versions.
(4) Maximum V_{CC} rise time for the EPM5032 is 10 ms. Maximum V_{CC} rise time for the EPM5032A is 200 ms.
(5) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(6) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(7) This parameter is measured with a device programmed as a 32-bit counter. I_{CC} measured at 0° C.
(8) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(9) The f_{MAX} values represent the highest frequency for pipelined data.
(10) For information on internal timing parameters, refer to *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* in this data book.