Order this document by MC44353/D

MOTOROLA

Advance Information

PLL Tuned UHF Audio/Video Modulator ICs for PAL, SECAM and NTSC TV Systems

MC44353 – Multi–Standard Modulator IC
MC44354 – PAL/NTSC Modulator IC
MC44355 – PAL/NTSC Modulator IC with Fixed Video Modulation Index

These modulator circuits are intended for use in VCRs, satellite receivers, set–top boxes, video games, etc. An on–chip high speed I^2C compatible bus receiver is included and is used to set the channel, tuned by a PLL over the full range in the UHF bands. The modulator incorporates a sound subcarrier oscillator, using a second PLL to derive 4.5, 5.5, 6.0 and 6.5 MHz carrier frequencies, selectable by the bus.

For the sound, either frequency modulation with pre–emphasis or amplitude modulation (MC44353 only) is possible. A control bit (MC44353 only) is used to select AM sound with positive RF modulation (system L). The level of the sound carrier with respect to the vision carrier and the modulation depth of both sound and vision may be adjusted by means of the bus. In addition, an on–chip video test pattern generator may be switched in with a 1.0 kHz audio test signal.

- Channel 21 through 69 UHF Operation (471 MHz to 855 MHz)
- On–Chip Low Power Operational Amplifier for Direct Tuning Varactor Voltage
- Single–Ended Output for Low Cost and Ease of Interface
- Low External Component Count
- High Speed I^2C Bus Compatible
- Programmable Video Modulation Depth (8 Steps of 2.5%)
- Programmable Picture/Sound Carriers Ratio and Audio Sensitivity (8 Steps of 1.0 dB)
- On–Chip Programmable Sound Subcarrier Oscillator (4.5 MHz to 6.5 MHz)
- On–Chip Video Test Pattern Generator with Sound Test Signal (1.0 kHz)
- V_{CC} Standby Mode (Typ 500 µA)
- Transient Output Inhibit During PLL Lock–Up at Power–On

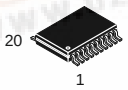
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44353DTB	T_A = –20° to +80°C	TSSOP–20
MC44353DW		SO–20L
MC44354DTB		TSSOP–20
MC44354DW		SO–20L
MC44355DTB		TSSOP–20
MC44355DW		SO–20L

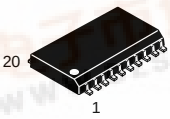
MC44353
MC44354
MC44355

MULTI–STANDARD AND PAL/NTSC MODULATOR ICs

SEMICONDUCTOR TECHNICAL DATA

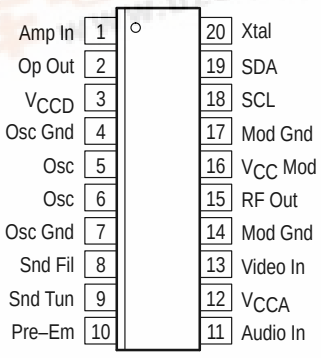


DTB SUFFIX
PLASTIC PACKAGE
CASE 948E
(TSSOP–20)



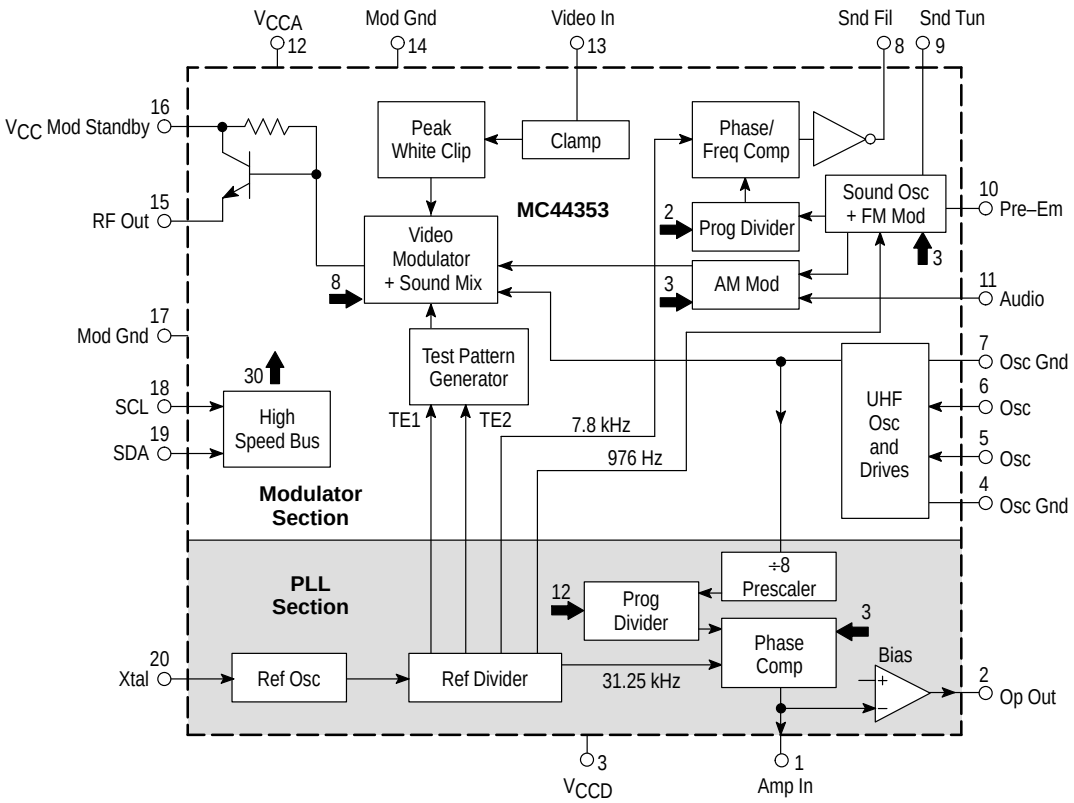
DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

PIN CONNECTIONS



(Top View)

Figure 1. MC44353 Simplified Block Diagram



MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7	V
Operational Amplifier Output Voltage		36	V
Operating Ambient Temperature	T_A	–20 to 80	°C
Storage Temperature	T_{stg}	–65 to 150	°C

NOTES: 1. Maximum ratings are those values beyond which damage to the device may occur. For functional operation, voltages should be restricted to the Recommended Operating Conditions.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (Parameter Type: A–100% Tested, B–100% Correlation Tested, C–Characterized on Samples. D–Design Parameter, VCC = 5.0 V, TA = 25C, Video input 1.0 Vpp, 10 step greyscale. Step 3 [typ. 80%] modulation depth for PAL; Step 5 [typ 90%] modulation for SECAM L; P/S ration Step 3 [typ 14.5 dB]. RF output into 75 Ω load. Unless otherwise noted.) (Specifications only valid for envelope demodulation.)

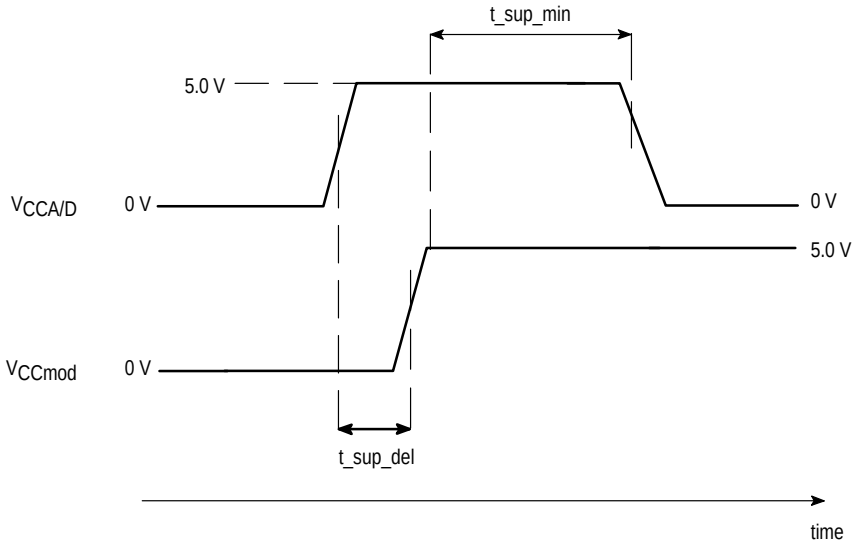
Characteristic	Symbol	Min	Typ	Max	Unit	Type
Operating Supply Voltage Range	V_{CCA},V_{CCD}, V_{CC} Mod	4.5	5.0	5.5	V	D
Analog Section Supply Current (V_{CC} = 5.0 V)	I_{CCA}	26	33	39.5	mA	A
Digital Section Supply Current (V_{CC} = 5.0 V)	I_{CCD}	24	32	39	mA	A
Modulator O/P Section Supply Current (V_{CC} = 5.0 V)	I_{CC} Mod	6.0	9.0	11.5	mA	A
Total Supply Current (V_{CC} = 5.0 V)	I_{CC}	56	74	90	mA	A
During Standby	V_{CC} Mod	4.0	–	5.5	V	D
During Standby (with Data Retension: V_{CC} Mod = 5.0V)	I_{CC} Mod	–	0.5	1.0	mA	B
Operational Amplifier Output Voltage (through R_{pullup})		–	30	35	V	B
Operational Amplifier Output Current (with Rpullup = 560 kΩ		–	56	100	μA	B
Test Pattern Sync Pulse Width	T_{E1}	4.0	4.7	5.6	μs	A

ELECTRICAL CHARACTERISTICS (continued) (Parameter Type: A–100% Tested, B–100% Correlation Tested, C–Characterized on Samples. D–Design Parameter, VCC = 5.0 V, TA = 25C, Video input 1.0 Vpp, 10 step greyscale. Step 3 [typ. 80%] modulation depth for PAL; Step 5 [typ 90%] modulation for SECAM L; P/S ration Step 3 [typ 14.5 dB]. RF output into 75 Ω load. Unless otherwise noted.) (Specifications only valid for envelope demodulation.)

Characteristic	Symbol	Min	Typ	Max	Unit	Type
UHF Comparator Pump Current (Note 1)		2.0	4.0	6.0	μA	A
Sound Comparator Pump Current (Note 2)		2.0	3.8	5.6	μA	A
Op–Amp Input Current		–	–	20	nA	A
Oscillator Stability – negative resistance		1.0	–	–	kΩ	D
Delay $V_{CCA/D}$ to V_{CC} Mod Application (See Figure 2)	t_sup_del	0	–	–	ns	D
$V_{CCA/D}$ & V_{CC} Mod Duration for Standby Mode Function (See Figure 2)	t_sup_min	30	–	–	ms	D

NOTES: 1. Current sources driven by the UHF phase comparactor, that are connected to Pin 1.
2. Current sources driven by the phase sound comparator, that are connected to Pin 8.

Figure 2. Initial Power–On and Standby Mode V_{CC} Timing Diagram



For proper operation of internal reset functions, V_{CCA} and V_{CCD} (which must be applied simultaneously) may not be applied after V_{CCmod}.

Normally, all V_{CC} lines will come up at the same time. However, due to the possibility of a Standby V_{CC} to be applied to the V_{CCmod} pin, care should be ensured that V_{CCmod} is not applied before V_{CCA} and V_{CCD} (which must be tied together). See the timing diagram and DATA RETENTION function description.

Note that $V_{CCA/D}$ and V_{CCmod} must be activated above 4.5 V for a least 30 msecs before the device can operate correctly in Standby Mode.

HIGH SPEED I²C COMPATIBLE BUS CHARACTERISTICS (Over Functional Temperature Range – V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit	Type
SDA/SCL Output Current at 0 V		–	–	10	μA	A
SDA/SCL Low Input Level	V_{il}	–	–	1.5	V	B
SDA/SCL High Input Level	V_{ih}	3.0	–	–	V	B
SDA/SCL Input Current for Input Level from 0.4 V to 0.3 V_{CC}		–5.0	–	5.0	μA	C
SDA/SCL Input Level		0	–	V_{CC} + 0.3	V	D
SDA/SCL Capacitance	C_i	–	–	10	pF	C
ACK Low Output Level (sinking 3.0 mA)		–	0.3	1.0	V	A
ACK Low Output Level (sinking 15 mA)		–	–	1.5	V	C

HIGH SPEED I²C COMPATIBLE BUS CHARACTERISTICS (continued) (Over Functional Temperature Range – V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit	Type
Bus Clock Frequency		0	–	800	kHz	C
Bus Free Time Between Stop and Start	T_{buf}	200	–	–	ns	C
Setup Time for Start Conditions	$T_{su;sta}$	500	–	–	ns	C
Hold Time for Start Condition	$T_{hd;sta}$	500	–	–	ns	C
Data Setup Time	$T_{su;dat}$	0	–	–	ns	C
Data Hold Time	$T_{hd;dat}$	0	–	–	ns	C
Setup Time for Stop Condition	$T_{su;sto}$	500	–	–	ns	C
Hold time for Stop Condition	$T_{hd;sto}$	500	–	–	ns	C
Acknowledge Propagation Delay	$T_{ack;low}$	–	–	300	ns	C
SDA Fall Time at 3.0 mA sink and 130 pF Load		–	–	50	ns	C
SDA Fall Time at 3.0 mA sink and 400 pF Load		–	–	80	ns	C
SDA/SCL Rise Time		–	–	300	ns	C
SCL Fall Time		–	–	300	ns	C
Pulse Width of Spikes Suppressed by the Input Filter	T_{sp}	–	–	50	ns	C

Figure 3. Timings Definition

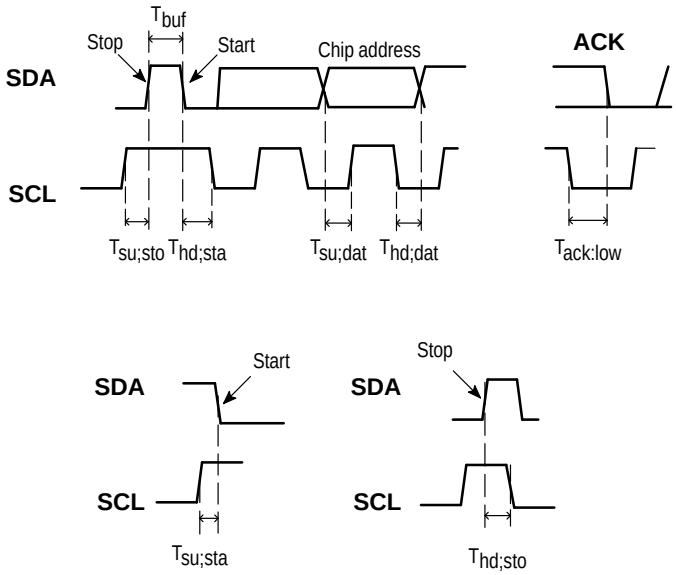
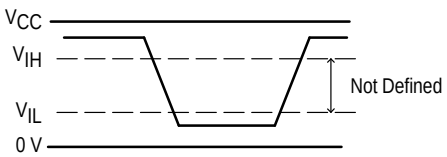


Figure 4. Levels Definition

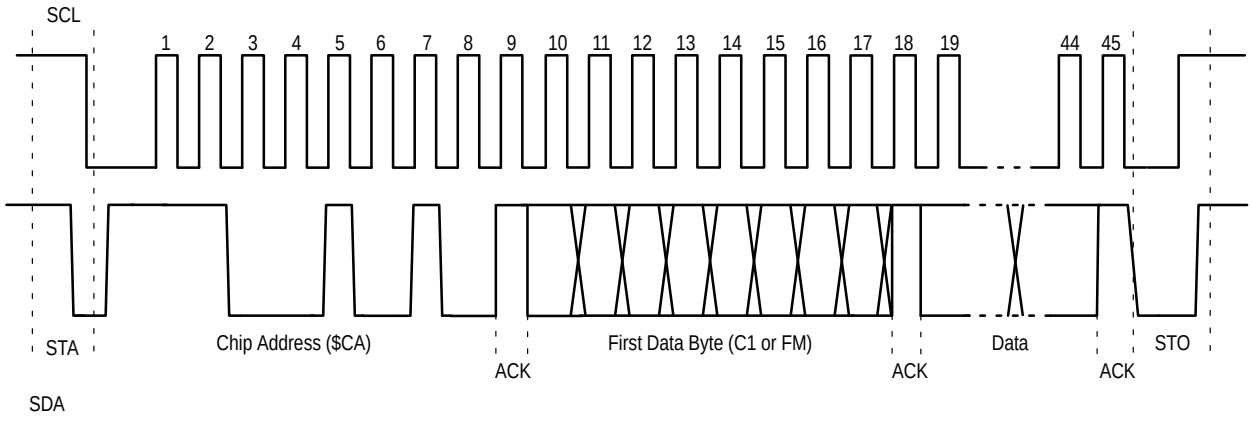


High Speed I²C Compatible Bus Format

	Bit 7							Bit 0	ACK
CA – Chip Address	1	1	0	0	1	0	1	0	ACK
C0 – Low Order Bits	VMD2	VMD1	VMD0	SFD1	SFD0	TB2	TB1	TB0	ACK
C1 – High Order Bits	1	AMD2	AMD1	AMD0	PSD2	PSD1	PSD0	SysL	ACK
FL – Low Order Bits	N_5	N_4	N_3	N_2	N_1	N_0	X_1	X_0	ACK
FM – High Order Bits	0	TPEN	N_{11}	N_{10}	N_9	N_8	N_7	N_6	ACK

NOTES: 1. C0 and FL: Low Order Bits and C1 and FM: High Order Bits.
2. VDM0–2: Video Mod Depth control bits (for MC44355 VMD0–2 are Don't Care).
3. SFD0–1: Sound subcarrier frequency control bits.
4. TB0–2 and X_1, X_0: Test modes bits, see table entitled TEST MODES.
5. AMD0–2: Audio Modulation Sensitivity, see table entitled AUDIO MODULATION SENSITIVITY (for MC44355 AMD0–2 are Don't Care).
6. PSD0–2: Picture to Sound carrier ratio, see table entitled PICTURE to SOUND CARRIER RATIO (for MC44355 PSD0–1 are Don't Care).
7. SysL: System L enable (selects AM sound and positive video modulation, MC44353 only).
8. TPEN: Test pattern enable (picture and sound).
9. N_0 to N_{11}: UHF frequency programming bits, in steps of 250 kHz.

Figure 5. High Speed I²C Compatible bus data format



VIDEO CHARACTERISTICS

Characteristic	Test Conditions	Min	Typ	Max	Unit	Type
Video Bandwidth	(0/–1.0 dB; ref 0 dB @ 100 kHz)	5	-	–	MHz	C
Video Input Level		–	–	1.5	V_{CVBS}	D
Video Input Current		–	50	200	nA	A
Peak White Clip (Note 1)		108	112	116	%	B
Video Input Impedance	Measured at 1.0 kHz (at Pin 13)	–	500/4	–	kΩ/pF	D
Video S/N	See Note 2	–	Figure 6	Figure 6	dB	C
Differential Phase		Figure 7	Figure 7	Figure 7	°	C
Differentical Gain	On line CCIR 310, worst from the first 4 steps out of 5	–	1.0	5	%	C
Luma/Sync ratio	Input ratio 7.0:3.0	6.8/3.2	–	7.2/2.8		B
PAL Video Modulation Depth Step 3	Programmable in 8 steps of 2.5%	76	82	88	%	B
SECAM Video Modulation Depth Step 5 (MC44353 Only)		84.5	90.5	96.5	%	B

NOTES: 1. The circuit is equipped with a 'soft clip' function. The Video Modulation depth is measured for a 1.0 V_{CVBS} input level, giving modulation depth MDA; then the same measurement is carried out for an input level of 1.5 V_{CVBS}, giving modulation depth MDB. The Peak White Clip is defined as 100*(MDB)/(MBA).

2. The frequency dependent specifications are greatly influenced by the PCB layout in the application. These specifications have all been measured using a Motorola application layout and circuit similarly as shown in Figures 19 and 21. The reference number for ordering this evaluation board is MC44350EVK.

Figure 6. Video Signal to Noise

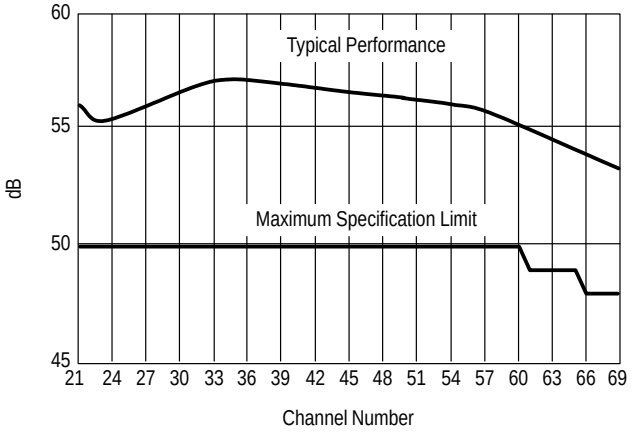
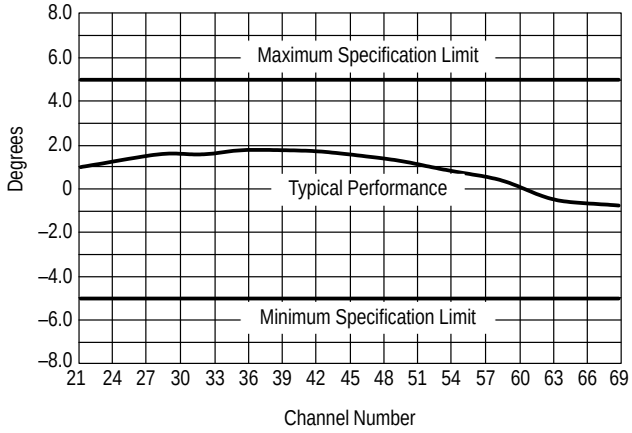


Figure 7. Differential Phase

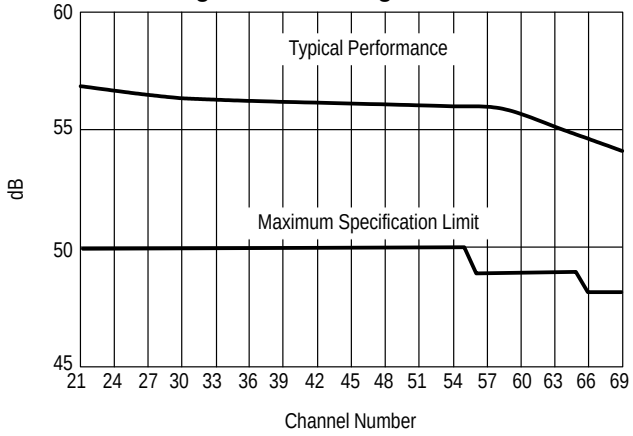


AUDIO CHARACTERISTICS

Characteristic	Test Conditions	Min	Typ	Max	Unit	Type
Audio input level AM Step 3, (SECAM) fs = 6.5 MHz, (for 8 steps see Table 4 – MC44353 Only)	for 85% AM modulation of sound subcarrier	240	290	340	mVrms	B @ 6.5 MHz
Audio input level FM Step 3 fs = 5.5, 6.0 or 6.5 MHz, (for 8 steps see table 4 – MC44353/4 Only	for +/– 40 kHz deviation using specified pre–emphasis circuit (FM), Audio frequency= 1.0 kHz	240	305	370	mVrms	B @ 5.5 MHz
Audio input Level FM fs = 5.5, 6.0 or 6.5 MHz (MC44355 Only)		155	195	235	mVrms	B @ 5.5 MHz
Audio input level FM Step 3 fs = 4.5 MHz (NTSC), (for 8 steps see table 4 – MC44353/4 Only	for ±20 kHz deviation using specified pre–emphasis circuit (FM), Audio frequency= 1.0 kHz	240	305	370	mVrms	D
Audio input Level FM fs = 4.5 MHz (NTSC) (MC44355 Only)		155	195	235	mVrms	D
Audio input resistance	at 15 kHz	30	50	75	kΩ	B
Audio Frequency response Minimum	–3.0 dB; ref 1.0 kHz; using specified pre–emphasis circuit	–	–	40	Hz	D
Minimum	–1.5 dB; ref 1.0 kHz; using specified pre–emphasis circuit	–	–	60	Hz	D
Maximum		15	–	–	kHz	D
Audio Distortion FM (THD only)	@ 1.0 kHz; 100% mod (±50 kHz No Video	–	0.4	2	%	C
Audio Distortion AM (THD only)	@ 1.0 kHz; 85% mod, No Video	–	1.5	2.5	%	D
Audio S/N with Sync Buzz FM	See Figure 8	–	Figure 8	Figure 8	dB	C
Audio S/N with Sync Buzz AM	Ref 1 khz; 85% mod; Video input EBU color bar 75%; Audio BW 40 Hz to 15 kHz – Weighing filter CCIR 468–2	45	50	–	dB	D
Sound/Picture ratio Step 3 (8 steps of 1.0 dB, see table P/S Ratio – MC44353/4 only)	Step 3 (typ 80%) PAL & Step 1 (typ 80%) SECAM Video Mod depth	11	14.5	18	dB	B
Sound/Picture ratio Step 5 (2 settings, see table P/S Ratio – MC44355 only)		13	16.5	20	dB	B

NOTE: 1. The frequency dependent specifications are greatly influenced by the PCB layout in the application. These specifications have all been measured using a Motorola application layout and circuit similarly as shown in Figures 19 and 21. The reference number for ordering this evaluation board is MC44350EVK.

Figure 8. Audio Signal to Noise



HIGH FREQUENCY CHARACTERISTICS

Characteristic	Test Conditions	Min	Typ	Max	Unit	Type
RF Output Level	See Note 1 and Figure 9.	Figure 9	Figure 9	Figure 9	dbµV	B
Output Inhibit Attenuation	See Note 1 and Figure 10.	Figure 10	Figure 10	Figure 10	dB	C
UHF Oscillator Frequency Minimum	Using specified circuit	–	–	450	MHz	D
UHF Oscillator Frequency Maximum	Using specified circuit	860	–	–	MHz	D
Sound Subcarrier Harmonics (f_p + n*fs)	Ref Picture carrier	–	–62	–54	dBc	Max: D Typ: C
Second Harmonic of chroma subcarrier	Using red EBU bar	–	–71	–60	dBc	C
Chroma/Sound Intermodualtion: $f_p + (f_{snd} - f_{chr})$	Using red EBU bar	–	–81	–72	dBc	C
F_O (picture carrier) Spurious	See Note 1 and Figure 11.	–	Figure 11	Figure 11	dbµV	C
F_O (picture carrier) Harmonics	See Note 1 and Figure 12.	–	Figure 12	Figure 12	dbµV	C
In band spurious (f_o ±5.0 MHz)	No video or sound modulation	–	–	–75	dBc	C
$F_0 + F_1$ Intermodulation Product	F_O = 599.25 MHz F_1 = 200 MHZ (at 80 dBµV $F_0 + F_1$ = 799.25 MHz	–	–	–60	dBc	D

NOTE: 1. The frequency dependent specifications are greatly influenced by the PCB layout in the application. These specifications have all been measured using a Motorola application layout and circuit similarly as shown in Figures 19 and 21. The reference number for ordering this evaluation board is MC44350EVK.

Figure 9. RF Output Level

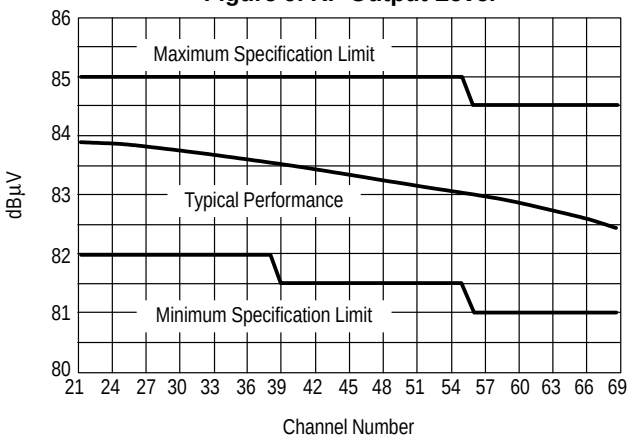


Figure 10. RF Output Inhibit Attenuation

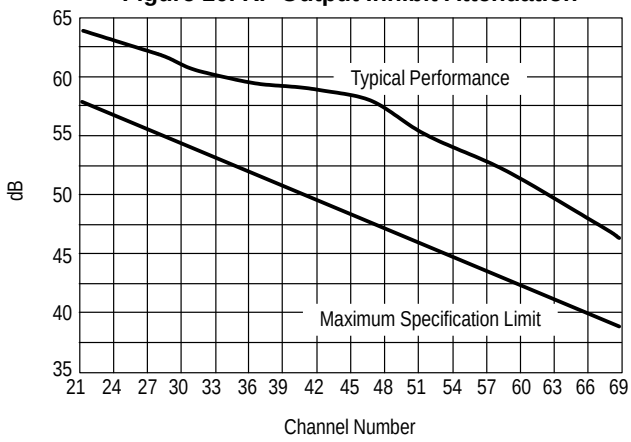


Figure 11. F_O (Picture Carrier) Spurious

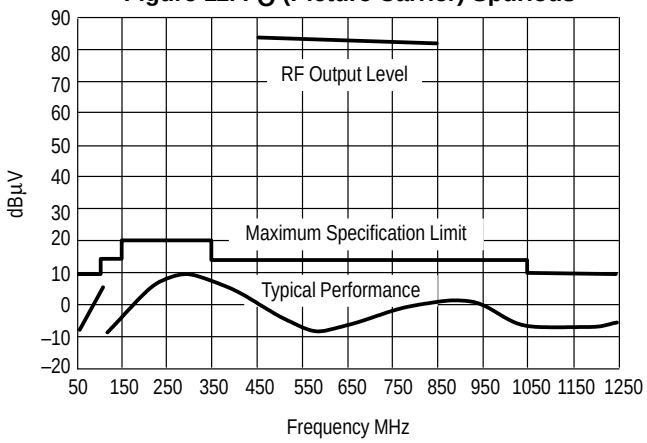
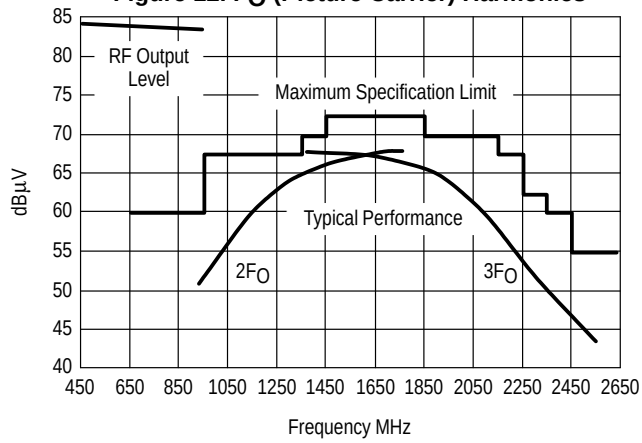


Figure 12. F_O (Picture Carrier) Harmonics



MODULATOR FUNCTIONAL DESCRIPTION

General

The device has two main sections; a PLL section to synthesize the channel frequency of the UHF output and a modulator section which accepts audio and video inputs and modulates the UHF carrier with them.

The channel frequency, sound and picture modulation index and sound/picture carrier ratio are all programmable by means of a high speed I^2C compatible bus. An on–chip video test pattern generator with an audio test signal is also included.

The MC44353 is designed to operate as a multi–standard modulator and can handle the systems B/G, D/K, H, I, L and N with the same external circuit components. The basic elements of the circuit are shown in Figure 1.

The Bus Receiver

The bus receiver operates I^2C compatible bus data format. Additional information on the data format is given on page 5. The chip address (I^2C bus) is: 1 1 0 0 1 0 1 0 (ACK) = $CA (hex). Each ninth data bit (bits 9, 18, 27, 36 and 45) is an ACK (acknowledge bit) during which the MCU sends a logic “1” and the Modulator circuit answers on the data line by pulling low. Besides the chip address the circuit needs 4 data bytes for operation. These bytes are defined in the section on control bits. The following sequences of data bytes are permitted:

Example 1	CA	C1	C0		
Example 2	CA	FM	FL		
Example 3	CA	C1	C0	FM	FL
Example 4	CA	FM	FL	C1	C0

For the significance of the control bits the section on control and test bit assignments on pages 11 and 12 should be consulted.

PLL SECTION

The programmable divider

The programmable divider’s division ratio is controlled by the state of control bits N0 to N11. The division ratio is given by:

N = 2048*N11+ 1024*N10 + ... + 4*N2 + 2*N1 + N0.

Max. ratio = 4095

Min. ratio = 17.

The prescaler

The prescaler is a fixed divide by 8 and is permanently engaged. It has a pre–amplifier for high sensitivity and good decoupling from the RF section.

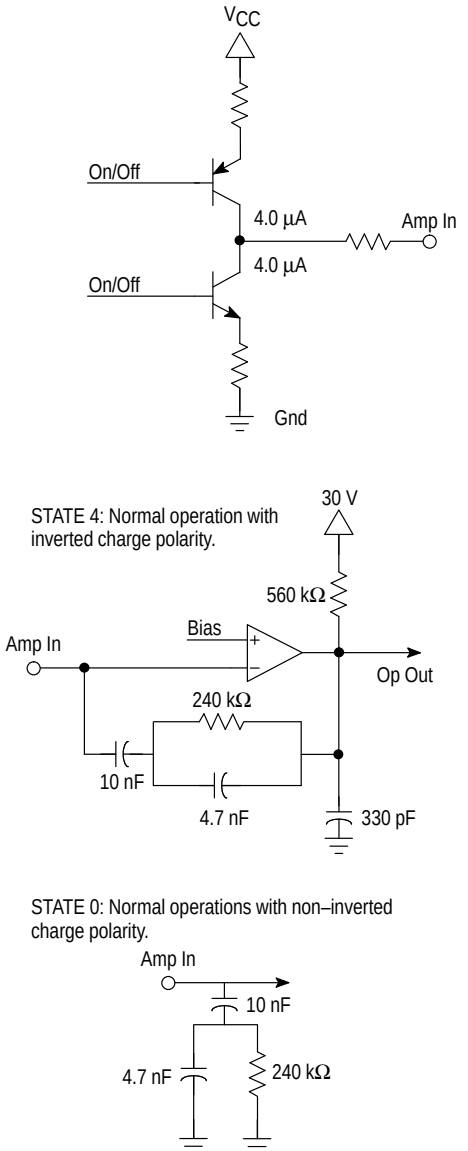
The phase comparator

The phase comparator has a current source/sink characteristic (charge pump, see Figure 13). The pump current is 4.0 μA. In normal operation (State 4) the phase comparator pulls high if the UHF oscillator frequency is too high. An internal amplifier is provided to generate tuning voltages greater than 5.0 V while inverting the output.

The phase comparator can also be programmed to work (in state 0) with the opposite charge pump polarity. In this case the phase comparator pulls low if the UHF frequency is too high. In this mode the amplifier is not required. The filter components may be connected directly to the phase comparator output pin. The tuning voltage range is then from just above 0 V to V_{CC} (5.0 V typical) and therefore not all channels can be synthesised without adjusting the circuit inductance.

Control bits T0, T1 and T2 are used to control the operational state of the phase comparator. A truth table is shown in the control bits section.

Figure 13. Output Configuration of the Phase Comparator



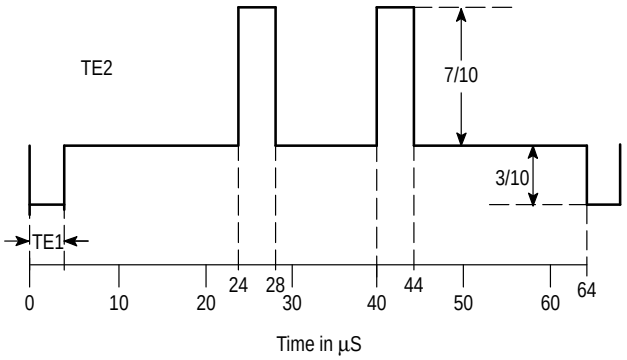
The reference divider

This divider divides by 128 resulting in a reference frequency of 31.25 kHz with a 4.0 MHz crystal. The UHF oscillator frequency may be synthesised in steps of 250 kHz. The 250 kHz steps are due to the presence of a divide by 8 prescaler prior to the programmable divider. The reference divider also generates the timing signals TE1 and TE2 for the on-chip test pattern generator and the audio test signal. The reference divider also provides the 7.8 kHz reference frequency for the Sound PLL.

Test Pattern Generator

A simple test pattern is generated on the IC which can be switched in under bus control to permit a TV receiver to easily tune in to the modulator output. The pattern consists of two white vertical bars on a black background and a 976 Hz audio test signal.

Figure 14. TPSG Typical Video Waveform



MODULATOR SECTION

Video Input–Clamp and Peak White Clip

The modulator requires a composite video input with negative going sync pulses and a nominal level of 1.0 V_{pp}. This signal is ac coupled to the video input where the sync tip level is clamped.

The video signal is then passed to a peak white clip circuit whose function is to soft clip the top of the video waveform if the amplitude from the sync tip to peak white goes too high. In this way over-modulation of the carrier by the video is avoided.

Sound Subcarrier Modulator

The sound modulator system consists of an FM modulator incorporating the sound subcarrier oscillator, and an AM modulator. The audio input signal is ac coupled into the amplifier which then drives the two types of modulator. In order to provide the accuracy needed for sound subcarrier frequencies, the sound oscillator consists of a phase/frequency locked loop. An external LC tank circuit is required, and the oscillator frequency is controlled by varicap tuning diodes. The resulting oscillator frequency is divided down by a divider whose ratio can be controlled via the bus. A phase/frequency comparator is then used to compare this frequency with a reference frequency (Fref 2), obtained from the main PLL Section. The resulting error voltage is used to control the varicap. To allow all tuning voltage to be derived from V_{CC}, a hyper–abrupt type of tuning diode is required to cover the necessary capacitance range. If only a single sound subcarrier frequency is being used, for example for PAL only or NTSC, then a less abrupt varicap diode may be used. The sound phase frequency comparator also requires an external loop filter.

The oscillator provides subcarrier frequencies of 4.5, 5.5, 6.0 and 6.5 MHz, selectable via the bus. For all applications except system L, the subcarrier is frequency modulated with the audio signal. For system L, amplitude modulation is employed. The level of audio at the input needed to give the maximum permissible modulation depth (50 kHz FM deviation, 85% AM depth), may be adjusted under bus control.

UHF Oscillator

The UHF oscillator is designed to operate over a range of 450 to 860 MHz. The oscillator drives an external LC tank circuit differentially, and is tuned by a varicap diode. The varicap tuning voltage, as described in an earlier section, is provided from an on chip operational amplifier and external filter arrangement which is controlled by the PLL Section of the chip. The UHF frequency thus generated is used by the modulator as the TV channel carrier frequency.

Video Modulator and Sound Mixer

This section of the circuit accepts as inputs:

1. composite video;
2. the selected sound subcarrier I^2C frequency;
3. the UHF carrier frequency at the selected channel;
4. the test pattern generator waveform.

Selection is made via the control bus between the composite video input and the on chip test pattern generator. The video and sound inter-carrier are used to amplitude modulate the UHF carrier. Negative modulation is used, except in the case of System L where positive modulation is used.In this part of the circuit, the video modulation depth and the sound to picture carrier ratio may be programmed under bus control. In system L mode the video modulation depth has the same range, but may extend to higher percentage values.

RF O/P Buffer

The TV signal generated in the video modulator and mixer section is fed to an emitter follower output stage, capable of driving a terminated line. This output is provided with a separate V_{CC} pin in order to avoid large circulating currents on the IC. It can provide at the output typically 84 dBµV of signal across a 75 Ω load.

Transient Output Inhibit

To minimize the risk of interference to other channels while the UHF PLL is acquiring lock on the desired frequency at Power-on, the UHF output stages are turned off for each power-on from zero and from standby mode. There is a timeout of 263 ms until the output is enabled. This allows the PLL to settle on its programmed frequency. Care must be taken therefore in determining the loop filter components so that the loop transient does not exceed this delay.

Data Retention

The circuit contains 4 bytes of memory holding the last frequency and control bits information. The circuit can retain this information at power down if a suitable V_{CC} is supplied.

The Standby V_{CC} of nominal 5.0 V must be applied to pin V_{CC} Mod. The 5.0 V current in data retention is approximately 500 µA. Note that the voltage source on this pin must be able to supply a much higher current in normal operation (typically 12 mA).

The circuit will enter into Data Retention Mode when the V_{CCA} pin voltage drops below approximately 3.0 V.

Test Modes

Various test modes can be enabled, by means of bits TB0–2 and X0–1. These operate by assigning some internal signals on the UHF phase comparator output current sources as outlined in the following 2 tables.

Table 1. Test Mode 1

Test Bits TB0 to TB2 are located in C0, bits 0 to 2:

TB2	TB1	TB0	State	Function
0	0	0	0	See Table Test Mode 2
0	0	1	1	Normal Operation, But Test Pattern Geneartor Disabled
0	1	0	2	Upper Source On, Lower Source Off
0	1	1	3	Lower Source On, Upper Source Off
1	0	0	4	Normal Operation with Inverted Charge Polarity
1	0	1	5	High Impedance
1	1	0	6	Test Ref divider on Upper Source (F_{ref}), Lower Source Off
1	1	1	7	Test Progr. divider on Lower Source ($F_{out/2}$), Upper Source Off

Table 2. Test Mode 2

Bits X0 and X1 are located in FL, bits 0 and 1:

X1	X0	State	Function
0	0	0a	Normal Operation with Non–Inverted Charge Pump Polarity
0	1	0b	Normal Inverted Operation (same as mode 4), but Transient Output Inhibit Disabled.
1	0	0c	Normal Inverted Operation (same as mode 4), but Transient Output Inhibit Circuitry Forced (output disabled).
1	1	0d	Normal Inverted Operation (same as mode 4), but Transient Output Inhibit counter Sped up (64 times).

In normal operation, the phase comparator pulls high if the UHF frequency is too high, and pulls low when the UHF frequency is too low. This mode is used when the tuning voltage is generated by the internal inverting operational amplifier, so in this case mode 4 (100) must be used.

Switching in mode 0d will reset the transient delay counter, which will time out at an accelerated rate of 64 times the normal rate.

Sound Section Test Modes

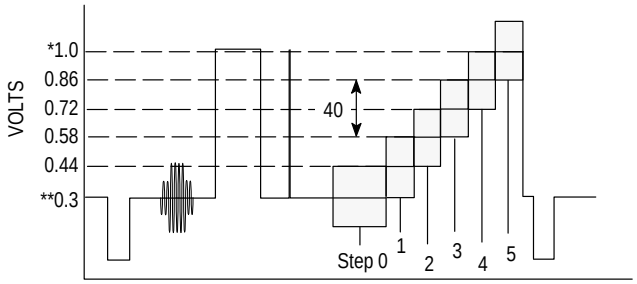
The Sound PLL is tested in a similar fashion, and responds to States 6 and 7 by placing the output of the sound PLL programmable divider on the upper current source.

Table 3. Sound Subcarrier Frequency

SFD1	SFD0	Sound Subcarrier Freq (MHz)
0	0	4.5
0	1	5.5
1	0	6.0
1	1	6.5

NOTE: 1. Bits SFD1–0 are located in C0 bits 4 and 3.

Figure 15. CCIR Test Line 330



NOTE: Not to scale
*100 IRE
** 1 IRE

Figure 16. Noise Measurement/Weighting Filter

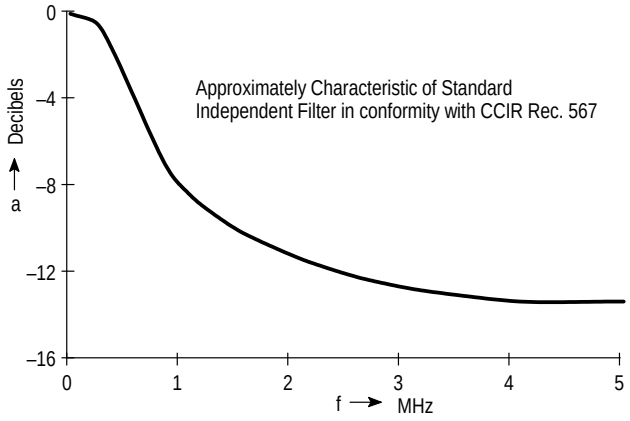


Table 4. Audio Modulation Sensitivity (Control Bits)

AMD2	AMD1	AMD0	Audio Input for FM PAL/NTSC (MC44353/4)	Audio Input for AM SECAM (MC44353 Only)	Audio Input for FM PAL/NTSC (MC44355 Only)
0	0	0	420 mVrms	405 mVrms	Not Programmable
0	0	1	375 mVrms	365 mVrms	Not Programmable
0	1	0	335 mVrms	325 mVrms	Not Programmable
0	1	1	300 mVrms	290 mVrms	Not Programmable
1	0	0	270 mVrms	260 mVrms	Not Programmable
1	0	1	240 mVrms	230 mVrms	Not Programmable
1	1	0	215 mVrms	205 mVrms	Not Programmable
1	1	1	190 mVrms	185 mVrms	190 mVrms

NOTE: 1. Audio sensitivity bits AMD2–0 are located in C1 bits 6 to 4.

Table 5. Picture to Sound Carrier Ratio (Control Bits)

PSD2	PSD1	PSD0	P/S Carrier Ratio (MC44353/4)	P/S Carrier Ratio (MC44355 Only)
0	0	0	11.5 dB	Not Programmable
0	0	1	12.5 dB	12.5 dB
0	1	0	13.5 dB	Not Programmable
0	1	1	14.5 dB	Not Programmable
1	0	0	15.5 dB	Not Programmable
1	0	1	16.5 dB	16.5 dB
1	1	0	17.5 dB	Not Programmable
1	1	1	18.5 dB	Not Programmable

NOTE: 1. Picture to sound carriers ratio bits PSD2–0 are located in C1 bits 3 to 1.

Table 6. Video Modulation Depth (Control Bits)

VMD2	VMD1	VMD0	Video Mod Depth PAL (MC44353/4)	Video Mod Depth SECAM (MC44353 Only)	Video Mod Depth PAL (MC44355 Only)
0	0	0	74.5%	78%	Not Programmable
0	0	1	77%	80.5%	Not Programmable
0	1	0	79.5%	83%	Not Programmable
0	1	1	82%	85.5%	82%
1	0	0	84.5%	88%	Not Programmable
1	0	1	87%	90.5%	Not Programmable
1	1	0	89.5%	93%	Not Programmable
1	1	1	92%	95.5%	Not Programmable

NOTES: 1. Video modulation depth bits VMD2–0 are located in C0 bits 7 to 5.
2. SECAM values are approximately 5% higher than PAL values.

Figure 17. Pin Circuit Schematic

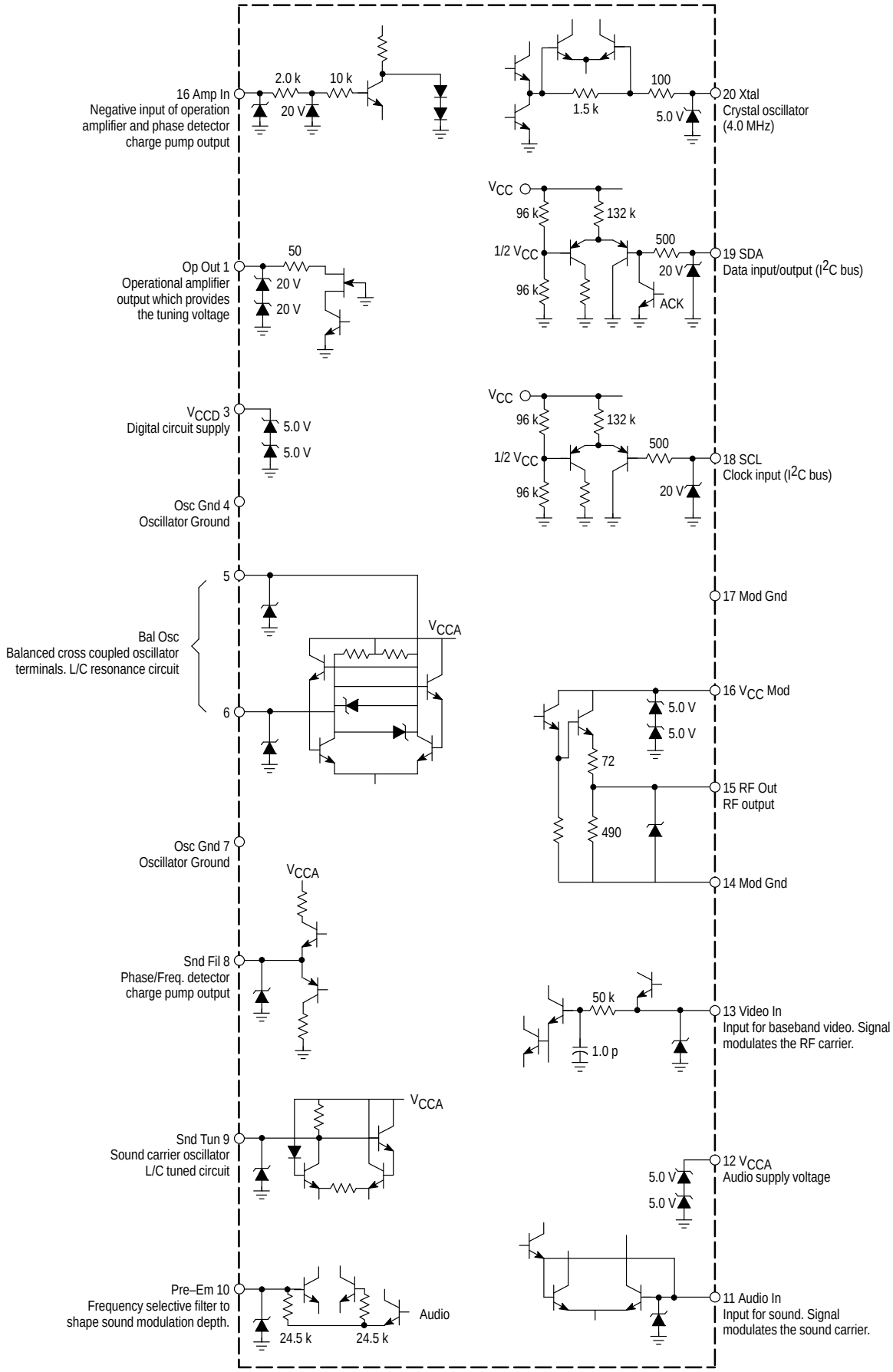
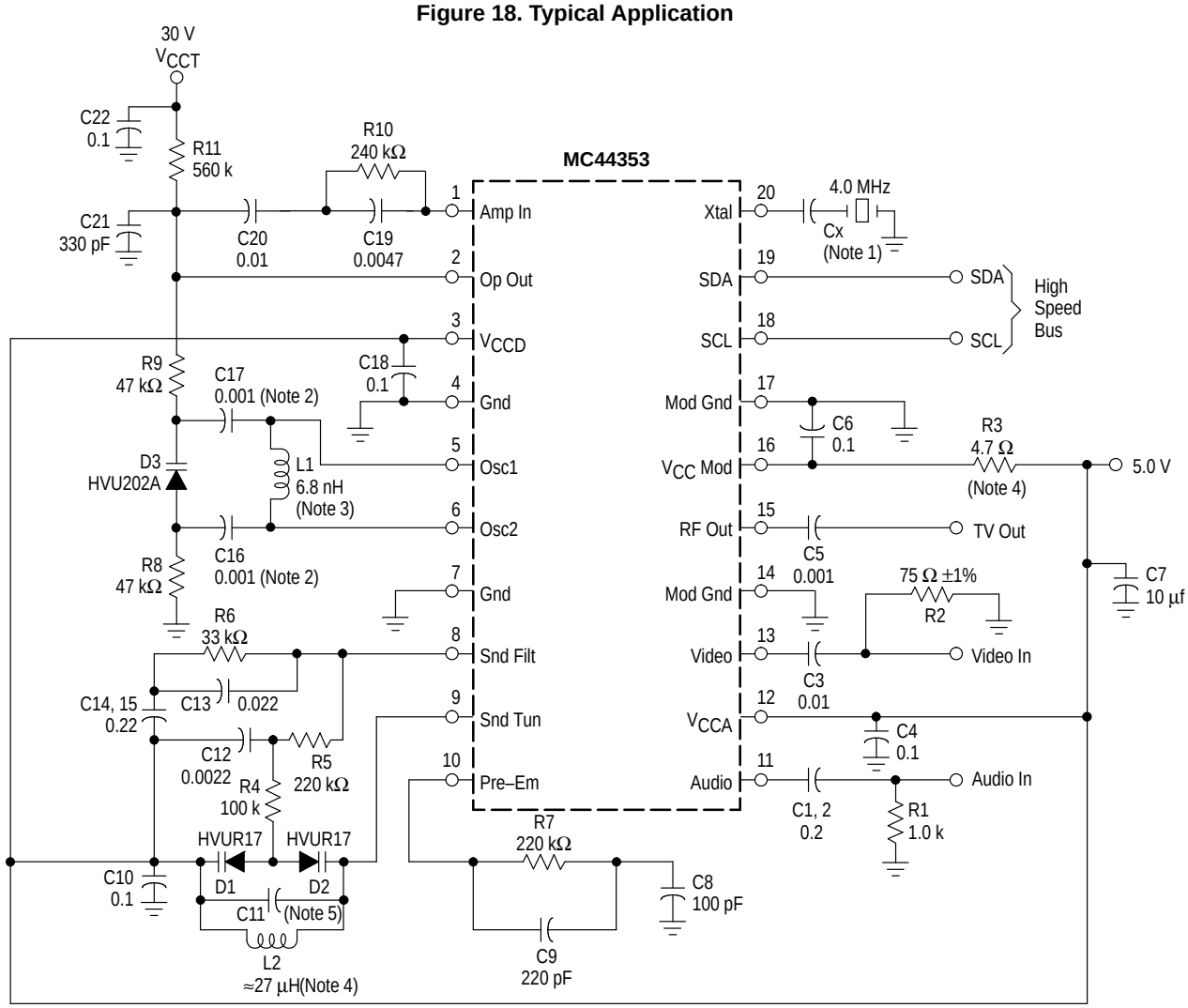


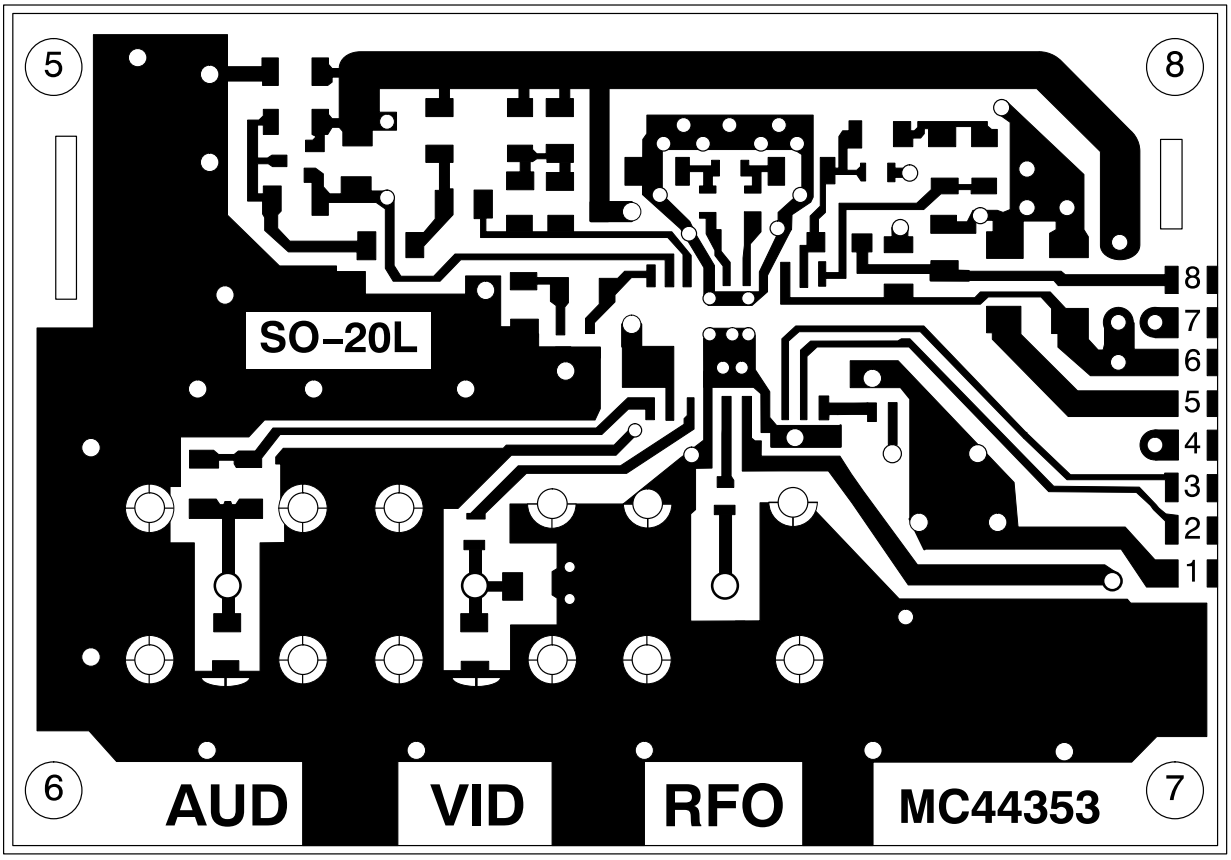
Figure 18. Typical Application



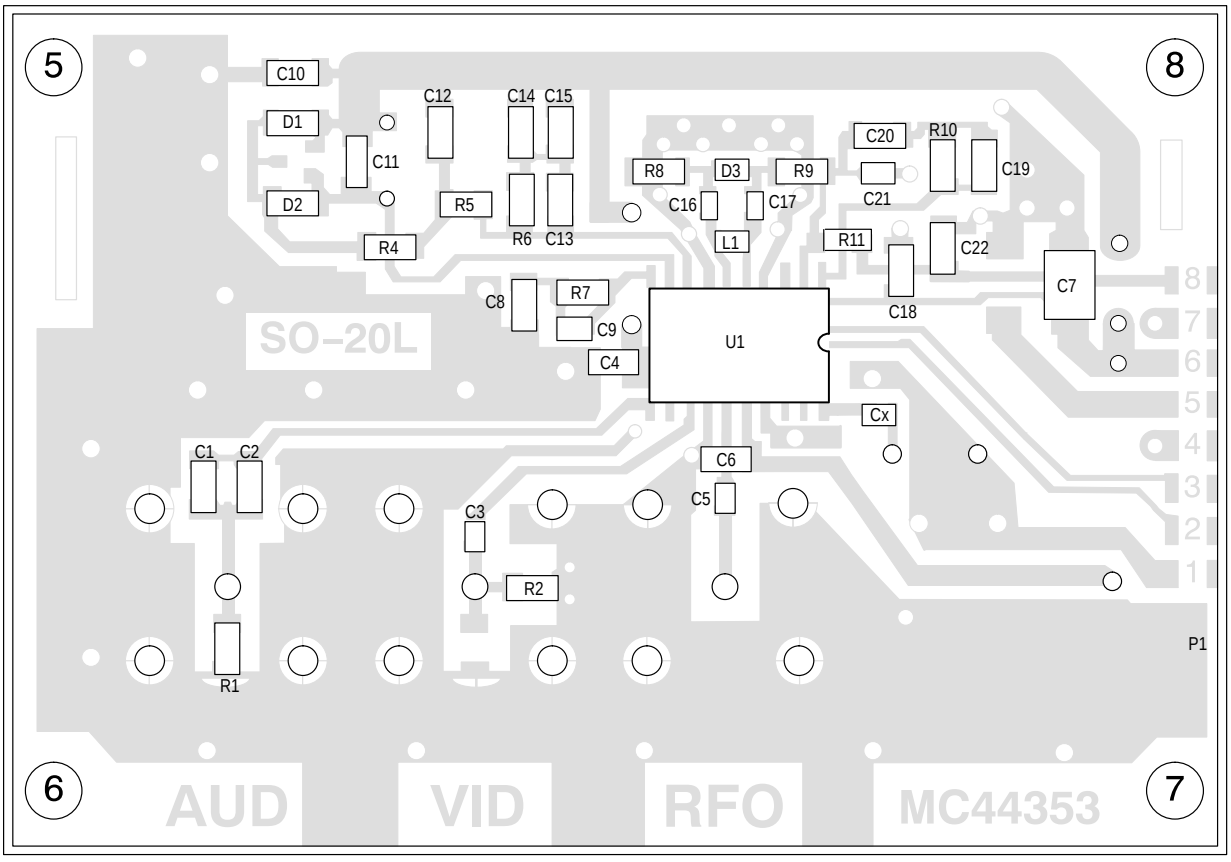
NOTES: 1. Cx depends on Crystal Load Capacitance, Crystal resistance < 200 Ω.
2. Tubular 0603 1.0 nF capacitors.
3. L1 is a 2 turn air coil.
4. L2 and R3 are non–surface mount components. Note L2 quality factor should be high enough to keep the sound carrier at the typical level Q min @ 5.5 MHz = 43, Q min @ 6.0 MHz = 40, and Q min @ 6.5 MHz = 37.
5. C11 and L2 are selected to control the sound carrier center frequency and its tuning range.
6. D1 and D2 are hyper–abrupt varactor. Minimum capacitance ratio between 1.0 and 4.5 V is C1/C4.5 = 5.6 to cover the full frequncy range. (C @ 1.0 V = 50 pF min)

Modifications to the application layout (Figures 19 through 21) will have an effect on the overall application performances. The most sensitive areas are around the UHF Oscillator and RF Output (Pins 4 to 7 and Pins 14 to 17) so care must be taken to reproduce a similar PCB layout in the final application.

Figure 19. PCB Layout for SO–20L (Top Layer)

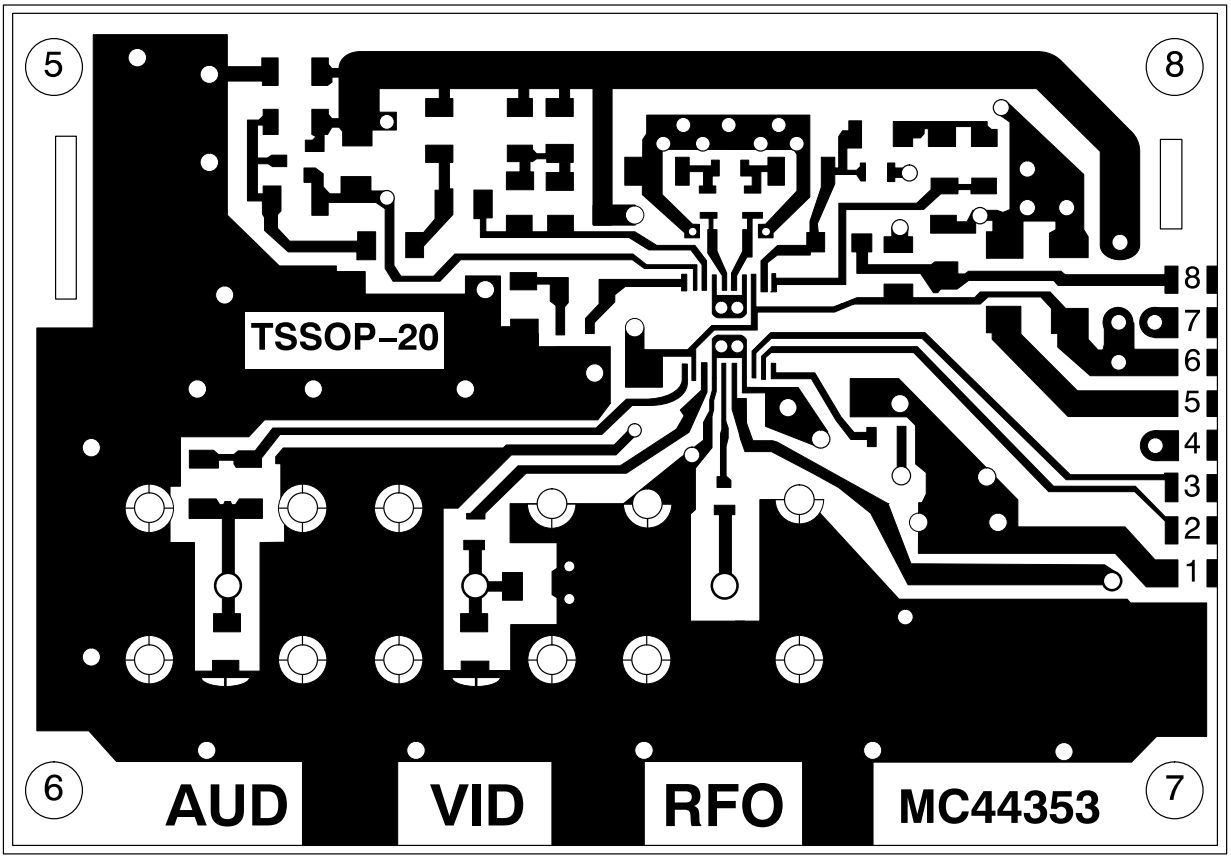


Scale 2:1

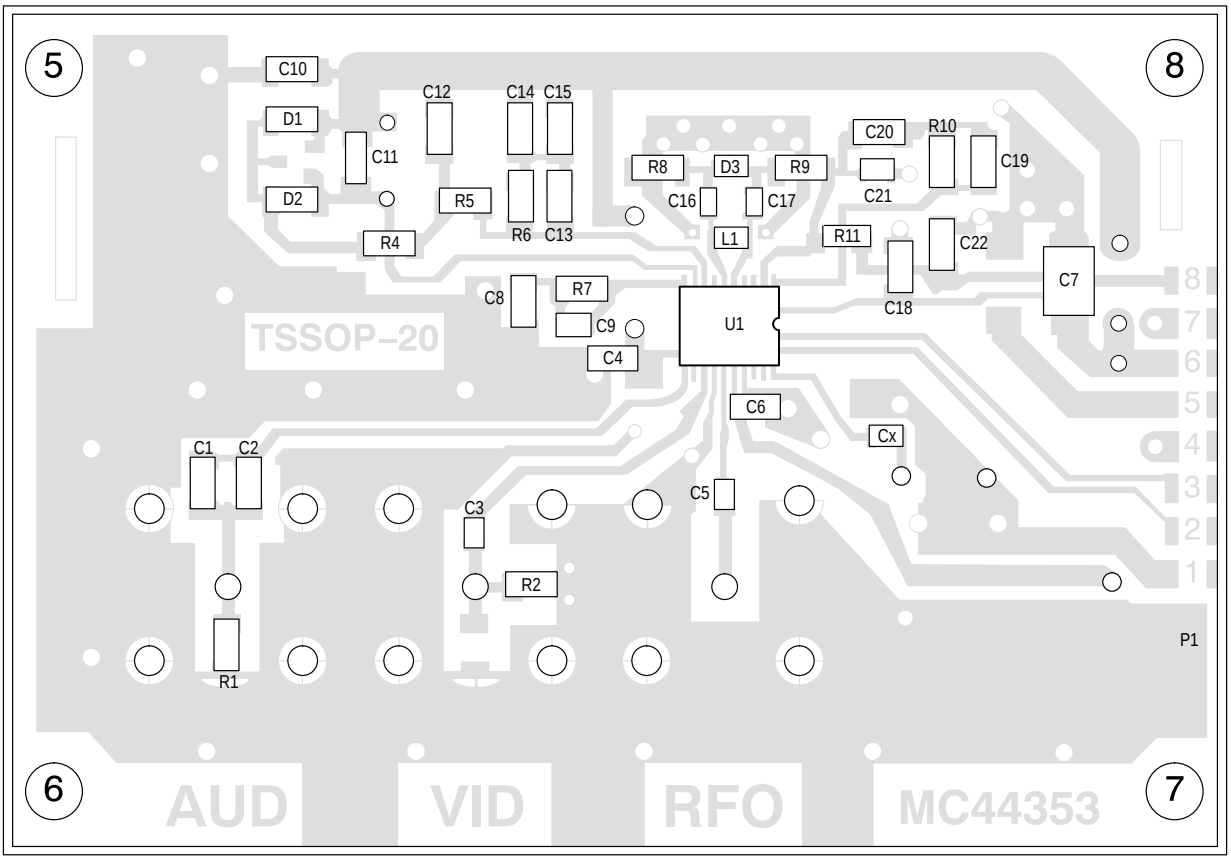


15 Pin D Connector

Figure 20. PCB Layout for TSSOP–20 (Top Layer)

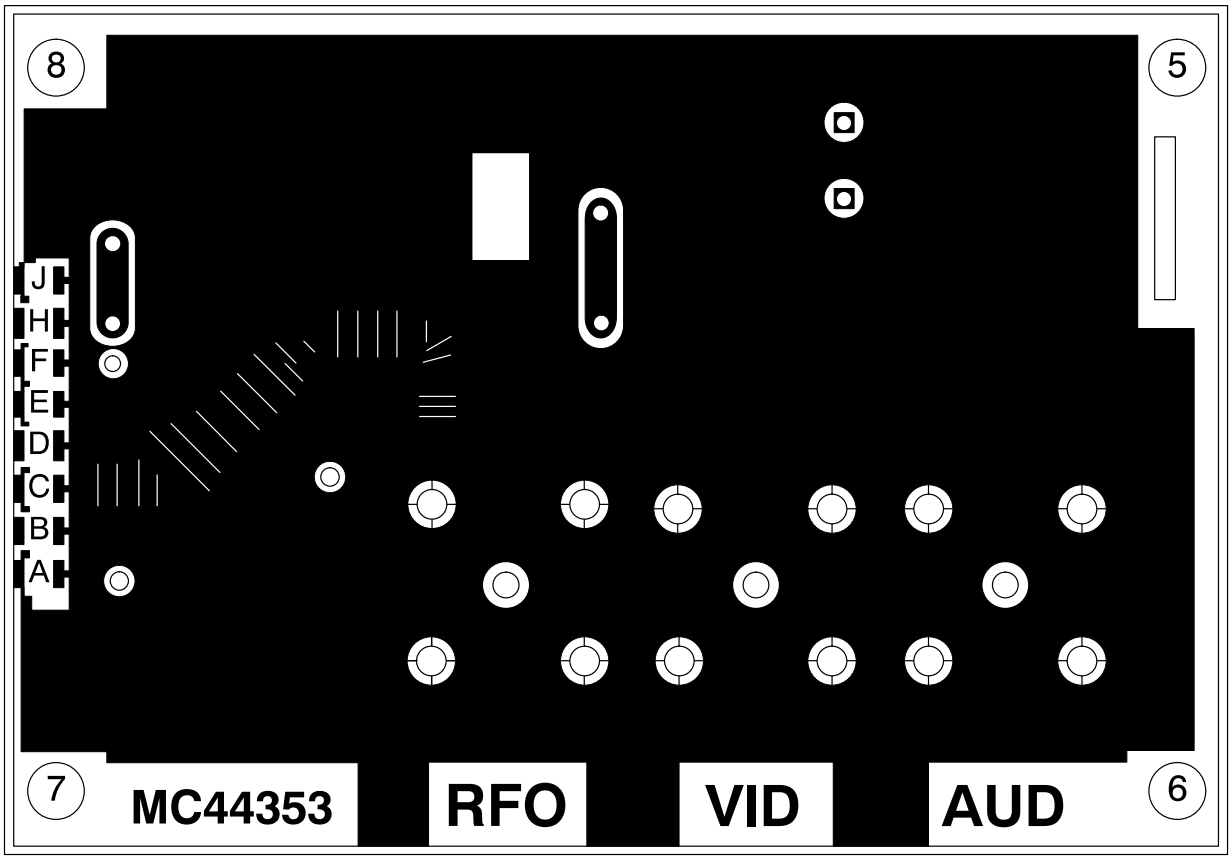


Scale 2:1

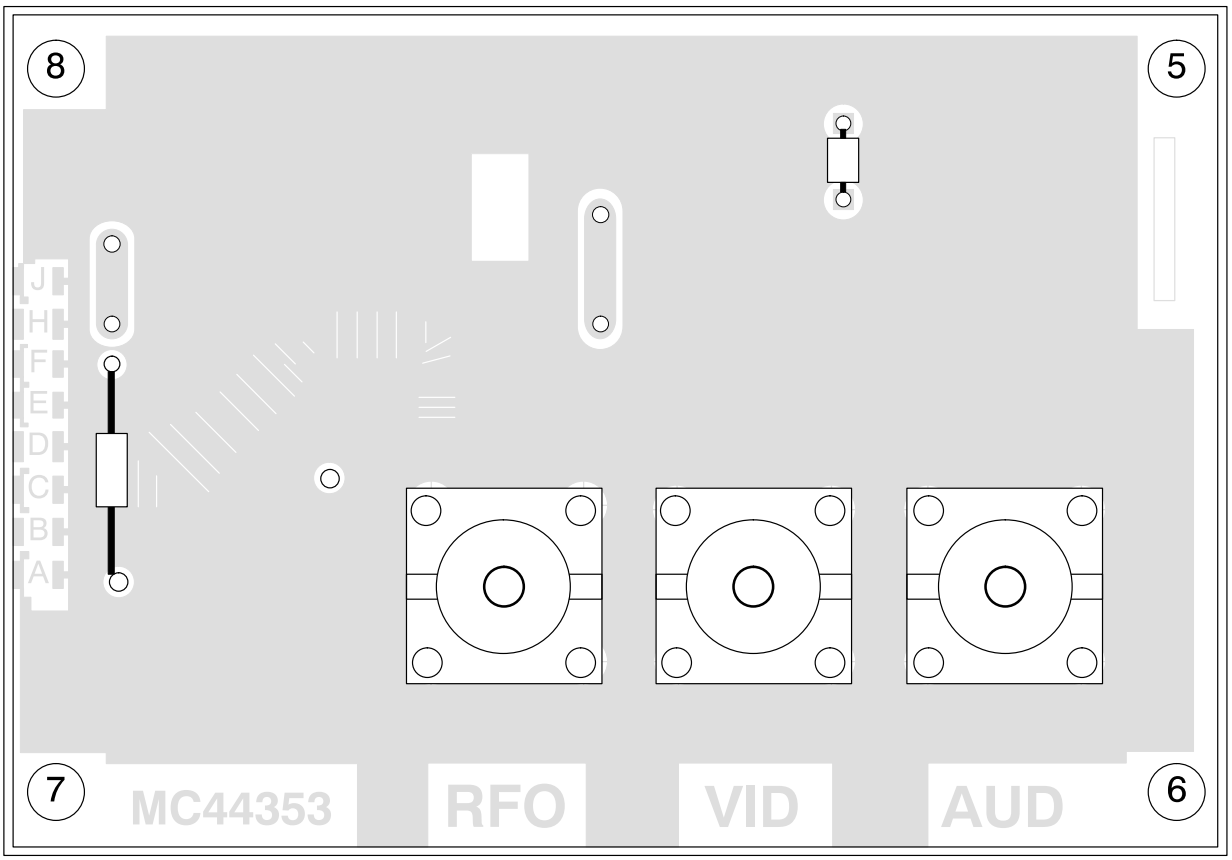


15 Pin D Connector

Figure 21. PCB Layout for SO−20L and TSSOP−20 used for Characterization (Bottom Layer)

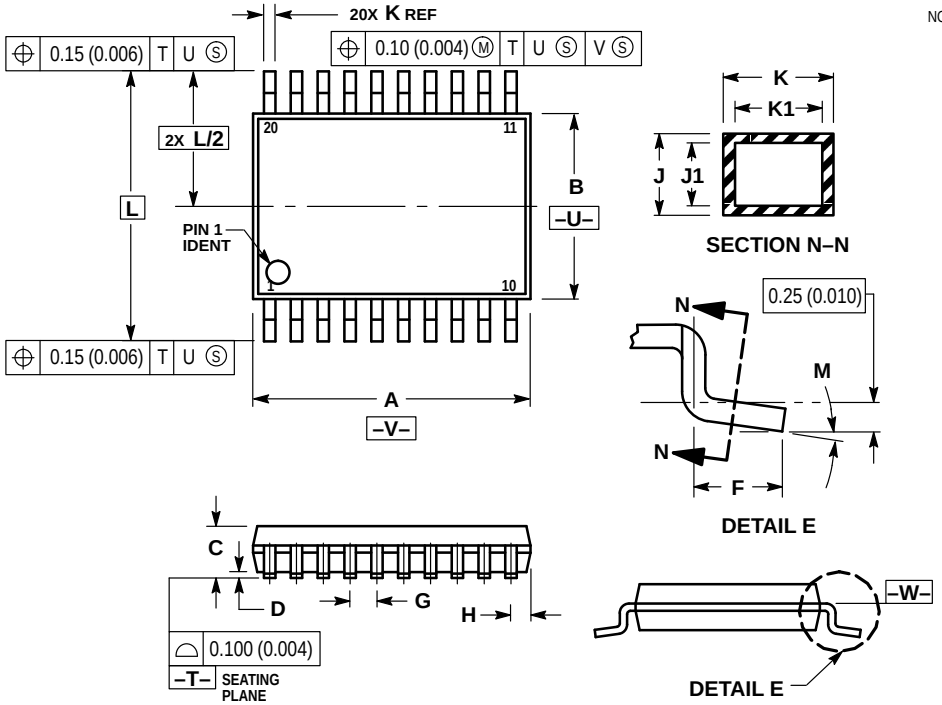


Scale 2:1



OUTLINE DIMENSION

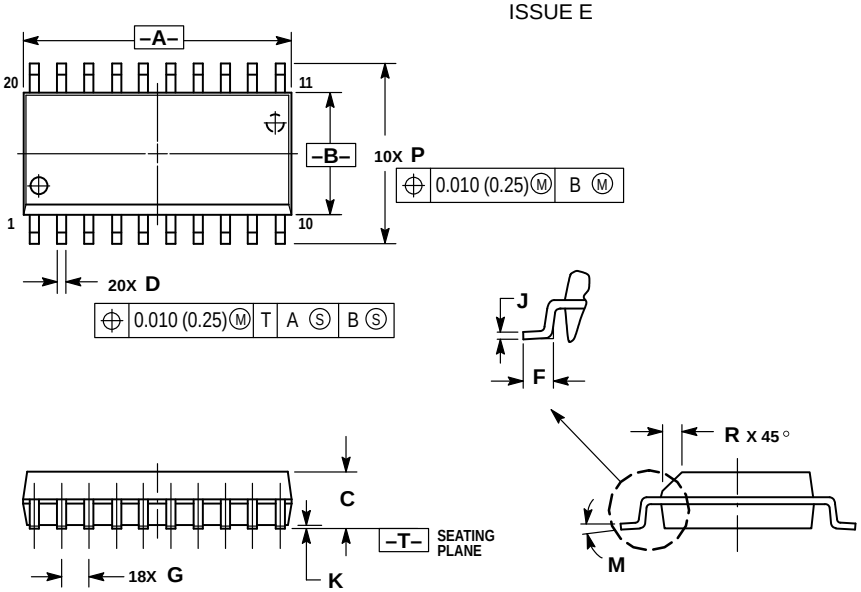
DTB SUFFIX
PLASTIC PACKAGE
CASE 948E–02
(TSSOP–20)
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

DW SUFFIX
PLASTIC PACKAGE
CASE 751D–04
(SO–20WB)
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 141,
4–32–1 Nishi–Gotanda, Shagawa–ku, Tokyo, Japan. 03–5487–8488

Customer Focus Center: 1–800–521–6274

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 1–602–244–6609
Motorola Fax Back System – US & Canada ONLY 1–800–774–1848
– http://sps.motorola.com/mfax/

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

HOME PAGE: http://motorola.com/sps/