MC68230

Technical Summary

Parallel Interface/Timer

The MC68230 parallel interface/timer (PI/T) provides versatile double-buffered parallel interfaces and a system-oriented timer for MC68000 systems. The parallel interfaces operate in unidirectional or bidirectional modes, either 8 or 16 bits wide. In the unidirectional modes, an associated data direction register determines whether each port pin is an input or output. In the bidirectional modes, the data direction registers are ignored, and the direction is determined dynamically by the state of four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low-, medium-, or high-speed peripherals or other computer systems. The PI/T ports allow use of vectored or autovectored interrupts, and also provide a direct memory access (DMA) request pin for connection to the MC68450 direct memory access controller (DMAC) or a similar circuit. The PI/T timer contains a 24-bit-wide counter and a 5-bit prescaler. The timer may be clocked by the system clock (PI/T CLK pin) or by an external clock (TIN pin), and a 5-bit prescaler can be used. The PI/T can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period; it can also be used for elapsed time measurement or as a device watchdog.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

The following features are included on the PI/T:

- M68000 Bus Compatible
- Port Modes Include:
  Bit I/O
  8- and 16-Bit Unidirectional
  8- and 16-Bit Bidirectional
- Programmable Handshaking Options
- 24-Bit Programmable Timer Modes
- Five Separate Interrupt Vectors, Four of which May Be Dedicated to External Interrupt Service Requests
- Separate Port and Timer Interrupt Service Requests
- Registers Are Read/Write and Directly Addressable
- Registers Are Addressed for Move Peripheral (MOVEP) and DMAC Compatibility

INTRODUCTION

The PI/T consists of two logically independent sections: the ports and the timer. The port section consists of port A (PA0–PA7), port B (PB0–PB7), four handshake pins (H1, H2, H3, and H4), two general input/output (I/O) pins, and six dual-function pins. The dual-function pins can individually operate as a third port (port C) or as an alternate function related to port A, port B, or the timer. The four programmable handshake pins, depending on the mode, can control data transfer to and from the ports, can be used as general-purpose I/O pins, or can be used as interrupt-generating edge-sensitive inputs with corresponding interrupt vector numbers (see Figure 1).

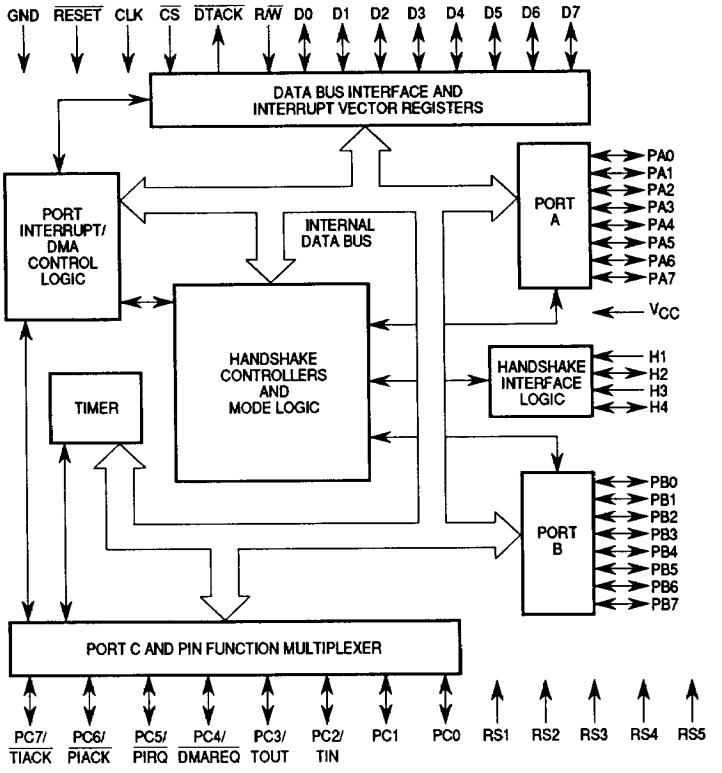

Figure 1. Block Diagram

The timer consists of a 24-bit counter, optionally clocked by a 5-bit prescaler. Three pins provide complete timer I/O: PC2/TIN, PC3/TOUT, and PC7/$\overline{\text{TIACK}}$. Only the ones needed for the given configuration perform the timer function, while the others remain port C I/O.

The system bus interface provides for asynchronous transfer of data from the PI/T to a bus master over the data bus (D0–D7). Data transfer acknowledge ($\overline{\text{DTACK}}$), register selects (RS1–RS5), timer interrupt acknowledge ($\overline{\text{TIACK}}$), read/write (R/$\overline{\text{W}}$), chip select ($\overline{\text{CS}}$), or port interrupt acknowledge ($\overline{\text{PIACK}}$) control data transfers between the PI/T and an M68000 processor.

PORT MODE DESCRIPTION

The primary focus of most applications will be on port A, port B, the handshake pins, the port interrupt pins, and the DMA request pin. They are controlled in the following way: the port general-control register contains a 2-bit field that specifies one of four operation modes. These modes govern the overall operation of the ports and determine their interrelationships. Some modes require additional information from each port's control register to further define its operation. Each port control register contains a 2-bit submode field that serves this purpose. Each port mode/submode combination specifies a set of programmable characteristics that fully define the behavior of that port and two of the handshake pins. This structure is summarized in Table 1 and Figure 2.

Table 1. Port Mode Control Summary

Mode 0 (Unidirectional 8-Bit Mode)
- Port A
  - Submode 00 — Pin-Definable Double-Buffered Input or Single-Buffered Output
    - H1 — Latches input data
    - H2 — Status/interrupt generating input, general-purpose output, or operation with H1 in the interlocked or pulsed handshake protocols
  - Submode 01 — Pin-Definable Double-Buffered Output or Nonlatched Input
    - H1 — Indicates data received by peripheral
    - H2 — Status/interrupt generating input, general-purpose output, or operation with H1 in the interlocked or pulsed handshake protocols
  - Submode 1X — Pin-Definable Single-Buffered Output or Nonlatched Input
    - H1 — Status/interrupt generating input
    - H2 — Status/interrupt generating input or general-purpose output
- Port B
  - H3/H4 — Identical to port A submodes, H1 and H2

Mode 1 (Unidirectional 16-Bit Mode)
- Port A — Most Significant Data Byte or Nonlatched Input or Single-Buffered Output
  - Submode XX — (Not Used)
    - H1 — Status/interrupt generating input
    - H2 — Status/interrupt generating input or general-purpose output
- Port B — Least Significant Data Byte
  - Submode X0 — Pin-Definable Double-Buffered Input or Single-Buffered Output
    - H3 — Latches input data
    - H4 — Status/interrupt generating input, general-purpose output, or operation with H3 in the interlocked or pulsed handshake protocols
  - Submode X1 — Pin-Definable Double-Buffered Output or Nonlatched Input
    - H3 — Indicates data received by peripheral
    - H4 — Status/interrupt generating input, general-purpose output, or operation with H3 in the interlocked or pulsed handshake protocols

Mode 2 (Bidirectional 8-Bit Mode)
- Port A — Bit I/O
  - Submode XX — (Not Used)
- Port B — Double-Buffered Bidirectional Data
  - Submode XX — (Not Used)
    - H1 — Indicates output data received by the peripheral and controls output drivers
    - H2 — Operating with H1 in the interlocked or pulsed output handshake protocols
    - H3 — Latches input data
    - H4 — Operation with H3 in the interlocked or pulsed input protocols

Mode 3 (Bidirectional 16-Bit Mode)
- Port A — Double-Buffered Bidirectional Data (Most Significant Data Byte)
  - Submode XX — (Not Used)
- Port B — Double-Buffered Bidirectional Data (Least Significant Data Byte)
  - Submode XX — (Not Used)
    - H1 — Indicates output data received by peripheral and controls output drivers
    - H2 — Operation with H1 in the interlocked or pulsed output handshake protocols
    - H3 — Latches input data
    - H4 — Operation with H3 in the interlocked or pulsed input handshake protocols

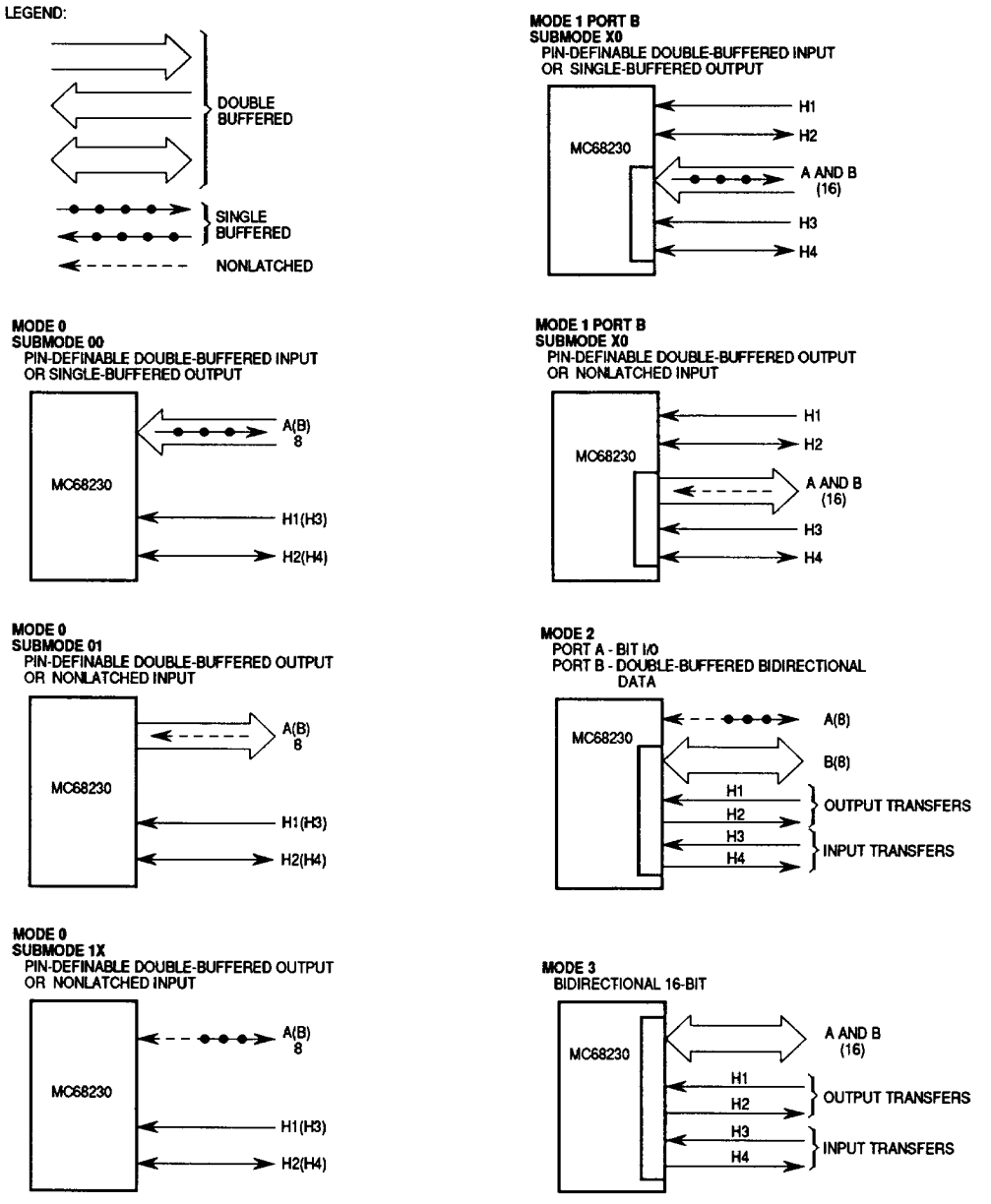

Figure 2. Port Mode Layout

SIGNAL DESCRIPTION

The input and output signals are illustrated functionally in Figure 3 and described in the following paragraphs.

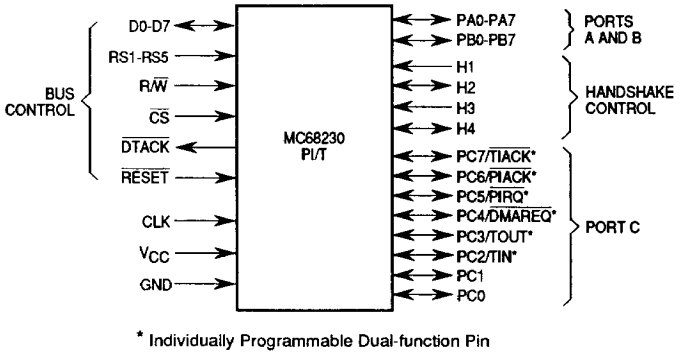

Figure 3. Functional Signal Groups

BIDIRECTIONAL DATA BUS (D0–D7)

The active-high data bus pins, D0–D7, form an 8-bit bidirectional data bus to/from an M68000 bus master.

REGISTER SELECT PINS (RS1–RS5)

The register select pins, RS1–RS5, are active-high high-impedance inputs that determine which of the 23 internal registers is being selected. They are provided by the M68000 bus master or other bus master.

READ/WRITE (R/$\overline{W}$)

R/$\overline{W}$ is a high-impedance read/write input signal from the M68000 bus master, indicating whether the current bus cycle is a read (high) or write (low) cycle.

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CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ is a high-impedance input that selects the PI/T registers for the current bus cycle. The data strobe (upper or lower) of the bus master, along with the appropriate address bits, must be included in the chip-select equation. A low level corresponds to an asserted chip select.

DATA TRANSFER ACKNOWLEDGE ($\overline{DTACK}$)

$\overline{DTACK}$ is an active-low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, $\overline{DTACK}$ is asserted after data has been provided on the data bus; during write cycles, it is asserted after data has been accepted on the data bus. $\overline{DTACK}$ is compatible with the MC68000 and with other M68000 bus mastsers such as the MC68450 DMAC. A pullup resistor is required to maintain $\overline{DTACK}$ high between bus cycles.

RESET ($\overline{RESET}$)

$\overline{RESET}$ is a high-impedance input used to initialize all PI/T functions. All control and data direction registers are cleared, and most internal operations are disabled by the assertion of $\overline{RESET}$ (low).

CLOCK (CLK)

The clock pin is a high-impedance TTL-compatible signal with the same specifications as the MC68000. Since the PI/T contains dynamic logic, this clock must not be gated off at any time. It is not necessary that this clock maintain any particular phase relationship with the M68000 system clock. It may be connected to an independent frequency source (faster or slower) as long as all bus specifications are met.

PORTS A AND B (PA0–PA7 and PB0–PB7)

Ports A and B are 8-bit ports that may be concatenated to form a 16-bit port in certain modes. The ports may be controlled in conjunction with the handshake pins, H1–H4. For stabilization during system power-up, ports A and B have internal pullup resistors to V_{CC}. All port pins are active high.

HANDSHAKE PINS (H1–H4)

Handshake pins H1–H4 are multipurpose pins that (depending on the operational mode) may provide an interlocked handshake, a pulsed handshake, interrupt-generating edge-sensitive inputs (independent of data transfers), or simple I/O pins. For stabilization during system power-up, H2 and H4 have internal pullup resistors to V_{CC}. The sense of H1–H4 (active high or low) may be programmed in bits 3-0 of the port general-control register. Independent of the mode, the instantaneous level of the handshake pins can be read from the port status register.

PORT C (PC0–PC7/ALTERNATE FUNCTION)

This port can be used as eight general-purpose I/O pins (PC0–PC7) or any combination of six special-function pins and two general-purpose I/O pins (PC0–PC1). Each dual-function pin can be a standard I/O or a special function independent of the other port C pins. When used as a port C pin, these pins are active high. They can be individually programmed as inputs or outputs by the port C data direction register. The dual-function pins are defined in the following paragraphs.

The alternate functions TIN, TOUT, and $\overline{\text{TIACK}}$ are timer I/O pins. TIN may be used as a rising-edge-triggered external clock input or an external run/halt control pin (the timer is in the run state if run/halt is high and in the halt state if run/halt is low). TOUT may provide an active-low timer interrupt request output or a general-purpose square-wave output, initially high. $\overline{\text{TIACK}}$ is an active-low high-impedance input used for timer interrupt acknowledge.

The port functions of the PI/T (ports A and B) have an independent pair of active-low interrupt request ($\overline{\text{PIRQ}}$) and interrupt acknowledge ($\overline{\text{PIACK}}$) pins.

The direct memory access request ($\overline{\text{DMAREQ}}$) pin provides an active-low DMAC request pulse for three clock cycles, completely compatible with the MC68450 DMAC. If these pins are used for an alternate function, the corresponding bit in the port C data direction register must be programmed as an input (0).

SIGNAL SUMMARY

Table 2 is a summary of all signals discussed in the previous paragraphs.

Table 2. Signal Summary

Signal Name	Input/Output	Active State	Edge/Level Sensitive	Output States
CLK	Input	—	Falling and Rising Edge	—
$\overline{CS}$	Input	Low	Level	—
D0–D7	Input/Output	High = 1, Low = 0	Level	High, Low, High Impedance
$\overline{DMAREQ}$	Output	Low	—	High, Low
$\overline{DTACK}$	Output	Low	—	High, Low, High Impedance*
H1(H3)***	Input	Low or High	Asserted Edge	—
H2(H4)**	Input or Output	Low or High	Asserted Edge	High, Low, High Impedance
PA0–PA7**, PB0–PB7**, PC0–PC7	Input/Output Input or Output	High = 1, Low = 0	Level	High, Low, High Impedance
$\overline{PIACK}$	Input	Low	Level	—
$\overline{PIRQ}$	Output	Low	—	Low, High Impedance*
RS1–RS5	Input	High = 1, Low = 0	Level	—
R/$\overline{W}$	Input	High Read, Low Write	Level	—
$\overline{RESET}$	Input	Low	Level	—
$\overline{TIACK}$	Input	Low	Level	—
TIN (External Clock)	Input	—	Rising Edge	—
TIN (Run/Halt)	Input	High	Level	—
TOUT (Square Wave)	Output	Low	—	High, Low
TOUT ($\overline{TIRQ}$)	Output	Low	—	Low, High Impedance*

*Pullup resistors required.
**Note these pins have internal pullup resistors.
***H1 is level sensitive for output buffer control in modes 2 and 3.

BUS INTERFACE OPERATION

The PI/T has an asynchronous bus interface, primarily designed for use with an MC68000 microprocessor. With care, however, it can be connected to synchronous buses.

In an asynchronous system, the PI/T clock may operate at a significantly different frequency (higher or lower) than the bus master and other system components if all bus specifications are met. The MC68230 CLK pin has the same specifications as the MC68000 CLK pin and must not be gated off.

The following signals generate normal read and write cycles to the PI/T: $\overline{CS}$, R/$\overline{W}$, RS1–RS5, DO–D7, and $\overline{DTACK}$. To generate interrupt acknowledge cycles, PC6/$\overline{PIACK}$ or PC7/$\overline{TIACK}$ is used instead of $\overline{CS}$, and RS1–RS5 are ignored. No combination of the following pin functions may be asserted simultaneously: $\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$.

TIMER OPERATION

The MC68230 timer can provide several facilities needed by MC68000 operating systems. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. Also, it can be used for elapsed-time measurement or as a device watchdog.

The PI/T contains a 24-bit synchronous down-counter that is loaded from three 8-bit counter preload registers. The 24-bit counter may be clocked by the output of a 5-bit (divide-by-32) prescaler or by an external timer input (TIN). If the prescaler is used, it may be clocked by the system clock (CLK) or by the TIN. The counter signals the occurrence of an event primarily through zero detection. (A zero is when the counter of the 24-bit timer is equal to zero). This sets the zero detect status (ZDS) bit in the timer status register. This bit may be checked by the processor or may be used to generate a timer interrupt. The ZDS bit can be reset by writing a one to the timer status register in that bit position, independent of timer operation.

The general operation of the timer is flexible and easily programmable. The timer is fully configured and controlled by programming the 8-bit timer control register. It controls 1) the choice between the port C operation of three timer pins, 2) whether the counter is loaded from the counter preload register or rolls over when zero detect is reached, 3) the clock input, 4) whether the prescaler is used, and 5) whether the timer is enabled.

REGISTER MODEL

A register model that includes the corresponding register selects is shown in Table 3.

Table 3. Register Model

Register Select Bits 5	4	3	2	1	7	6	5	4	3	2	1	0	Register Hex Value After RESET	Register
0	0	0	0	0	Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense	00	Port General-Control Register
0	0	0	0	1	*	SVCRQ Select		IPF Select		Port Interrupt Priority Control			00	Port Service Request Register
0	0	0	1	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	00	Port A Data Direction Register
0	0	0	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	00	Port B Data Direction Register
0	0	1	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	00	Port C Data Direction Register
0	0	1	0	1	Interrupt Vector Number						*	*	0F	Port Interrupt Vector Register
0	0	1	1	0	Port A Submode		H2 Control			H2 Int Enable	H1 SVCRQ Enable	H1 Stat Control	00	Port A Control Register
0	0	1	1	1	Port B Submode		H4 Control			H4 Int Enable	H3 SVCRQ Enable	H3 Stat Control	00	Port B Control Register
0	1	0	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Port A Data Register
0	1	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Port B Data Register
0	1	0	1	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	***	Port A Alternate Register
0	1	0	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	***	Port B Alternate Register
0	1	1	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	****	Port C Data Register
0	1	1	0	1	H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S	****	Port Status Register
0	1	1	1	0	*	*	*	*	*	*	*	*	00	(Null)
0	1	1	1	1	*	*	*	*	*	*	*	*	00	(Null)
1	0	0	0	0	TOUT/TIACK Control			Z D Control	Clock Control			Timer Enable	00	Timer Control Register
1	0	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0F	Timer Interrupt Vector Register
1	0	0	1	0	*	*	*	*	*	*	*	*	00	(Null)

Table 3. Register Model (Continued)

Register Select Bits 5	4	3	2	1	7	6	5	4	3	2	1	0	Register Hex Value After RESET	Register
0	0	0	0	0	Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense	00	Port General-Control Register
1	0	0	1	1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	**	Counter Preload Register (High)
1	0	1	0	0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	**	Counter Preload Register (Mid)
1	0	1	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Counter Preload Register (Low)
1	0	1	1	0	*	*	*	*	*	*	*	*	00	(Null)
1	0	1	1	1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	**	Count Register (High)
1	1	0	0	0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	**	Count Register (Mid)
1	1	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Count Register (Low)
1	1	0	1	0	*	*	*	*	*	*	*	ZDS	00	Timer Status
1	1	0	1	1	*	*	*	*	*	*	*	*	00	(Null)
1	1	1	0	0	*	*	*	*	*	*	*	*	00	(Null)
1	1	1	0	1	*	*	*	*	*	*	*	*	00	(Null)
1	1	1	1	0	*	*	*	*	*	*	*	*	00	(Null)
1	1	1	1	1	*	*	*	*	*	*	*	*	00	(Null)

*Unused, read as zero
**Value before RESET
***Current value on pins
****Undetermined value

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precuations be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value (Max)	Symbol	Value (Max)	Rating
Thermal Resistance	θ_{JA}		θ_{JC}		°C/W
Ceramic (L/LC)		40		15*	
Plastic (P)		40		20*	

DC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 Vdc ± 5%; T_A = 0 to 70°C; unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Input High Voltage	All Inputs	V_{IH}	GND +2.0	V_{CC}	V
Input Low Voltage	All Inputs	V_{IL}	GND −0.3	GND +0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)	H1, H3, R/$\overline{W}$, $\overline{RESET}$, CLK, RS1–RS5, $\overline{CS}$	I_{in}	—	10.0	μA
Hi-Z (Off State) Input Current	$\overline{DTACK}$, PC0–PC7, D0–D7	I_{TSI}	—	20	μA
(V_{in} = 0.4 to 2.4 V)	H2, H4, PA0–PA7, PB0–PB7		−0.1	−1.0	mA
Output High Voltage		V_{OH}	GND +2.4	—	V
(I_{Load} = −400 μA, V_{CC} = Min)	$\overline{DTACK}$, D0–D7				
(I_{Load} = −150 μA, V_{CC} = Min)	H2, H4, PB0–PB7, PA0–PA7				
(I_{Load} = −100 μA, V_{CC} = Min)	PC0–PC7				
Output low Voltage		V_{OL}	—	0.5	V
(I_{Load} = 8.8 mA, V_{CC} = Min)	PC3/TOUT, PC5/$\overline{PIRQ}$				
(I_{Load} = 5.3 mA, V_{CC} = Min)	D0–D7, $\overline{DTACK}$				
(I_{Load} = 2.4 mA, V_{CC} = Min)	PA0–PA7, PB0–PB7, H2, H4, PC0–PC2, PC4, PC6, PC7				
Maximum Internal Power Dissipation (Measured at T_A = 0°C)		P_{INT}	—	750	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz)		C_{in}	—	15	pF

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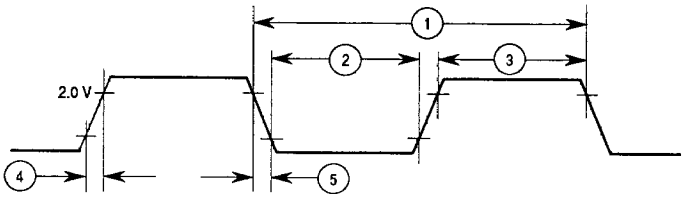
AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING (see Figure 4)

Num.	Characteristic	Symbol	8 MHz		10 MHz		Unit
			Min	Max	Min	Max	
	Frequency of Operation	f	2.0	8.0	2.0	10.0	MHz
1	Cycle Time	t_{cyc}	125	500	100	500	ns
2,3	Clock Pulse Width	t_{CL} t_{CH}	55 55	250 250	45 45	250 250	ns
4,5	Clock Rise and Fall Times	t_{Cr} t_{Cf}	— —	10 10	— —	10 10	ns



NOTE:
Timing measurements are referenced to and from a low voltage of 0.8 V and high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise of fall will be linear between 0.8 V and 2.0 V.

Figure 4. Clock Input Timing Diagram

AC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; T_A = 0°C to 70°C, unless otherwise noted; see Figures 5–10)

Num.	Characteristic	8 MHz		10 MHz		Unit
		Min	Max	Min	Max	
1	R/$\overline{W}$, RS1–RS5 Valid of $\overline{CS}$ Low (Setup Time)	0	—	0	—	ns
2	$\overline{CS}$ Low to R/$\overline{W}$ and RS1–RS5 Invalid (Hold Time)	100	—	65	—	ns
3[1]	$\overline{CS}$ Low to CLK Low (Setup Time)	30	—	20	—	ns
4[2]	$\overline{CS}$ Low to Data Out Valid	—	75	—	60	ns
5	RS1–RS5 Valid to Data Out Valid	—	140	—	100	ns
6	CLK Low to $\overline{DTACK}$ Low (Read/Write Cycle)	0	70	0	60	ns
7[3]	$\overline{DTACK}$ Low to $\overline{CS}$ High (Hold Time)	0	—	0	—	ns
8	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to Data Out Invalid (Hold Time)	0	—	0	—	ns
9	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to D0–D7 High Impedance	—	50	—	45	ns
10	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to $\overline{DTACK}$ High	—	50	—	45	ns
11	$\overline{CS}$ or PIACK or $\overline{TIACK}$ High to $\overline{DTACK}$ High Impedance	—	100	—	55	ns
12	Data In Valid to $\overline{CS}$ Low (Setup Time)	0	—	0	—	ns
13	$\overline{CS}$ Low to Data In Invalid (Hold Time)	100	—	65	—	ns
14	Port Input Data Valid to H1(H3) Asserted (Setup Time)	100	—	60	—	ns
15	H1(H3) Asserted to Port Input Data Invalid (Hold Time)	20	—	20	—	ns
16	Handshake Input H1(H4) Pulse Width Asserted	40	—	40	—	ns
17	Handshake Input H1(H4) Pulse Width Negated	40	—	40	—	ns
18	H1(H3) Asserted to H2(H4) Negated (Delay Time)	—	150	—	120	ns
19	CLK Low to H2(H4) Asserted (Delay Time)	—	100	—	100	ns
20[4]	H2(H4) Asserted to H1(H3) Asserted	0	—	0	—	ns
21[5]	CLK Low to H2(H4) Pulse Negated (Delay Time)	—	125	—	125	ns
22[9,10]	Synchronized H1(H3) to CLK Low on which $\overline{DMAREQ}$ Is Asserted	2.5	3.5	2.5	3.5	Clk. Per.
23	CLK Low on which $\overline{DMAREQ}$ is Asserted to CLK Low on which $\overline{DMAREQ}$ Is Negated	2.5	3	2.5	3	Clk. Per.
24	CLK Low to Port Output Data Valid (Delay Time) (Modes 0 and 1)	—	150	—	120	ns
25[9,10]	Synchronized H1(H3) to Port Output Data Invalid (Modes 0 and 1)	1.5	2.5	1.5	2.5	Clk. Per.
26	H1 Negated to Port Output Data Valid (Modes 2 and 3)	—	70	—	50	ns
27	H1 Asserted to Port Output Data High Impedance (Modes 2 and 3)	0	70	0	70	ns
28	Read Data Valid to $\overline{DTACK}$ Low (Setup Time)	0	—	0	—	ns
29	CLK Low to Data Output Valid, Interrupt Acknowledge Cycle	—	120	—	100	ns
30[7]	H1(H3) Asserted to CLK High (Setup Time)	50	—	40	—	ns
31	$\overline{PIACK}$ to $\overline{TIACK}$ Low to CLK Low (Setup Time)	50	—	40	—	ns
32[10]	Synchronized $\overline{CS}$ to CLK Low on which $\overline{DMAREQ}$ Is Asserted	3	3	3	3	Clk. Per.
33[9,10]	Synchronized H1(H3) to CLK Low on which H2(H4) Is Asserted	3.5	4.5	3.5	4.5	Clk. Per.

AC ELECTRICAL SPECIFICATIONS (Continued)

Num.	Characteristic	8 MHz		10 MHz		Unit
		Min	Max	Min	Max	
34	CLK Low to $\overline{DTACK}$ Low Interrupt Acknowledge Cycle (Delay Time)	—	100	—	100	ns
35	CLK Low to $\overline{DMAREQ}$ Low (Delay Time	0	120	0	100	ns
36	CLK Low to $\overline{DMAREQ}$ High (Delay Time)	0	120	0	100	ns
37[10]	Synchronized H1(H3) to CLK Low on which $\overline{PIRQ}$ Is Asserted	3.5	3.5	3.5	3.5	Clk. Per.
38[10]	Synchronized $\overline{CS}$ to CLK Low on which $\overline{PIRQ}$ Is High Impedance	3	3	3	3	Clk. Per.
39	CLK Low to $\overline{PIRQ}$ Low or High Impedance	0	250	0	225	ns
40[8]	TIN Frequency (External Clock) — Prescaler Used	0	1	0	1	f_{clk} (Hz)[6]
41	TIN Frequency (External Clock) — Prescaler Not Used	0	1/8	0	1/8	f_{clk} (Hz)[6]
42	TIN Pulse Width High or Low (External Clock)	55	—	45	—	ns
43	TIN Pulse Width Low (Run/Halt Control)	1	—	1	—	Clk. Per.
44	CLK Low to TOUT High, Low, or High Impedance	0	250	0	225	ns
45	$\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$ High to $\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$ Low	50	—	30	—	ns

NOTES:

1. This specification only applies if the PI/T had completed all operations initiated by the previous bus cycle when $\overline{CS}$ was asserted. Following a normal read or write busy cycle, all operations are complete within three clocks after the falling edge of the CLK pin on which $\overline{DTACK}$ was asserted. If $\overline{CS}$ is asserted prior to completion of these operations, the new bus cycle and $\overline{DTACK}$ are postponed. If all operations of the previous bus cycle were complete when $\overline{CS}$ was asserted, this specification is made only to ensure that $\overline{DTACK}$ is asserted with respect to the falling edge of the CLK pin as shown in the timing diagram not to guarantee operation of the part. If the $\overline{CS}$ setup time is violated, DTACK may be asserted as shown or may be asserted one clock later.
2. Assuming the RS1–RS5 to data valid time has also expired.
3. This specification imposes a lower bound on $\overline{CS}$ low time, guaranteeing that $\overline{CS}$ will be low for at least one CLK period.
4. This specification assures recognition of the asserted edge of H1(H3).
5. This specification applies only when a pulsed handshake option is chosen, and the pulse is not shortened due to any early asserted edge of H1(H3).
6. CLK refers to the actual frequency of the CLK pin, not the maximum allowable CLK frequency.
7. If the setup time on the rising edge of the clock is not met, H1(H3) may not be recognized until the next rising of the clock.
8. This limit applies to the frequency of the signal at TIN compared to the frequency of the CLK signal during each clock cycle. If any period of the waveform at TIN is smaller than the period of the CLK signal at that instant, then it is likely that the timer circuit will completely ignore one cycle of the TIN signal. If these two signals are derived from different sources they will have different instantaneous frequency variations. In this case, the frequency applied to the TIN pin must be distinctly less than the frequency at the CLK pin to avoid lost cycles of the TIN signal. With signals derived from different crystal oscillators applied to the TIN and CLK pins with fast rise and fall times, the TIN frequency can approach 80 to 90% of the frequency of the CLK signal without loss of a TIN cycle. If these two signals are derived from the same frequency source, then the frequency of the signal applied to TIN can be 100% of the frequency at the CLK pin. They may be generated by different buffers from the same signal or one may be an inverted version of the other. The TIN signal may be generated by an AND function of the clock and a control signal.
9. The maximum value is caused by a peripheral access (H1(H3) asserted) and bus access ($\overline{CS}$ asserted) occurring simultaneously.
10. Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1(H3) and falling edge for $\overline{CS}$).

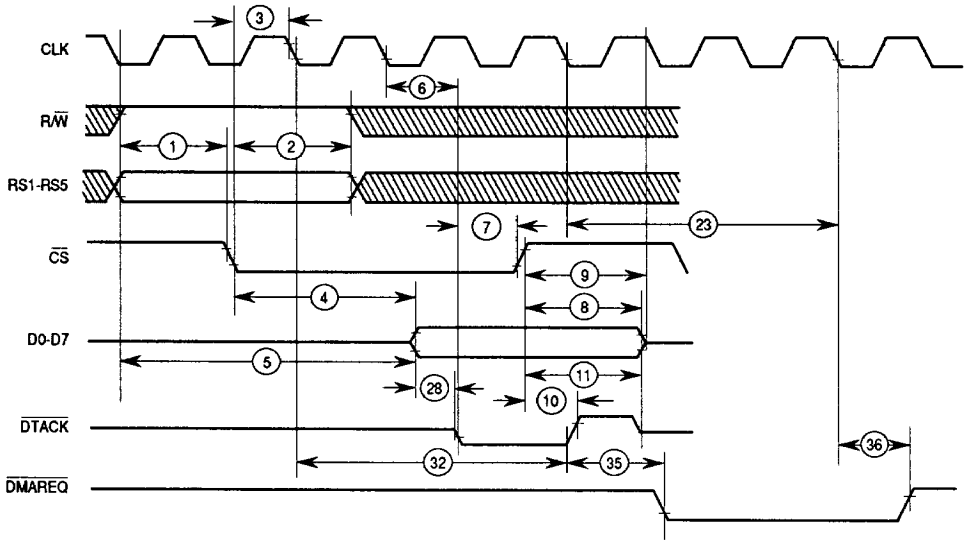


Figure 5. Read Cycle Timing Diagram

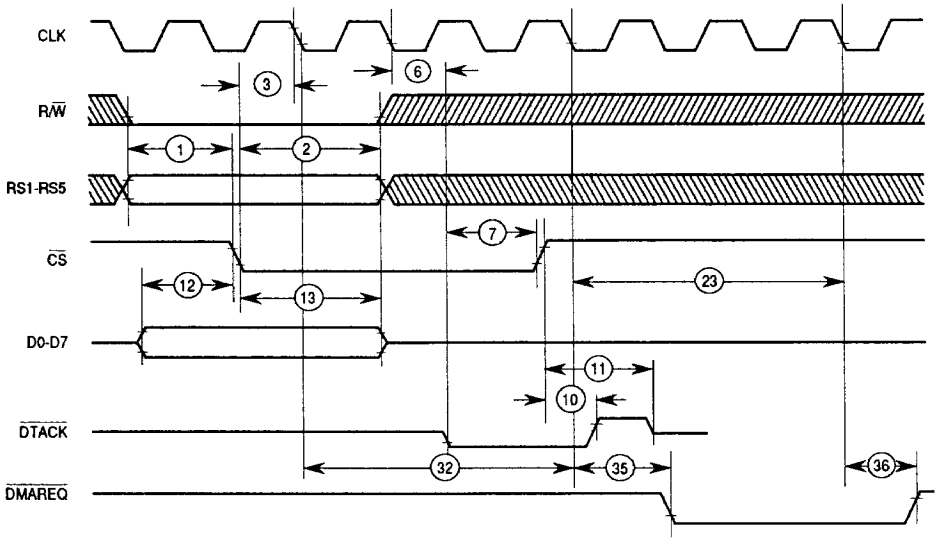
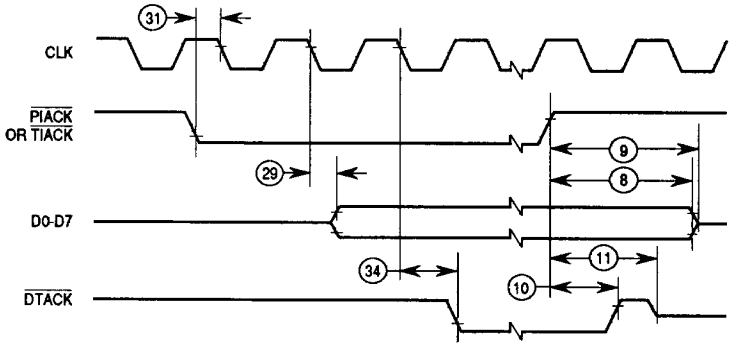
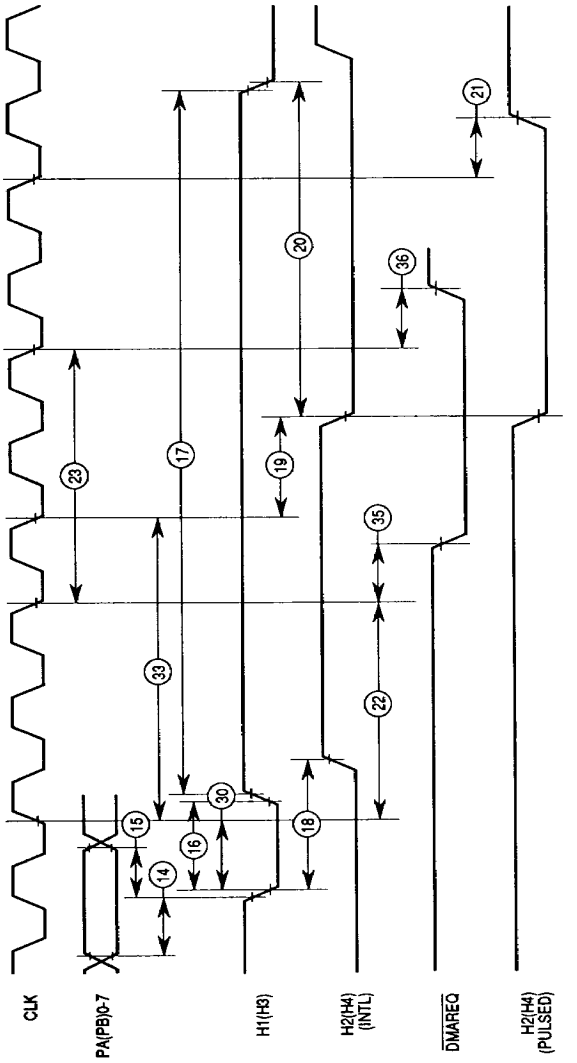


Figure 6. Write Cycle Timing Diagram



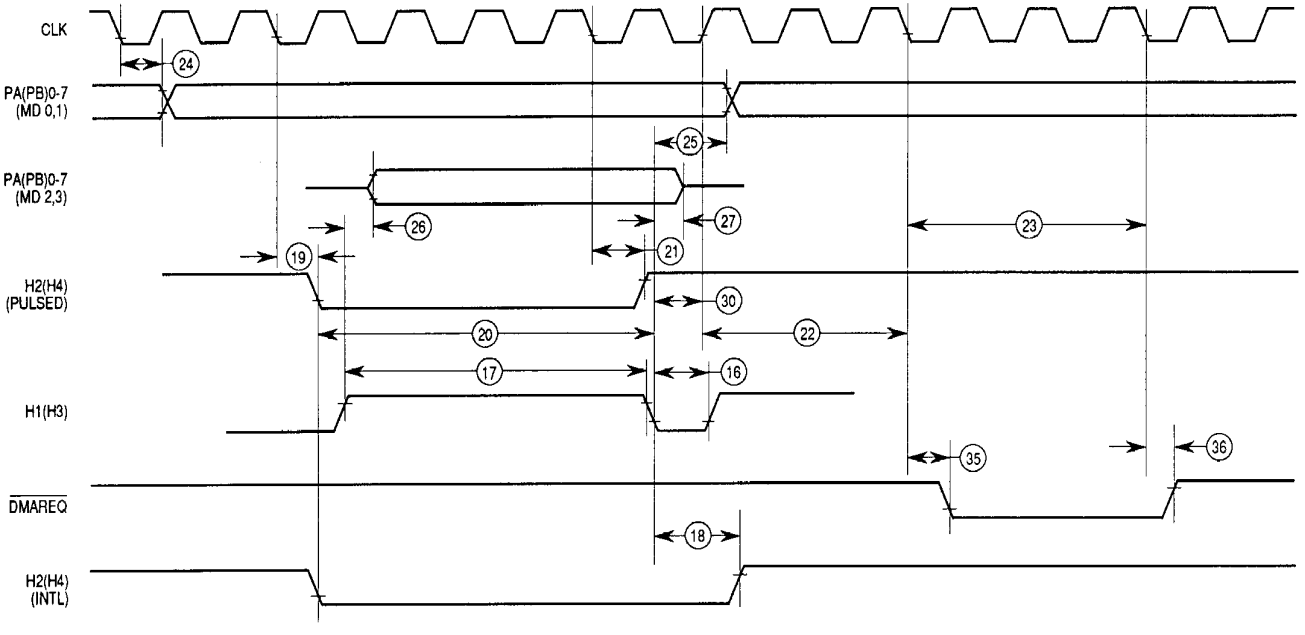
NOTE: Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted.

Figure 7. IACK Timing Diagram



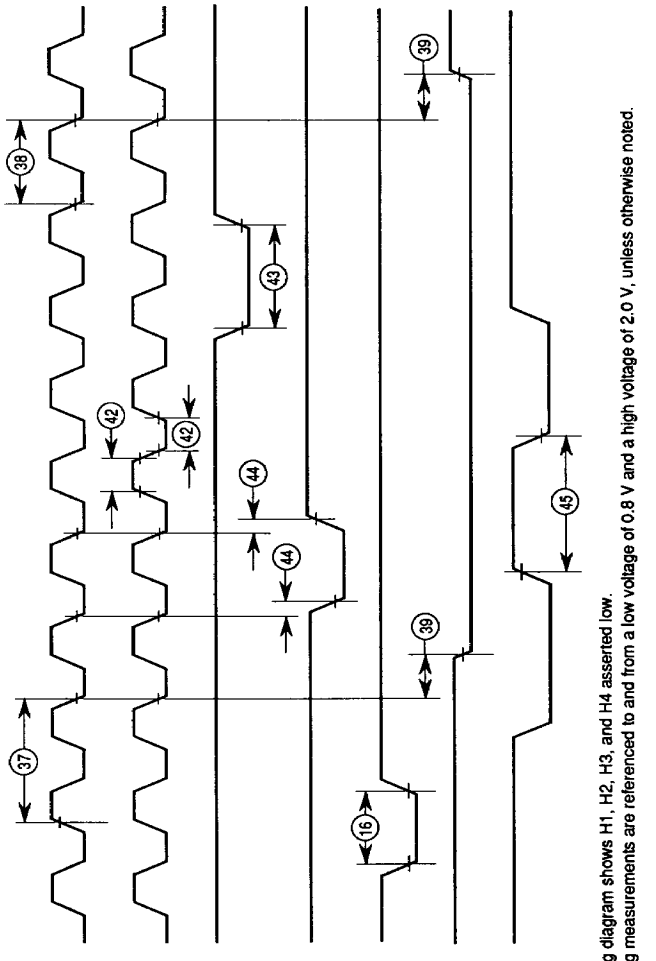
NOTES:
1. Timing diagram shows H1, H2, H3, and H4 asserted low.
2. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted.

Figure 8. Peripheral Input Timing Diagram



NOTES:
1. Timing diagram shows H1, H2, H3, and H4 asserted low.
2. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted.

Figure 9. Peripheral Output Timing Diagram

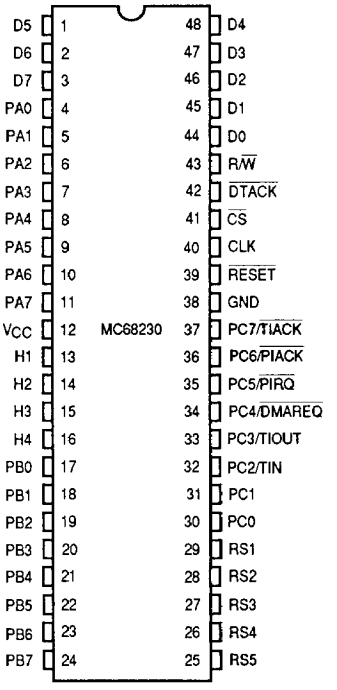


NOTES:
1. Timing diagram shows H1, H2, H3, and H4 asserted low.
2. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted.

Figure 10. TIN, TOUT, $\overline{\text{PIRQ}}$ Timing Diagram

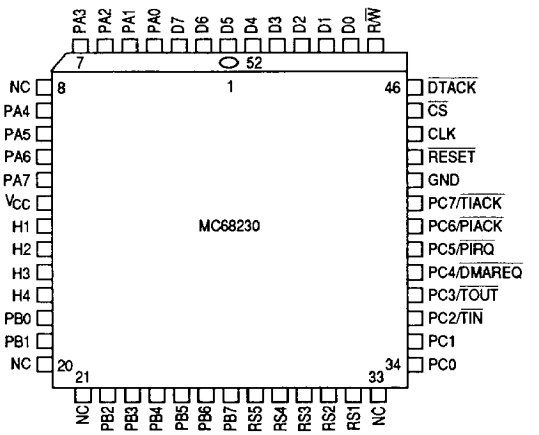
PIN ASSIGNMENTS

48-LEAD DUAL-IN-LINE PACKAGE



9

52-LEAD PLASTIC LEADED CHIP CARRIER



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