

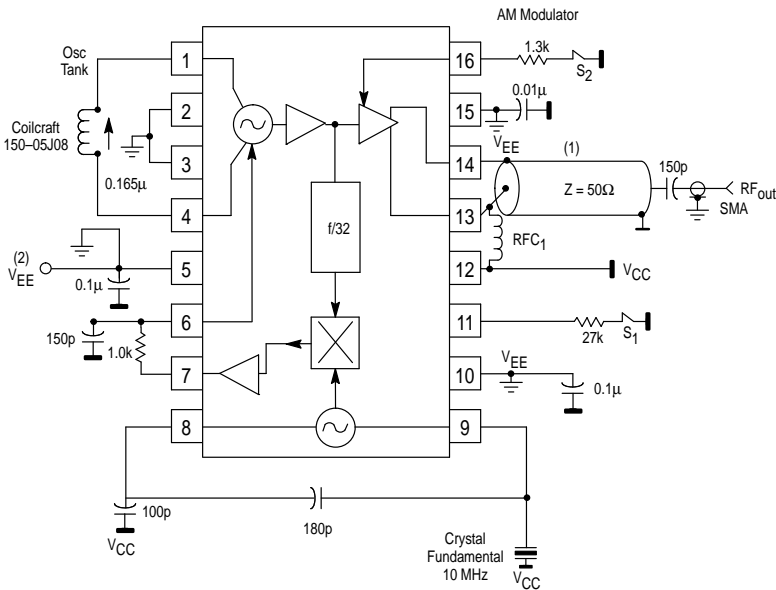


# UHF FM/AM Transmitter

The MC13176 is a one chip FM/AM transmitter subsystem designed for AM/FM communication systems. It include a Colpitts crystal reference oscillator, UHF oscillator,  $\div 32$  prescaler and phase detector forming a versatile PLL system. Targeted applications are in the 260 to 470 MHz band and the 902 to 928 MHz band covered by FCC Title 47; Part 15. Other applications include local oscillator sources in UHF and 900 MHz receivers, UHF and 900 MHz video transmitters, RF Local Area Networks (LANs), and high frequency clock drivers. The MC13176 offers the following features:

- UHF Current Controlled Oscillator
- Uses Easily Available 3rd Overtone or Fundamental Crystals for Reference
- Fewer External Parts Required
- Low Operating Supply Voltage (1.8 to 5.0 Vdc)
- Low Supply Drain Currents
- Power Output Adjustable (Up to 10 dBm)
- Differential Output for Loop Antenna or Balun Transformer Networks
- Power Down Feature
- ASK Modulated by Switching Output On and Off
- $f_o = 32 \times f_{ref}$

Figure 1. Typical Application as 320 MHz AM Transmitter



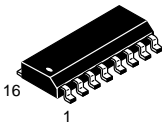
NOTES: 1. 50  $\Omega$  coaxial balun, 1/10 wavelength at 320 MHz equals 1.5 inches.  
2. Pins 5, 10 & 15 are ground and connected to  $V_{EE}$  which is the component/DC ground plane side of PCB. These pins must be decoupled to  $V_{CC}$ ; decoupling capacitors should be placed as close as possible to the pins.

Order this document by MC13176/D

## MC13176

### UHF FM/AM TRANSMITTER

#### SEMICONDUCTOR TECHNICAL DATA



D SUFFIX  
PLASTIC PACKAGE  
CASE 751B  
(SO-16)

#### PIN CONNECTIONS

Osc 1	1	16	I <sub>mod</sub>
NC	2	15	Out Gnd
NC	3	14	Out 2
Osc 4	4	13	Out 1
V <sub>EE</sub>	5	12	V <sub>CC</sub>
I <sub>Cont</sub>	6	11	Enable
PD <sub>out</sub>	7	10	Reg. Gnd
Xtaleb	8	9	Xtaleb

#### ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13176D	T <sub>A</sub> = - 40 to 85°C	SO-16

# MC13176

**MAXIMUM RATINGS** (  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

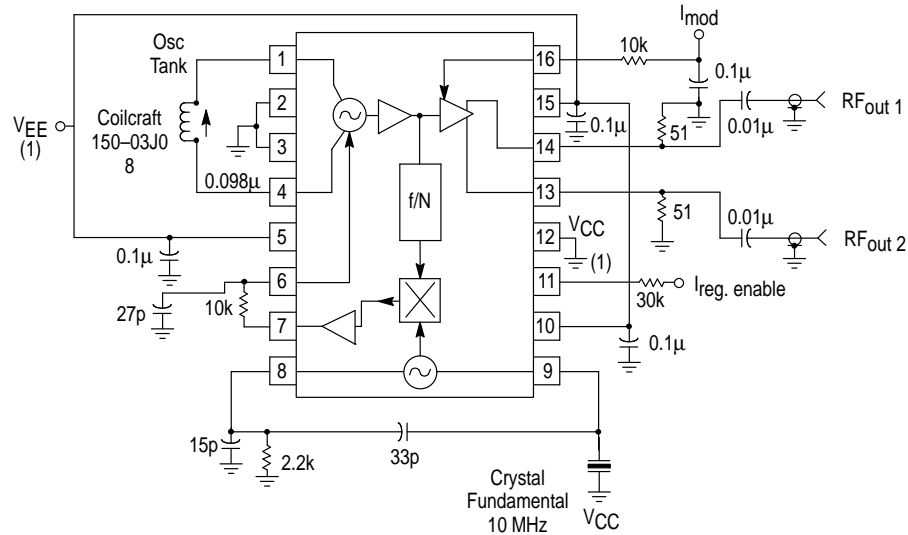
Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	7.0 (max)	Vdc
Operating Supply Voltage Range	$V_{CC}$	1.8 to 5.0	Vdc
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Operating Ambient Temperature	$T_A$	-40 to 85	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS** (Figure 2;  $V_{EE} = -3.0\text{ Vdc}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)\*

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Supply Current (Power down: $I_{11}$ & $I_{16} = 0$ )	—	$I_{EE1}$	-0.5	—	—	$\mu\text{A}$
Supply Current (Enable [Pin 11] to $V_{CC}$ thru 30 k, $I_{16} = 0$ )	—	$I_{EE2}$	-18	-14	—	mA
Total Supply Current (Transmit Mode) ( $I_{mod} = 2.0\text{ mA}$ ; $f_o = 320\text{ MHz}$ )	—	$I_{EE3}$	-39	-34	—	mA
Differential Output Power ( $f_o = 320\text{ MHz}$ ; $V_{ref}$ [Pin 9] = $500\text{ mV}_{p-p}$ ; $f_o = N \times f_{ref}$ ) $I_{mod} = 2.0\text{ mA}$ (see Figure 7) $I_{mod} = 0\text{ mA}$	13 & 14	$P_{out}$	2.0 —	4.7 -45	— —	dBm
Hold-in Range ( $\pm \Delta f_{ref} \times N$ ) (see Figure 7)	13 & 14	$\pm \Delta f_H$	4.0	8.0	—	MHz
Phase Detector Output Error Current	7	$I_{error}$	22	27	—	$\mu\text{A}$
Oscillator Enable Time (see Figure 26)	11 & 8	$t_{enable}$	—	4.0	—	ms
Amplitude Modulation Bandwidth (see Figure 28)	16	$BW_{AM}$	—	25	—	MHz
Spurious Outputs ( $I_{mod} = 2.0\text{ mA}$ ) Spurious Outputs ( $I_{mod} = 0\text{ mA}$ )	13 & 14 13 & 14	$P_{son}$ $P_{soff}$	— —	-50 -50	— —	dBc
Maximum Divider Input Frequency Maximum Output Frequency	— 13 & 14	$f_{div}$ $f_o$	— —	950 950	— —	MHz

\* For testing purposes,  $V_{CC}$  is ground (see Figure 2).

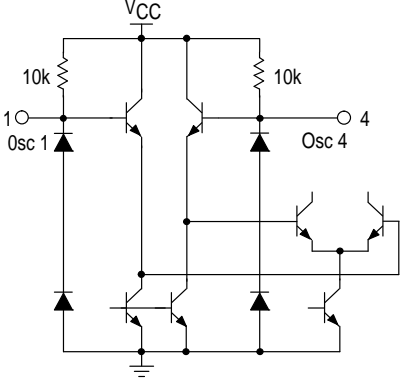
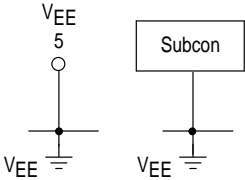
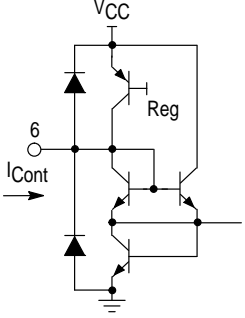
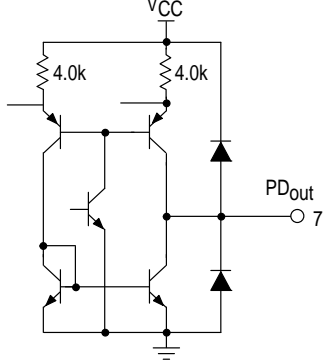
**Figure 2. 320 MHz Test Circuit**



**NOTES:** 1.  $V_{CC}$  is ground; while  $V_{EE}$  is negative with respect to ground.  
2. Pins 5, 10 and 15 are brought to the circuit side of the PCB via plated through holes.  
They are connected together with a trace on the PCB and each Pin is decoupled to  $V_{CC}$  (ground).

# MC13176

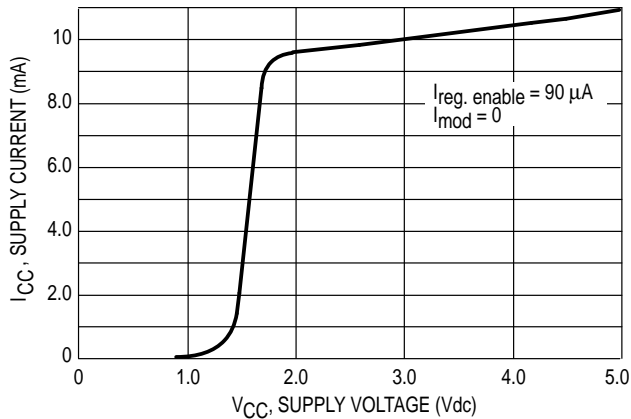
## PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
1 & 4	Osc 1, Osc 4		<b>CCO Inputs</b> The oscillator is a current controlled type. An external oscillator coil is connected to Pins 1 and 4 which forms a parallel resonance LC tank circuit with the internal capacitance of the IC and with parasitic capacitance of the PC board. Three base-emitter capacitances in series configuration form the capacitance for the parallel tank. These are the base-emitters at Pins 1 and 4 and the base-emitter of the differential amplifier. The equivalent series capacitance in the differential amplifier is varied by the modulating current from the frequency control circuit (see Pin 6, internal circuit). A more thorough discussion is found in the Applications Information section.
5	V <sub>EE</sub>		<b>Supply Ground (V<sub>EE</sub>)</b> In the PCB layout, the ground pins (also applies to Pins 10 and 15) should be connected directly to chassis ground. Decoupling capacitors to V <sub>CC</sub> should be placed directly at the ground returns.
6	I <sub>Cont</sub>		<b>Frequency Control</b> For V <sub>CC</sub> = 3.0 Vdc, the voltage at Pin 6 is approximately 1.55 Vdc. The oscillator is current controlled by the error current from the phase detector. This current is amplified to drive the current source in the oscillator section which controls the frequency of the oscillator. Figures 8 and 9 show the $\Delta f_{osc}$ versus I <sub>Cont</sub> . Figure 5 shows the $\Delta f_{osc}$ versus I <sub>Cont</sub> at -40°C, +25°C and +85°C for 320 MHz. The CCO may be FM modulated as shown in Figures 17 and 18, MC13176 320 MHz FM Transmitter. A detailed discussion is found in the Applications Information section.
7	PD <sub>out</sub>		<b>Phase Detector Output</b> The phase detector provides $\pm 30 \mu A$ to keep the CCO locked at the desired carrier frequency. The output impedance of the phase detector is approximately 53 k $\Omega$ . Under closed loop conditions there is a DC voltage which is dependent upon the free running oscillator and the reference oscillator frequencies. The circuitry between Pins 7 and 6 should be selected for adequate loop filtering necessary to stabilize and filter the loop response. Low pass filtering between Pin 7 and 6 is needed so that the corner frequency is well below the sum of the divider and the reference oscillator frequencies, but high enough to allow for fast response to keep the loop locked. Refer to the Applications Information section regarding loop filtering and FM modulation.

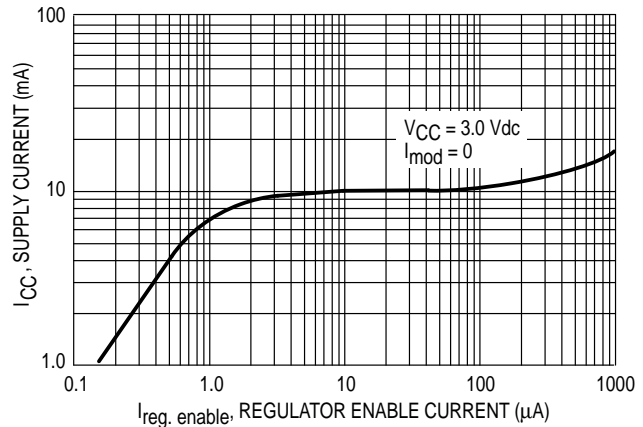
## PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
8	Xtale		<b>Crystal Oscillator Inputs</b> The internal reference oscillator is configured as a common emitter Colpitts. It may be operated with either a fundamental or overtone crystal depending on the carrier frequency and the internal prescaler. Crystal oscillator circuits and specifications of crystals are discussed in detail in the applications section. With $V_{CC} = 3.0$ Vdc, the voltage at Pin 8 is approximately 1.8 Vdc and at Pin 9 is approximately 2.3 Vdc. 500 to 1000 mVp-p should be present at Pin 9. The Colpitts is biased at 200 $\mu$ A; additional drive may be acquired by increasing the bias to approximately 500 $\mu$ A. Use 6.2 k from Pin 8 to ground.
9	Xtalb		
10	Reg. Gnd		<b>Regulator Ground</b> An additional ground pin is provided to enhance the stability of the system. Decoupling to the $V_{CC}$ (RF ground) is essential; it should be done at the ground return for Pin 10.
11	Enable		<b>Device Enable</b> The potential at Pin 11 is approximately 1.25 Vdc. When Pin 11 is open, the transmitter is disabled in a power down mode and draws less than 1.0 $\mu$ A $I_{CC}$ if the MOD at Pin 16 is also open (i.e., it has no current driving it). To enable the transmitter a current source of 10 $\mu$ A to 90 $\mu$ A is provided. Figures 3 and 4 show the relationship between $I_{CC}$ , $V_{CC}$ and $I_{reg. enable}$ . Note that $I_{CC}$ is flat at approximately 10 mA for $I_{reg. enable} = 5.0$ to 100 $\mu$ A ( $I_{mod} = 0$ ).
12	$V_{CC}$		<b>Supply Voltage (<math>V_{CC}</math>)</b> The operating supply voltage range is from 1.8 Vdc to 5.0 Vdc. In the PCB layout, the $V_{CC}$ trace must be kept as wide as possible to minimize inductive reactances along the trace; it is best to have it completely fill around the surface mount components and traces on the circuit side of the PCB.
13 & 14	Out 1 and Out 2		<b>Differential Output</b> The output is configured differentially to easily drive a loop antenna. By using a transformer or balun, as shown in the application schematic, the device may then drive an unbalanced low impedance load. Figure 6 shows how much the Output Power and Free-Running Oscillator Frequency change with temperature at 3.0 Vdc; $I_{mod} = 2.0$ mA.
15	Out_Gnd		<b>Output Ground</b> This additional ground pin provides direct access for the output ground to the circuit board $V_{EE}$ .
16	$I_{mod}$		<b>AM Modulation/Power Output Level</b> The DC voltage at this pin is 0.8 Vdc with the current source active. An external resistor is chosen to provide a source current of 1.0 to 3.0 mA, depending on the desired output power level at a given $V_{CC}$ . Figure 27 shows the relationship of Power Output to Modulation Current, $I_{mod}$ . At $V_{CC} = 3.0$ Vdc, 3.5 dBm power output can be acquired with about 35 mA $I_{CC}$ . For FM modulation, Pin 16 is used to set the desired output power level as described above. For AM modulation, the modulation signal must ride on a positive DC bias offset which sets a static (modulation off) modulation current. External circuitry for various schemes is further discussed in the Applications Information section.

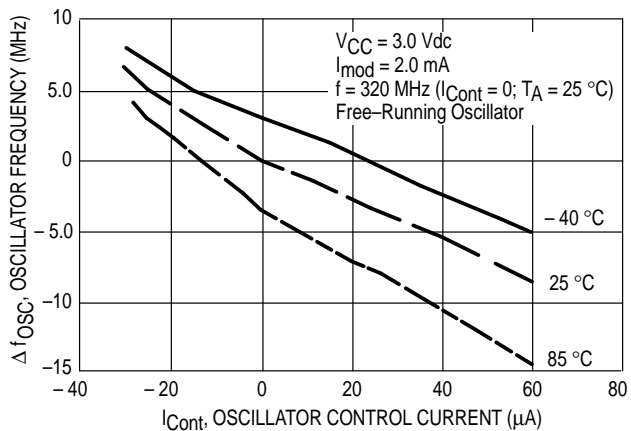
**Figure 3. Supply Current versus Supply Voltage**



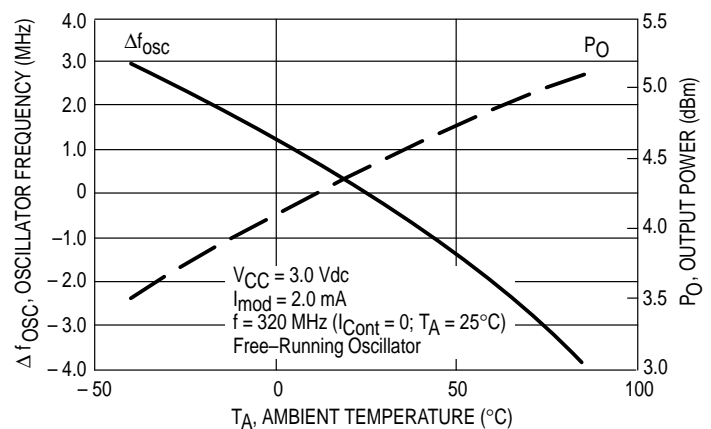
**Figure 4. Supply Current versus Regulator Enable Current**



**Figure 5. Change Oscillator Frequency versus Oscillator Control Current**



**Figure 6. Change in Oscillator Frequency and Output Power versus Ambient Temperature**



**Figure 7. Reference Oscillator Frequency versus Phase Detector Current**

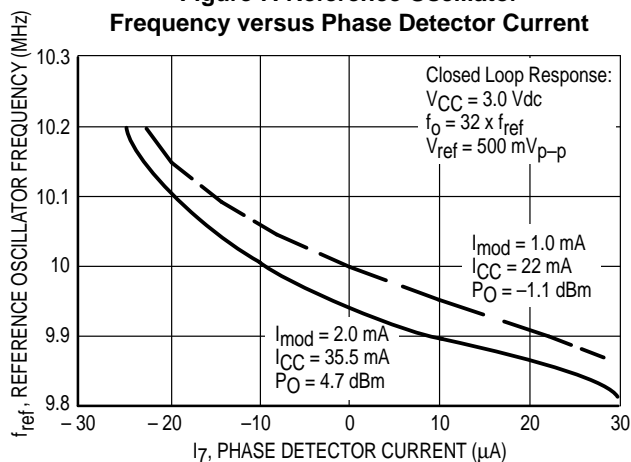


Figure 8. Change in Oscillator Frequency versus Oscillator Control Current

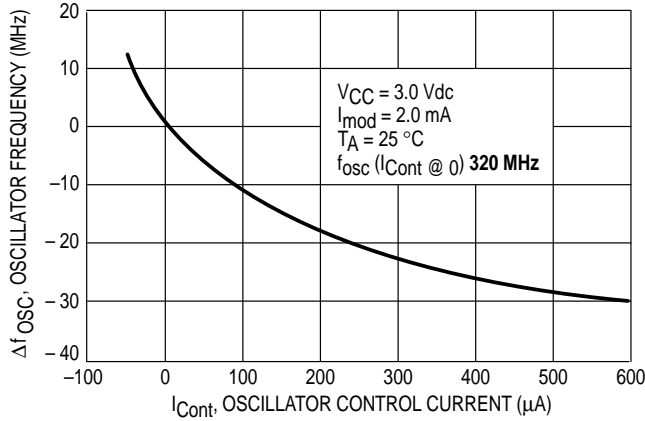
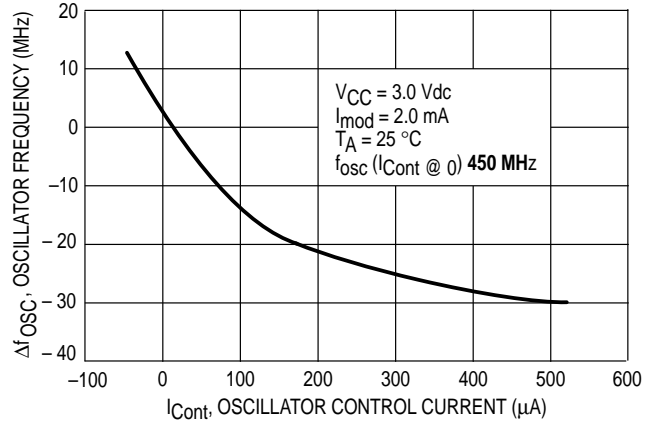


Figure 9. Change in Oscillator Frequency versus Oscillator Control Current



## APPLICATIONS INFORMATION

## Evaluation PC Board

The evaluation PCB, shown in Figures 32 and 33, is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side of the PCB (see Figures 34 and 35). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

## Current Controlled Oscillator (Pins 1 to 4)

It is critical to keep the interconnect leads from the CCO (Pins 1 and 4) to the external inductor symmetrical and equal in length. With a minimum inductor, the maximum free running frequency is greater than 1.0 GHz. Since this inductor will be small, it may be either a microstrip inductor, an air wound inductor or a tuneable RF coil. An air wound inductor may be tuned by spreading the windings, whereas tuneable RF coils are tuned by adjusting the position of an aluminum core in a threaded coilform. As the aluminum core coupling to the windings is increased, the inductance is decreased. The temperature coefficient using an aluminum core is better than a ferrite core. The UniCoil™ inductors made by Coilcraft may be obtained with aluminum cores (Part No. 51-129-169).

## Ground (Pins 5, 10 and 15)

**Ground Returns:** It is best to take the grounds to a backside ground plane via plated through holes or eyelets at the pins. The application PCB layout implements this technique. Note that the grounds are located at or less than 100 mils from the devices pins.

**Decoupling:** Decoupling each ground pin to  $V_{CC}$  isolates each section of the device by reducing interaction between sections and by localizing circulating currents.

## Loop Characteristics (Pins 6 and 7)

Figure 10 is the component block diagram of the MC13176D PLL system where the loop characteristics are described by the gain constants. Access to individual components of this PLL system is limited, inasmuch as the loop is only pinned out at the phase detector output and the

frequency control input for the CCO. However, this allows for characterization of the gain constants of these loop components. The gain constants  $K_p$ ,  $K_o$  and  $K_n$  are well defined in the MC13176.

## Phase Detector (Pin 7)

With the loop in lock, the difference frequency output of the phase detector is DC voltage that is a function of the phase difference. The sinusoidal type detector used in this IC has the following transfer characteristic:

$$I_e = A \sin \theta_e$$

The gain factor of the phase detector,  $K_p$  (with the loop in lock) is specified as the ratio of DC output current,  $I_e$  to phase error,  $\theta_e$ :

$$K_p = I_e / \theta_e \text{ (Amps/radians)}$$

$$K_p = A \sin \theta_e / \theta_e$$

$$\sin \theta_e \sim \theta_e \text{ for } \theta_e \leq 0.2 \text{ radians;}$$

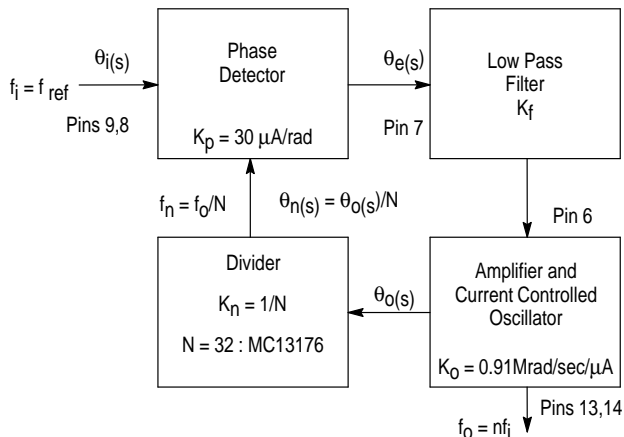
$$\text{thus, } K_p = A \text{ (Amps/radians)}$$

Figure 7 shows that the detector DC current is approximately 30  $\mu A$  where the loop loses lock at  $\theta_e = \pm \pi/2$  radians; therefore,  $K_p$  is 30  $\mu A$ /radians.

## Current Controlled Oscillator, CCO (Pin 6)

Figures 8 and 9 show the non-linear change in frequency of the oscillator over an extended range of control current for 320 and 450 MHz applications.  $K_o$  ranges from approximately  $6.3 \times 10^5$  rad/sec/ $\mu A$  or 100 kHz/ $\mu A$  (Figure 8) to  $8.8 \times 10^5$  rad/sec/ $\mu A$  or 140 kHz/ $\mu A$  (Figure 9) over a relatively linear response of control current (0 to 100  $\mu A$ ). The oscillator gain factor depends on the operating range of the control current (i.e., the slope is not constant). Included in the CCO gain factor is the internal amplifier which can sink and source at least 30  $\mu A$  of input current from the phase detector. The internal circuitry at Pin 6 limits the CCO control current to 50  $\mu A$  of source capability while its sink capability exceeds 200  $\mu A$  as shown in Figures 8 and 9. Further information to follow shows how to use the full capabilities of the CCO by addition of an external loop amplifier and filter (see Figure 14). This additional circuitry yields at  $K_o = 0.145$  MHz/ $\mu A$  or  $9.1 \times 10^5$  rad/sec/ $\mu A$ .

Figure 10. Block Diagram of MC1317XD PLL



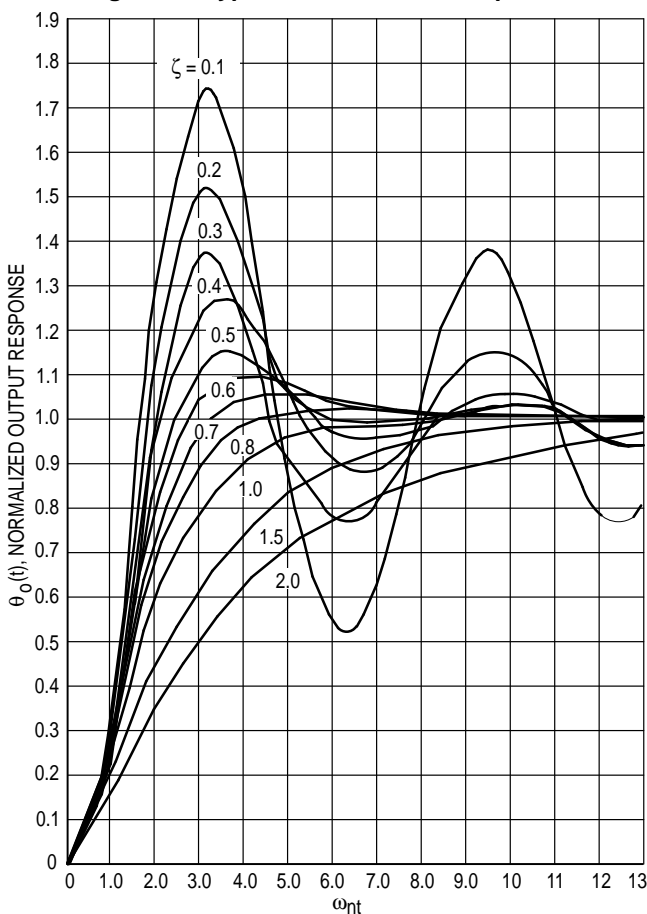
Where:  $K_p$  = Phase detector gain constant in  $\mu\text{A/rad}$ ;  $K_p = 30 \mu\text{A/rad}$   
 $K_f$  = Filter transfer function  
 $K_n = 1/N$ ;  $N = 32$   
 $K_o$  = CCO gain constant in  $\text{rad/sec}/\mu\text{A}$   
 $K_o = 9.1 \times 10^5 \text{ rad/sec}/\mu\text{A}$

### Loop Filtering

The fundamental loop characteristics, such as capture range, loop bandwidth, lock-up time and transient response are controlled externally by loop filtering.

The natural frequency ( $\omega_n$ ) and damping factor ( $\partial$ ) are important in the transient response to a step input of phase or frequency. For a given  $\partial$  and lock time,  $\omega_n$  can be determined from the plot shown in Figure 11.

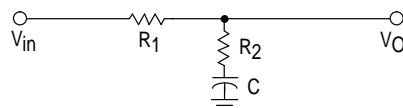
Figure 11. Type 2 Second Order Response



For  $\partial = 0.707$  and lock time = 1.0 ms;  
then  $\omega_n = 5.0/t = 5.0 \text{ krad/sec}$ .

The loop filter may take the form of a simple low pass filter or a lag-lead filter which creates an additional pole at origin in the loop transfer function. This additional pole along with that of the CCO provides two pure integrators ( $1/s^2$ ). In the lag-lead low pass network shown in Figure 12, the values of the low pass filtering parameters  $R_1$ ,  $R_2$  and  $C$  determine the loop constants  $\omega_n$  and  $\partial$ . The equations  $t_1 = R_1C$  and  $t_2 = R_2C$  are related in the loop filter transfer functions  $F(s) = 1 + t_2s/1 + (t_1 + t_2)s$ .

Figure 12. Lag-Lead Low Pass Filter



The closed loop transfer function takes the form of a 2nd order low pass filter given by,

$$H(s) = K_V F(s)/s + K_V F(s)$$

From control theory, if the loop filter characteristic has  $F(0) = 1$ , the DC gain of the closed loop,  $K_V$  is defined as,

$$K_V = K_p K_o K_n$$

and the transfer function has a natural frequency,

$$\omega_n = (K_V/t_1 + t_2)^{1/2}$$

and a damping factor,

$$\partial = (\omega_n/2) (t_2 + 1/K_V)$$

Rewriting the above equations and solving for the MC13176 with  $\partial = 0.707$  and  $\omega_n = 5.0 \text{ k rad/sec}$ :

$$K_V = K_p K_o K_n = (30) (0.91 \times 10^6) (1/32) = 0.853 \times 10^6$$

$$t_1 + t_2 = K_V/\omega_n^2 = 0.853 \times 10^6/(25 \times 10^6) = 34.1 \text{ ms}$$

$$t_2 = 2\partial/\omega_n = (2) (0.707)/(5 \times 10^3) = 0.283 \text{ ms}$$

$$t_1 = (K_V/\omega_n^2) - t_2 = (34.1 - 0.283) = 33.8 \text{ ms}$$



For  $C = 0.47 \mu$ ;

then,  $R_1 = t_1/C = 33.8 \times 10^{-3}/0.47 \times 10^{-6} = 72 \text{ k}$

thus,  $R_2 = t_2/C = 0.283 \times 10^{-3}/0.47 \times 10^{-6} = 0.60 \text{ k}$

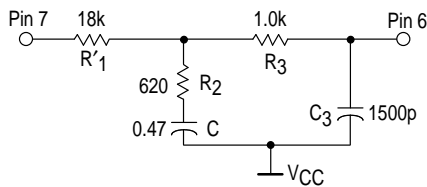
In the above example, the following standard value components are used,

$C = 0.47 \mu$ ;  $R_2 = 620$  and  $R'_1 = 72 \text{ k} - 53 \text{ k} \sim 18 \text{ k}$

( $R'_1$  is defined as  $R_1 - 53 \text{ k}$ , the output impedance of the phase detector.)

Since the output of the phase detector is high impedance ( $\sim 50 \text{ k}$ ) and serves as a current source, and the input to the frequency control, Pin 6 is low impedance (impedance of the two diode to ground is approximately  $500 \Omega$ ), it is imperative that the second order low pass filter design above be modified. In order to minimize loading of the  $R_2C$  shunt network, a higher impedance must be established to Pin 6. A simple solution is achieved by adding a low pass network between the passive second order network and the input to Pin 6. This helps to minimize the loading effects on the second order low pass while further suppressing the sideband spurs of the crystal oscillator. A low pass filter with  $R_3 = 1.0 \text{ k}$  and  $C_2 = 1500 \text{ p}$  has a corner frequency ( $f_c$ ) of  $106 \text{ kHz}$ ; the reference sideband spurs are down greater than  $-60 \text{ dBc}$ .

Figure 13. Modified Low Pass Loop Filter



#### Hold-In Range

The hold-in range, also called the lock range, tracking range and synchronization range, is the ability of the CCO frequency,  $f_o$  to track the input reference signal,  $f_{ref} \cdot N$  as it gradually shifted away from the free running frequency,  $f_f$ . Assuming that the CCO is capable of sufficient frequency deviation and that the internal loop amplifier and filter are not overdriven, the CCO will track until the phase error,  $\theta_e$  approaches  $\pm\pi/2$  radians. Figures 5 through 7 are a direct

measurement of the hold-in range (i.e.  $\Delta f_{ref} \times N = \pm \Delta f_H \times 2\pi$ ). Since  $\sin \theta_e$  cannot exceed  $\pm 1.0$ , as  $\theta_e$  approaches  $\pm\pi/2$  the hold-in range is equal to the DC loop gain,  $K_V \times N$ .

$$\pm \Delta \omega_H = \pm K_V \times N$$

where,  $K_V = K_P K_O K_N$ .

In the above example,

$$\pm \Delta \omega_H = \pm 27.3 \text{ Mrad/sec}$$

$$\pm \Delta f_H = \pm 4.35 \text{ MHz}$$

#### Extended Hold-in Range

The hold-in range of about 3.4% could cause problems over temperature in cases where the free-running oscillator drifts more than 2 to 3% because of relatively high temperature coefficients of the ferrite tuned CCO inductor. This problem might worsen for lower frequency applications where the external tuning coil is large compared to internal capacitance at Pins 1 and 4. To improve hold-in range performance, it is apparent that the gain factors involved must be carefully considered.

$K_N$  = is  $1/32$  in the MC13176.

$K_P$  = is fixed internally and cannot be altered.

$K_O$  = Figures 8 and 9 suggest that there is capability of greater control range with more current swing. However, this swing must be symmetrical about the center of the dynamic response. The suggested zero current operating point for  $\pm 100 \mu\text{A}$  swing of the CCO is at about  $+70 \mu\text{A}$  offset point.

$K_a$  = External loop amplification will be necessary since the phase detector only supplies  $\pm 30 \mu\text{A}$ .

In the design example in Figure 14, an external resistor ( $R_5$ ) of  $15 \text{ k}$  to  $V_{CC}$  ( $3.0 \text{ Vdc}$ ) provides approximately  $100 \mu\text{A}$  of current boost to supplement the existing  $50 \mu\text{A}$  internal source current.  $R_4$  ( $1.0 \text{ k}$ ) is selected for approximately  $0.1 \text{ Vdc}$  across it with  $100 \mu\text{A}$ .  $R_1$ ,  $R_2$  and  $R_3$  are selected to set the potential at Pin 7 and the base of 2N4402 at approximately  $0.9 \text{ Vdc}$  and the emitter at  $1.55 \text{ Vdc}$  when error current to Pin 6 is approximately zero  $\mu\text{A}$ .  $C_1$  is chosen to reduce the level of the crystal sidebands.

Figure 14. External Loop Amplifier

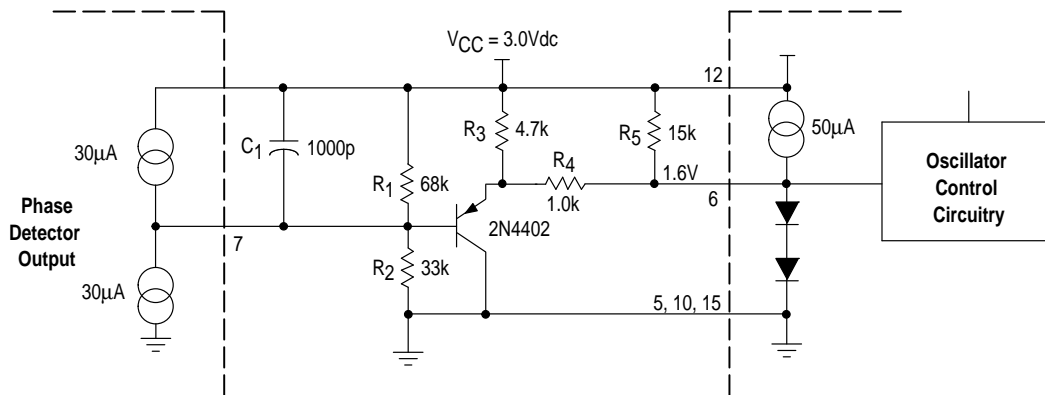
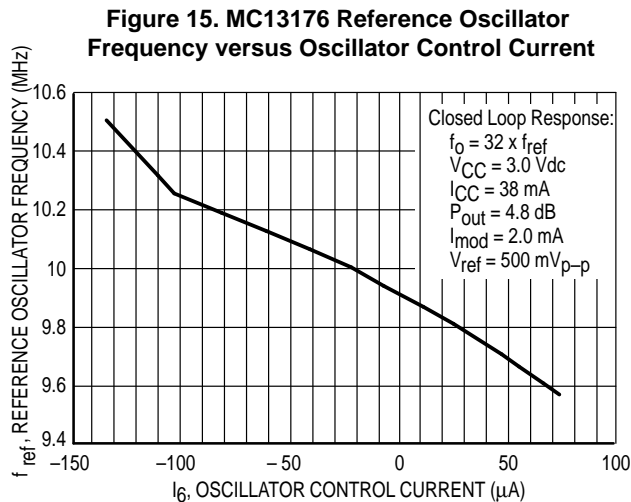




Figure 15 shows the improved hold-in range of the loop. The  $\Delta f_{\text{ref}}$  is moved 950 kHz with over 200  $\mu\text{A}$  swing of control current for an improved hold-in range of  $\pm 15.2 \text{ MHz}$  or  $\pm 95.46 \text{ Mrad/sec}$ .



### Lock-in Range/Capture Range

If a signal is applied to the loop not equal to free running frequency,  $f_f$ , then the loop will capture or lock-in the signal by making  $f_s = f_o$  (i.e. if the initial frequency difference is not too great). The lock-in range can be expressed as  $\Delta\omega_L \sim \pm 2\partial\omega_n$

### FM Modulation

Noise external to the loop (phase detector input) is minimized by narrowing the bandwidth. This noise is minimal in a PLL system since the reference frequency is usually derived from a crystal oscillator. FM can be achieved by applying a modulation current superimposed on the control current of the CCO. The loop bandwidth must be narrow enough to prevent the loop from responding to the modulation frequency components, thus, allowing the CCO to deviate in frequency. The loop bandwidth is related to the natural frequency  $\omega_n$ . In the lag-lead design example where the natural frequency,  $\omega_n = 5.0 \text{ krad/sec}$  and a damping factor,  $\partial = 0.707$ , the loop bandwidth =  $1.64 \text{ kHz}$ . Characterization data of the closed loop responses at 320 MHz (Figure 7) show satisfactory performance using only a simple low-pass loop filter network. The loop filter response is strongly influenced by the high output impedance of the phase detector.

$$f_c = 0.159/RC;$$

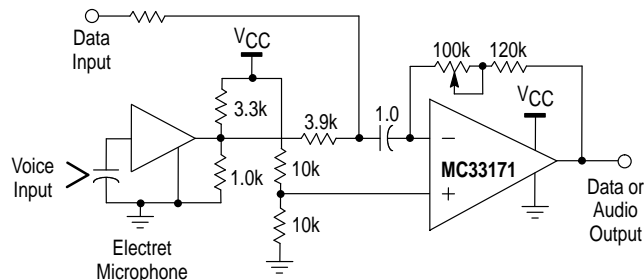
For  $R = 1.0 \text{ k} + R_7$  ( $R_7 = 53 \text{ k}$ ) and  $C = 390 \text{ pF}$

$$f_c = 7.55 \text{ kHz or } \omega_c = 47 \text{ krad/sec}$$

The application example in Figure 17 of a 320 MHz FM transmitter demonstrates the FM capabilities of the IC. A high value series resistor (100 k) to Pin 6 sets up the current source to drive the modulation section of the chip. Its value is dependent on the peak to peak level of the encoding data and the maximum desired frequency deviation. The data input is AC coupled with a large coupling capacitor which is selected for the modulating frequency. The component placements on the circuit side and ground side of the PC board are shown in Figures 34 and 35, respectively. Figure 19 illustrates the input data of a 10 kHz modulating signal at 1.6 Vp-p. Figures 20 and 21 depict the deviation and resulting modulation spectrum showing the carrier null at  $-40 \text{ dBc}$ . Figure 22 shows the unmodulated carrier power output at 3.5 dBm for  $V_{\text{CC}} = 3.0 \text{ Vdc}$ .

For voice applications using a dynamic or an electret microphone, an op amp is used to amplify the microphone's low level output. The microphone amplifier circuit is shown in Figure 16. Figure 18 shows an application example for NBFM audio or direct FSK in which the reference crystal oscillator is modulated.

**Figure 16. Microphone Amplifier**

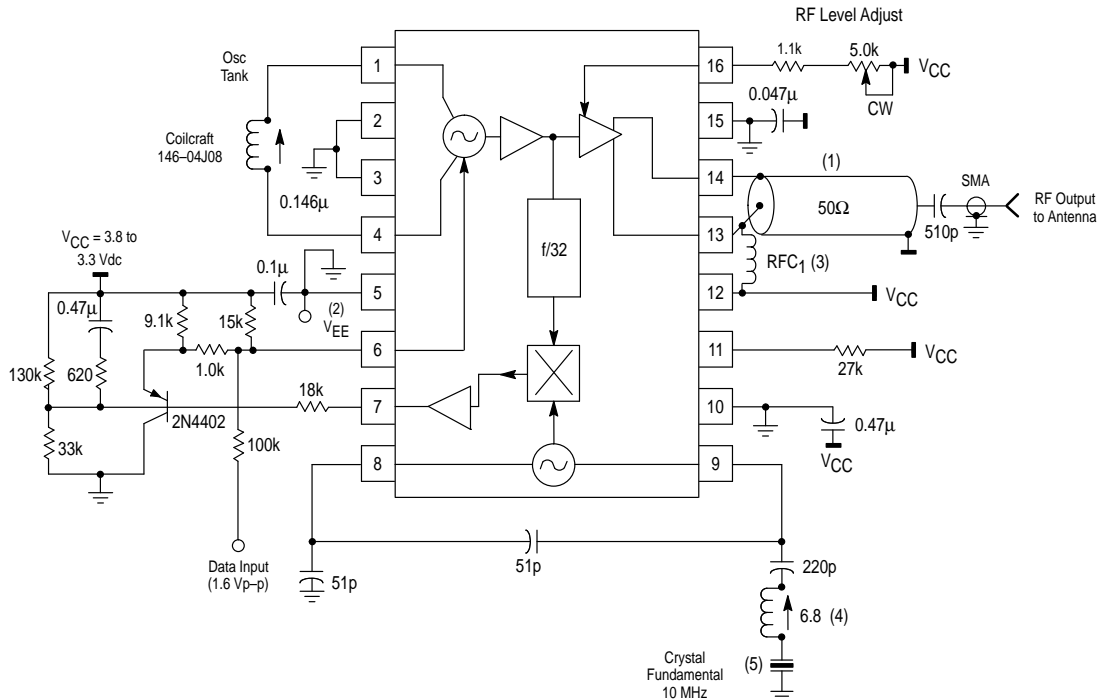


### Local Oscillator Application

To reduce internal loop noise, a relatively wide loop bandwidth is needed so that the loop tracks out or cancels the noise. This is emphasized to reduce inherent CCO and divider noise or noise produced by mechanical shock and environmental vibrations. In a local oscillator application the CCO and divider noise should be reduced by proper selection of the natural frequency of the loop. Additional low pass filtering of the output will likely be necessary to reduce the crystal sideband spurs to a minimal level.

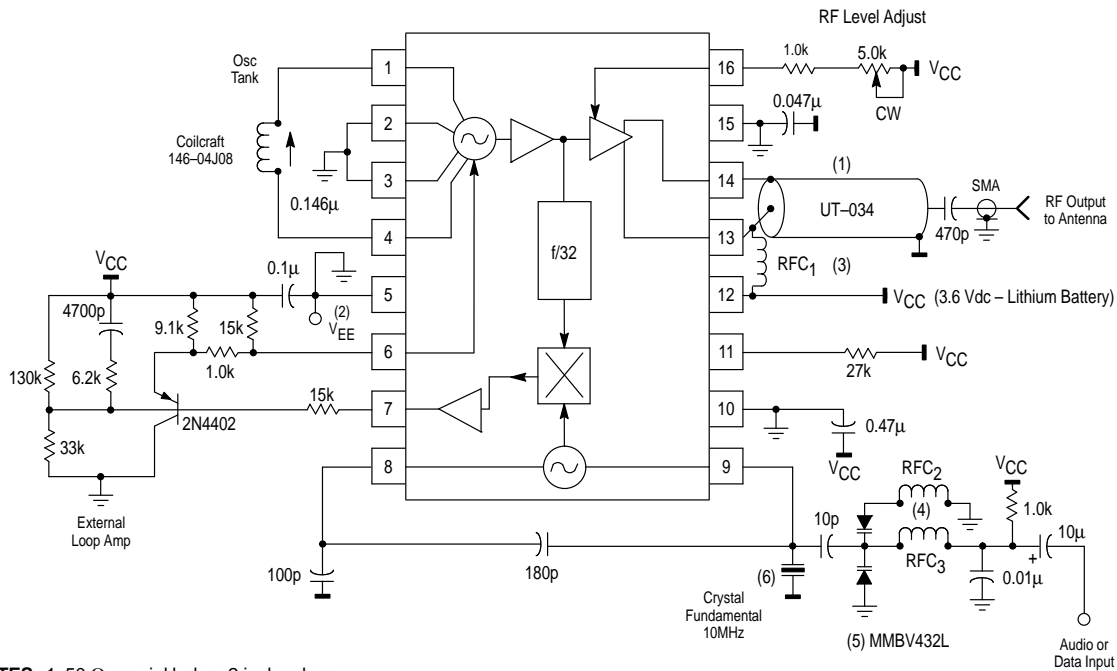
## MC13176

Figure 17. 320 MHz MC13176D FM Transmitter



- NOTES:**
1. 50  $\Omega$  coaxial balun, 2 inches long.
  2. Pins 5, 10 and 15 are grounds and connected to  $V_{EE}$  which is the component's side ground plane. These pins must be decoupled to  $V_{CC}$ ; decoupling capacitors should be placed as close as possible to the pins.
  3. RFC<sub>1</sub> is 180 nH Coilcraft surface mount inductor or 190 nH Coilcraft 146-05J08.
  4. Recommended source is a Coilcraft "slot seven" 7.0 mm tuneable inductor, part #7M3-682.
  5. The crystal is a parallel resonant, fundamental mode calibrated with 32 pF load capacitance.

Figure 18. 320 MHz NBFM Transmitter



- NOTES:**
1. 50  $\Omega$  coaxial balun, 2 inches long.
  2. Pins 5, 10 and 15 are grounds and connected to  $V_{EE}$  which is the component's side ground plane. These pins must be decoupled to  $V_{CC}$ ; decoupling capacitors should be placed as close as possible to the pins.
  3. RFC<sub>1</sub> is 180 nH Coilcraft surface mount inductor.
  4. RFC<sub>2</sub> and RFC<sub>3</sub> are high impedance crystal frequency of 10 MHz; 8.2  $\mu$ H molded inductor gives  $X_L > 1000 \Omega$ .
  5. A single varactor like the MV2105 may be used whereby RFC<sub>2</sub> is not needed.
  6. The crystal is a parallel resonant, fundamental mode calibrated with 32 pF load capacitance.

Figure 19. Input Data Waveform

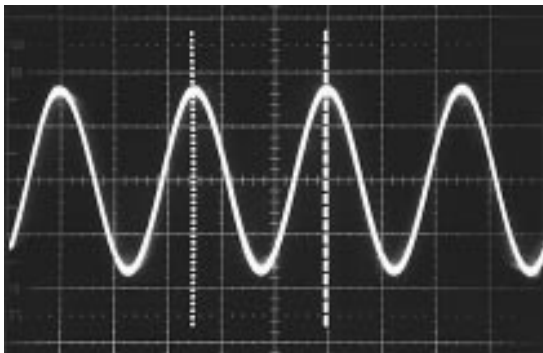


Figure 20. Frequency Deviation



Figure 21. Modulation Spectrum

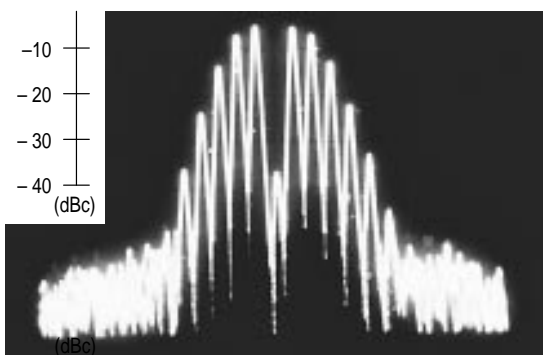


Figure 22. Unmodulated Carrier



### Reference Crystal Oscillator (Pins 8 and 9)

**Selection of Proper Crystal:** A crystal can operate in a number of mechanical modes. The lowest resonant frequency mode is its fundamental while higher order modes are called overtones. At each mechanical resonance, a crystal behaves like a RLC series-tuned circuit having a large inductor and a high Q. The inductor  $L_S$  is series resonance with a dynamic capacitor,  $C_S$  determined by the elasticity of the crystal lattice and a series resistance  $R_S$ , which accounts for the power dissipated in heating the crystal. This series RLC circuit is in parallel with a static capacitance,  $C_P$  which is created by the crystal block and by the metal plates and leads that make contact with it.

Figure 23 is the equivalent circuit for a crystal in a single resonant mode. It is assumed that other modes of resonance are so far off frequency that their effects are negligible.

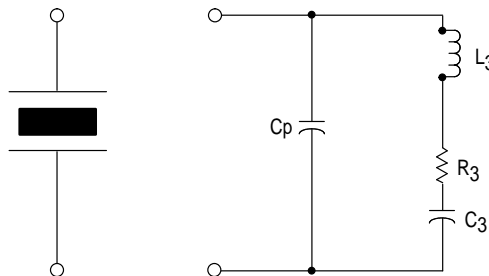
Series resonant frequency,  $f_S$  is given by;

$$f_S = 1/2\pi(L_S C_S)^{1/2}$$

and parallel resonant frequency,  $f_P$  is given by;

$$f_P = f_S(1 + C_S/C_P)^{1/2}$$

Figure 23. Crystal Equivalent Circuit



the frequency separation at resonance is given by;

$$\Delta f = f_P - f_S = f_S[1 - (1 + C_S/C_P)^{-1/2}]$$

Usually  $f_P$  is less than 1% higher than  $f_S$ , and a crystal exhibits an extremely wide variation of the reactance with frequency between  $f_P$  and  $f_S$ . A crystal oscillator circuit is very stable with frequency. This high rate of change of impedance with frequency stabilizes the oscillator, because any significant change in oscillator frequency will cause a large phase shift in the feedback loop keeping the oscillator on frequency.

Manufacturers specify crystal for either series or parallel resonant operation. The frequency for the parallel mode is calibrated with a specified shunt capacitance called a “load capacitance.” The most common value is 30 to 32 pF. If the load capacitance is placed in series with the crystal, the equivalent circuit will be series resonance at the specified parallel-resonant frequency. Frequencies up to 20 MHz use parallel resonant crystal operating in the fundamental mode, while above 20 MHz to about 60 MHz, a series resonant crystal specified and calibrated for operation in the overtone mode is used.

#### Application Examples

Two types of crystal oscillator circuits are used in the applications circuits: 1) fundamental mode common emitter Colpitts (Figures 1, 17, 18, and 24), and 2) third overtone impedance inversion Colpitts (also Figures 1 and 24).

The fundamental mode common emitter Colpitts uses a parallel resonant crystal calibrated with a 32 pF load capacitance. The capacitance values are chosen to provide excellent frequency stability and output power of > 500 mVp-p at Pin 9. In Figures 1 and 24, the fundamental mode reference oscillator is fixed tuned relying on the repeatability of the crystal and passive network to maintain the frequency, while in the circuit shown in Figures 17 and 18, the oscillator frequency can be adjusted with the variable inductor for the precise operating frequency.

The reference oscillator can be operated as high as 60 MHz with a third overtone crystal. Therefore, it is possible to use the MC13176 up to 950 MHz (based on the maximum capability of the divider network).

#### Enable (Pin 11)

The enabling resistor at Pin 11 is calculated by:

$$R_{\text{reg. enable}} = V_{CC} - 1.0 \text{ Vdc} / I_{\text{reg. enable}}$$

From Figure 4,  $I_{\text{reg. enable}}$  is chosen to be 75  $\mu\text{A}$ . So, for a  $V_{CC} = 3.0 \text{ Vdc}$   $R_{\text{reg. enable}} = 26.6 \text{ k}\Omega$ , a standard value 27 k $\Omega$  resistor is adequate.

#### Layout Considerations

**Supply (Pin 12):** In the PCB layout, the  $V_{CC}$  trace must be kept as wide as possible to minimize inductive reactance

along the trace; it is best that  $V_{CC}$  (RF ground) completely fills around the surface mounted components and interconnect traces on the circuit side of the board. This technique is demonstrated in the evaluation PC board.

#### Battery/Selection/Lithium Types

The device may be operated from a 3.0 V lithium battery. Selection of a suitable battery is important. Because one of the major problems for long life battery powered equipment is oxidation of the battery terminals, a battery mounted in a clip-in socket is not advised. The battery leads or contact post should be isolated from the air to eliminate oxide build-up. The battery should have PC board mounting tabs which can be soldered to the PCB. Consideration should be given for the peak current capability of the battery. Lithium batteries have current handling capabilities based on the composition of the lithium compound, construction and the battery size. A 1300 mA/hr rating can be achieved in the cylindrical cell battery. The Rayovac CR2/3A lithium-manganese dioxide battery is a crimp sealed, spiral wound 3.0 Vdc, 1300 mA/hr cylindrical cell with PC board mounting tabs. It is an excellent choice based on capacity and size (1.358" long by 0.665" in diameter).

#### Differential Output (Pins 13, 14)

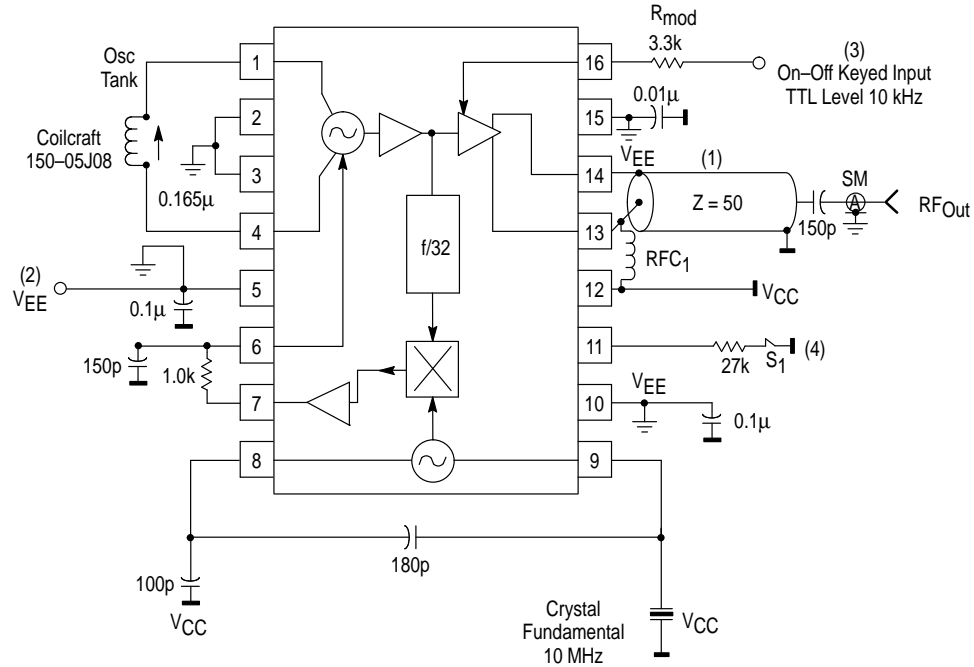
The availability of micro-coaxial cable and small baluns in surface mount and radial-leaded components allows for simple interface to the output ports. A loop antenna may be directly connected with bias via RFC or 50  $\Omega$  resistors. Antenna configuration will vary depending on the space available and the frequency of operation.

#### AM Modulation (Pin 16)

**Amplitude Shift Key:** The MC13176 is designed to accommodate Amplitude Shift Keying (ASK). ASK modulation is a form of digital modulation corresponding to AM. The amplitude of the carrier is switched between two or more values in response to the PCM code. For the binary case, the usual choice is On-Off Keying (often abbreviated OOK). The resultant amplitude modulated waveform consists of RF pulses called marks, representing binary 1 and spaces representing binary 0.

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Figure 24. ASK 320 MHz Application Circuit



- NOTES:**
1. 50  $\Omega$  coaxial balun, 1/10 wavelength line (1.5") provides the best match to a 50  $\Omega$  load.
  2. Pins 5, 10 and 15 are ground and connected to  $V_{EE}$  which is the component/DC ground plane side of PCB. These pins must be decoupled to  $V_{CC}$ ; decoupling capacitors should be placed as close as possible to the pins.

3. The On-Off keyed signal turns the output of the transmitter off and on with TTL level pulses through  $R_{mod}$  at Pin 16. The "On" power and  $I_{CC}$  is set by the resistor which sets  $I_{mod} = V_{TTL} - 0.8 / R_{mod}$ . (see Figure 27).
4. S1 simulates an enable gate pulse from a microprocessor which will enable the transmitter. (see Figure 4 to determine precise value of the enabling resistor based on the potential of the gate pulse and the desired enable.)

Figure 24 shows a typical application in which the output power has been reduced for linearity and current drain. The current draw on the device is 16 mA  $I_{CC}$  (average) and -22.5 dBm (average power output) using a 10 kHz modulating rate for the on-off keying. This equates to 20 mA and -2.3 dBm "On", 13 mA and -41 dBm "Off". In Figure 25, the device's modulating waveform and encoded carrier are

displayed. The crystal oscillator enable time is needed to set the acquisition timing. It takes typically 4.0 msec to reach full magnitude of the oscillator waveform (see Figure 26, Oscillator Waveform, at Pin 8). A square waveform of 3.0 V peak with a period that is greater than the oscillator enable time is applied to the Enable (Pin 11).

Figure 25. ASK Input Waveform and Modulated Carrier

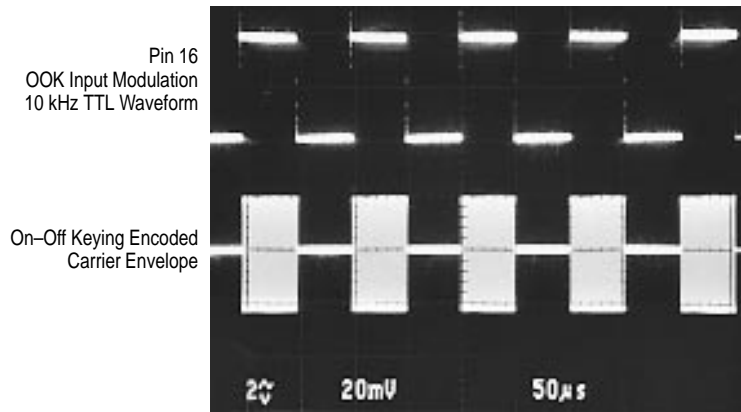
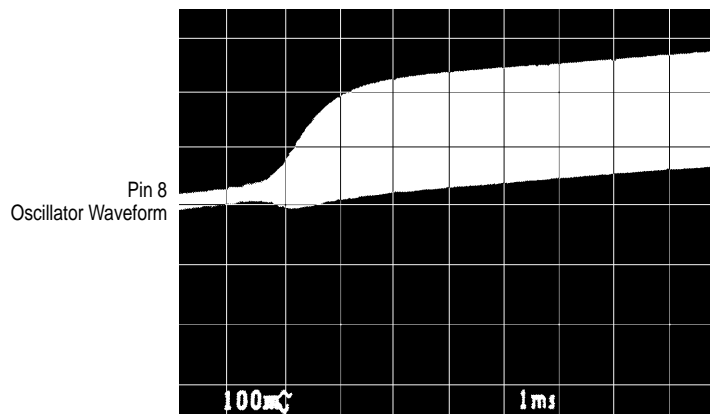
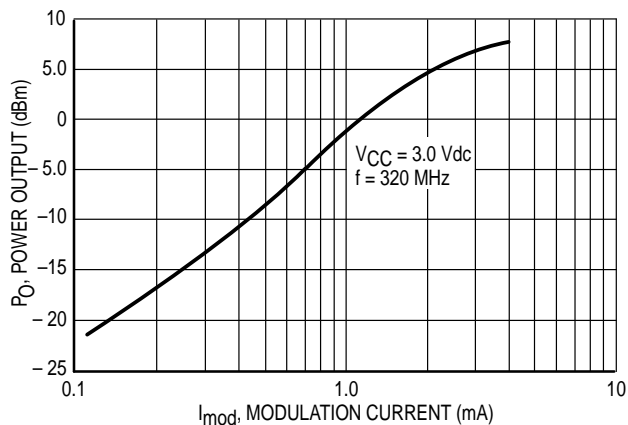
Figure 26. Oscillator Enable Time,  $T_{enable}$ 

Figure 27. Power Output versus Modulation Current



### Analog AM

In analog AM applications, the output amplifier's linearity must be carefully considered. Figure 27 is a plot of Power Output versus Modulation Current at 320 MHz, 3.0 Vdc. In order to achieve a linear encoding of the modulating sinusoidal waveform on the carrier, the modulating signal must amplitude modulate the carrier in the linear portion of its power output response. When using a sinewave modulating signal, the signal rides on a positive DC offset called  $V_{mod}$  which sets a static (modulation off) modulation current,  $I_{mod}$ .  $I_{mod}$  controls the power output of the IC. As the modulating signal moves around this static bias point the modulating current varies causing power output to vary or to be AM modulated. When the IC is operated at modulation current levels greater than 2.0 mA the differential output stage starts to saturate.



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In the design example, shown in Figure 28, the operating point is selected as a tradeoff between average power output and quality of the AM.

For  $V_{CC} = 3.0 \text{ Vdc}$ ;  $I_{CC} = 18.5 \text{ mA}$  and  $I_{mod} = 0.5 \text{ mAdc}$  and a static DC offset of  $1.04 \text{ Vdc}$ , the circuit shown in Figure 28 completes the design. Figures 29, 30 and 31 show the results of  $-6.9 \text{ dBm}$  output power and 100% modulation by the  $10 \text{ kHz}$  and  $1.0 \text{ MHz}$  modulating sinewave signals. The amplitude of the input signals is approximately  $800 \text{ mVp-p}$ .

Where  $R_{mod} = (V_{CC} - 1.04 \text{ Vdc}) / 0.5 \text{ mA} = 3.92 \text{ k}$ , use a standard value resistor of  $3.9 \text{ k}$ .

Figure 28. Analog AM Transmitter

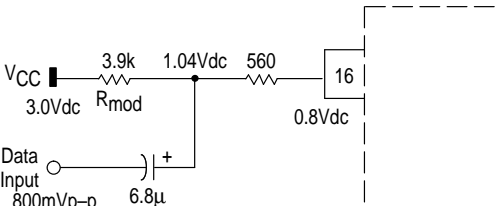


Figure 29. Power Output of Unmodulated Carrier

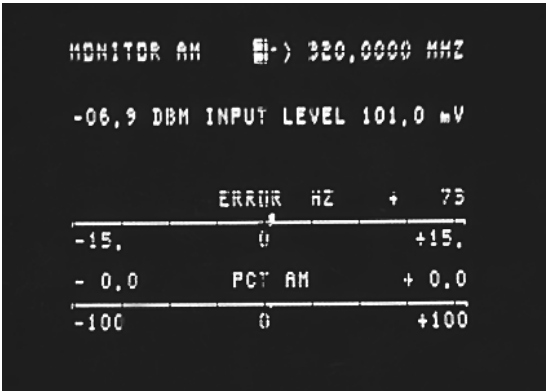


Figure 30. Input Signal and AM Modulated Carrier for  $f_{mod} = 10 \text{ kHz}$

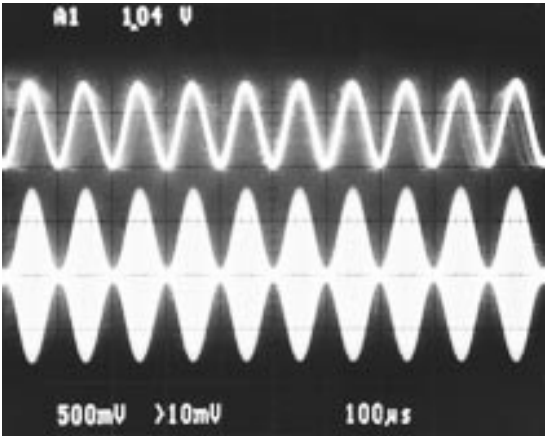
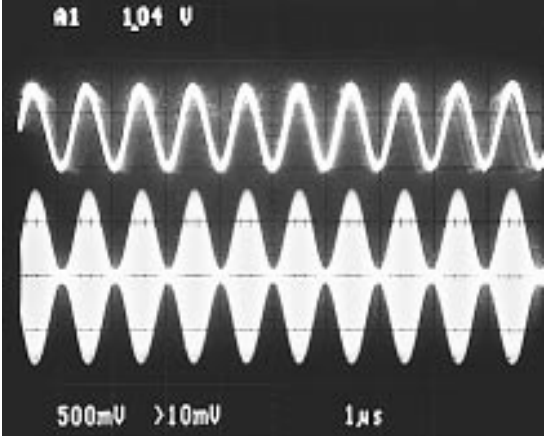


Figure 31. Input Signal and AM Modulated Carrier for  $f_{mod} = 1.0 \text{ MHz}$



# MC13176

Figure 32. Circuit Side View of MC13176D

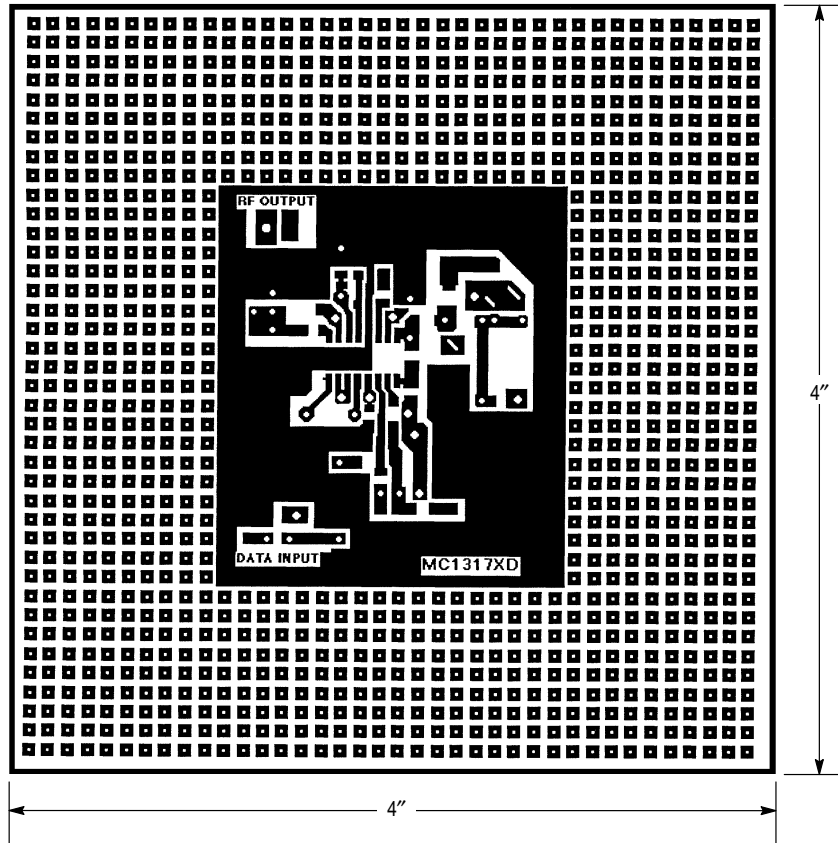
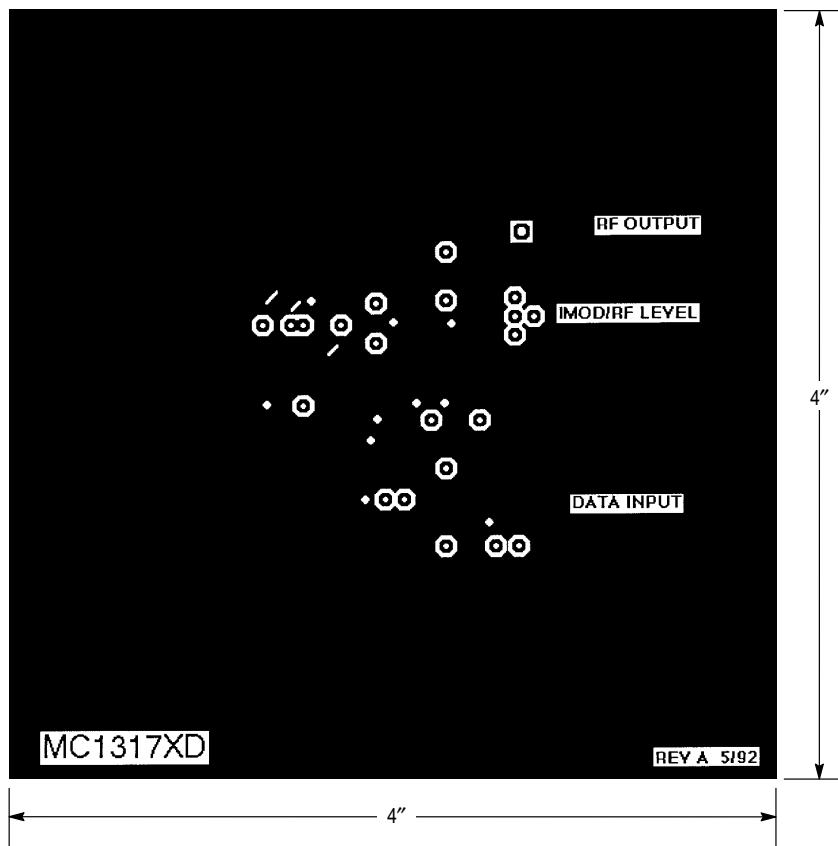


Figure 33. Ground Side View



## MC13176

Figure 34. Surface Mounted Components Placement  
(on Circuit Side)

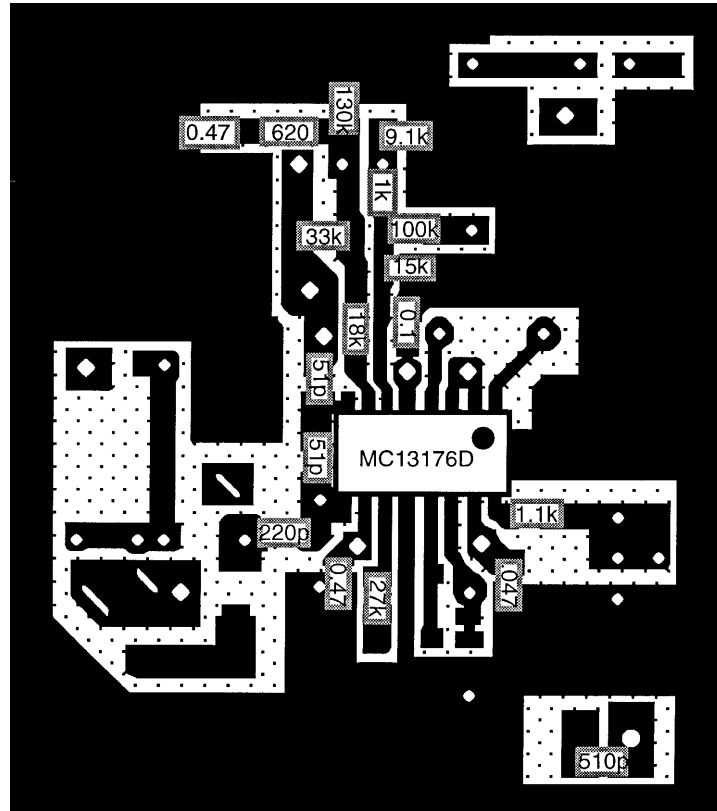
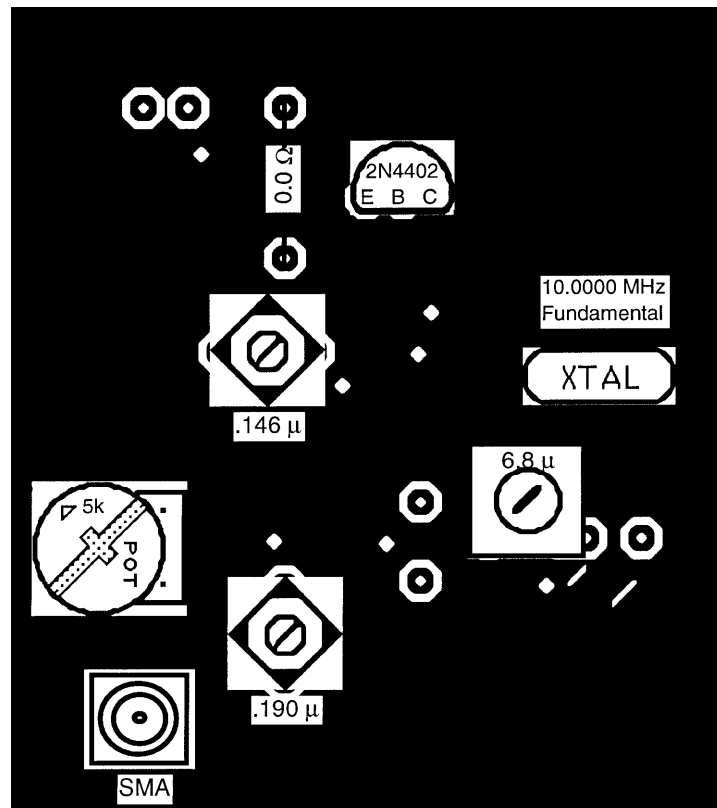


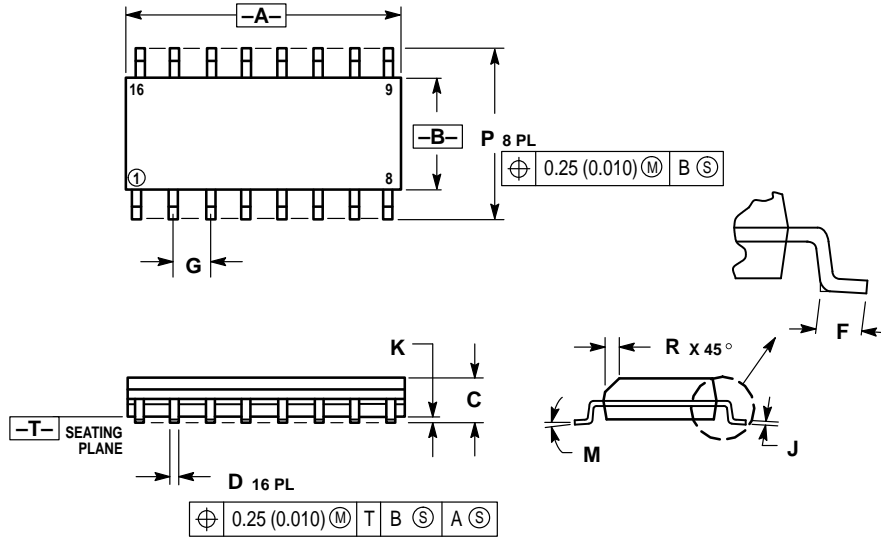
Figure 35. Radial Leaded Components Placement  
(on Ground Side)



# MC13176

## OUTLINE DIMENSIONS

**D SUFFIX**  
PLASTIC PACKAGE  
CASE 751B-05  
(SO-16)  
ISSUE J



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
E	0.40	1.25	0.016	0.049
F	1.27 BSC		0.050 BSC	
G	0.19	0.25	0.008	0.009
H	0.10	0.25	0.004	0.009
I	0°	7°	0°	7°
J	5.80	6.20	0.229	0.244
K	0.25	0.50	0.010	0.019

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