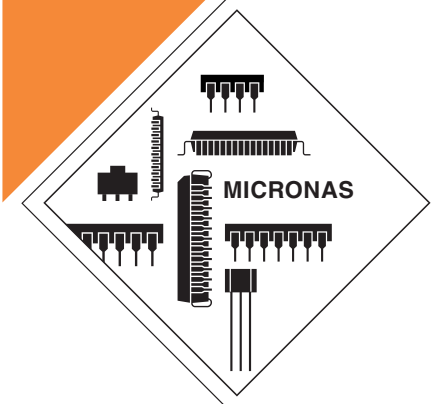


PRELIMINARY DATA SHEET

VPC 323xD
Comb Filter Video Processor

Edition July 26, 2001
6251-472-1PD

MICRONAS

Contents

Contents, continued

Contents, continued

Comb Filter Video Processor

1. Introduction

The VPC 323xD is a high-quality, single-chip video front-end, which is targeted for 4:3 and 16:9, 50/60-Hz and 100/120 Hz TV sets. It can be combined with other members of the DIGIT3000 IC family (such as DDP 331x) and/or it can be used with 3rd-party products.

The main features of the VPC 323xD are

- high-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
- multi-standard color decoder PAL/NTSC/SECAM including all substandards
- four CVBS, one S-VHS input, one CVBS output
- two RGB/YC_rC_b component inputs, one Fast Blank (FB) input
- integrated high-quality A/D converters and associated clamp and AGC circuits
- multi-standard sync processing
- linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling ‘Panoramavision’
- PAL+ preprocessing
- line-locked clock, data and sync, or 656-output interface
- peaking, contrast, brightness, color saturation and tint for RGB/YC_rC_b and CVBS/S-VHS
- high-quality soft mixer controlled by Fast Blank
- PIP processing for four picture sizes ($\frac{1}{4}$, $\frac{1}{9}$, $\frac{1}{16}$, or $\frac{1}{36}$ of normal size) with 8-bit resolution
- 15 predefined PIP display configurations and expert mode (fully programmable)
- control interface for external field memory
- I^2C-bus interface
- one 20.25-MHz crystal, few external components
- 80-pin PQFP package

1.1. System Architecture

Fig.1–1 shows the block diagram of the video processor

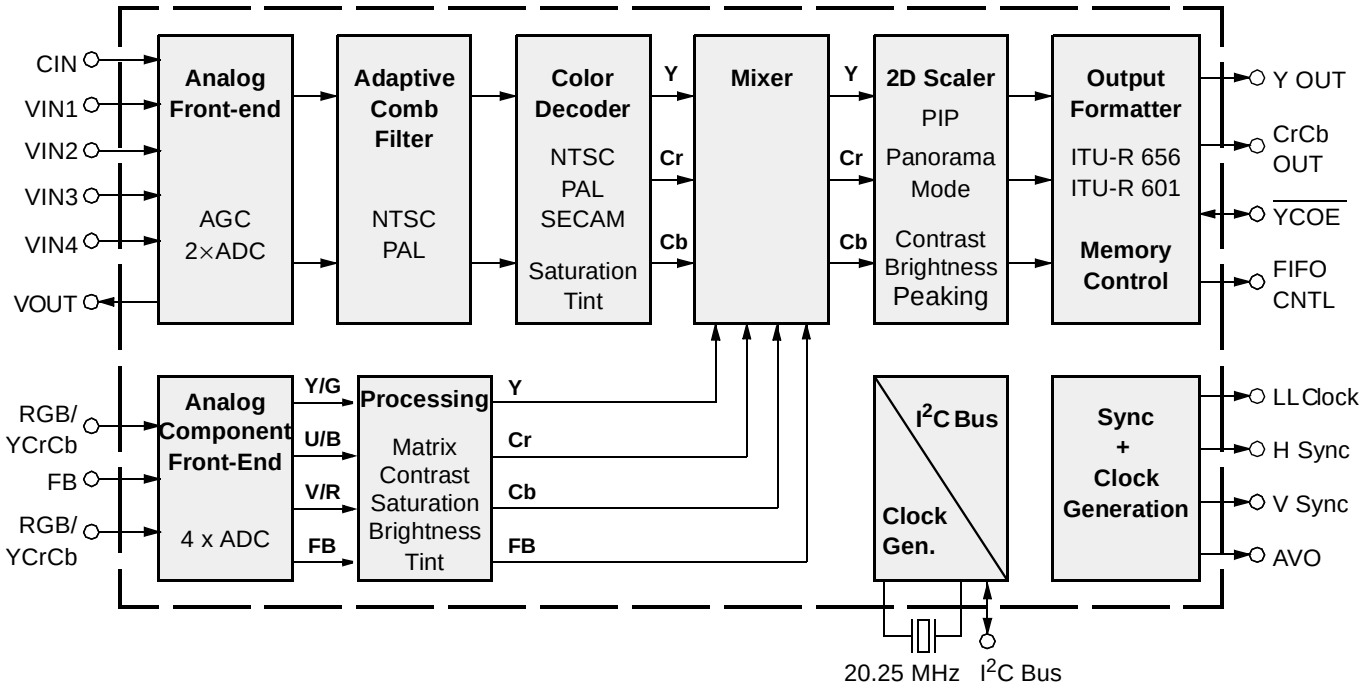


Fig. 1–1: Block diagram of the VPC 323xD

1.2. Video Processor Family

The VPC video processor family supports 15/32-kHz systems and is available with different comb filter options. Table 1–1 gives an overview of the VPC video processor family.

Table 1–1: VPC Processor Family for 100 Hz, Double-Scan and Line-Locked Clock Applications

	Features				
Type	**Adaptive Combfilter (PAL/NTSC)**	**Panorama Vision**	**Analog Component Inputs**	**Vertical Scaler (PIP)**	**Digital Output Interface**
VPC 32**30D**	4H	✓	2	✓	ITU-R 601, ITU-R 656
VPC 32**31D**		✓	2	✓	ITU-R 601, ITU-R 656
VPC 32**32D**	4H	✓		✓	ITU-R 601, ITU-R 656
VPC 32**33D**		✓		✓	ITU-R 601, ITU-R 656
VPC 32**15C**	4H	✓			ITU-R 601
VPC 32**10A**	2H	✓			ITU-R 601
VPC 32**11A**		✓			ITU-R 601

1.3. VPC Applications

Fig. 1–2 depicts several VPC applications. Since the VPC functions as a video front-end, it must be complemented with additional functionality to form a complete TV set.

The DDP 331x contains the video back-end with video postprocessing (contrast, peaking, CTI,...), H/V-deflection, RGB insertion (SCART, Text, PIP,...) and tube control (cutoff, white-drive, beam current limiter). It generates a beam scan velocity modulation output from the digital YC_rC_b and RGB signals. Note, that this signal is not generated from the external analog RGB inputs.

The component interface of the VPC 323xD provides a high-quality analog RGB interface with character insertion capability. It also allows appropriate processing of external sources, such as MPEG-2 set-top boxes in transparent (4:2:2) quality. Furthermore, it transforms RGB/Fast Blank signals to the common digital video bus and makes those signals available for 100-Hz upconversion or double-scan processing. In some European countries (Italy), this feature is mandatory.

SRC (e. g. SDA 94xx from Micronas) indicates memory based image processing, such as scan rate conversion, vertical processing (Zoom), or PAL+ reconstruction. The VPC supports memory-based applications through line-locked clocks, syncs, and data. Additionally, the VPC 323xD provides a 656-output interface and FIFO control signals.

Examples:

– Europe: 15 kHz/50 Hz → 32 kHz/100 Hz interlaced

– US: 15 kHz/60 Hz → 32 kHz/60 Hz non-interlaced

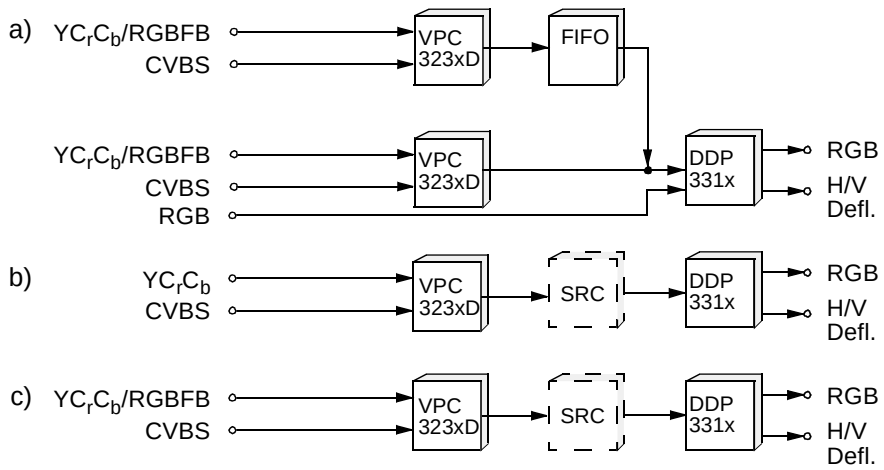


Fig. 1–2: VPC 32xxD applications
a) 15-kHz application Europe
b) double-scan application (US, Japan) with YC_rC_b inputs
c) 100-Hz application (Europe) with RGBFB inputs

2. Functional Description

2.1. Analog Video Front-End

This block provides the analog interfaces to all video inputs and mainly carries out analog-to-digital conversion for the following digital video processing. A block diagram is given in Fig. 2–1.

Most of the functional blocks in the front-end are digitally controlled (clamping, AGC, and clock-DCO). The control loops are closed by the Fast Processor ('FP') embedded in the decoder.

2.1.1. Input Selector

Up to five analog inputs can be connected. Four inputs are for composite video or S-VHS luma signal. These inputs are clamped to the sync back porch and are amplified by a variable gain amplifier. One input is for connection of S-VHS carrier chrominance signal. This input is internally biased and has a fixed gain amplifier. A second S-VHS chroma signal can be connected to video-input VIN1.

2.1.2. Clamping

The composite video input signals are AC coupled to the IC. The clamping voltage is stored on the coupling capacitors and is generated by digitally controlled current sources. The clamping level is the back porch of the video signal. S-VHS chroma is also AC coupled. The input pin is internally biased to the center of the ADC input range.

2.1.3. Automatic Gain Control

A digitally working automatic gain control adjusts the magnitude of the selected baseband by +6/–4.5 dB in 64 logarithmic steps to the optimal range of the ADC. The gain of the video input stage including the ADC is 213 steps/V with the AGC set to 0 dB.

2.1.4. Analog-to-Digital Converters

Two ADCs are provided to digitize the input signals. Each converter runs with 20.25 MHz and has 8 bit resolution. An integrated bandgap circuit generates the required reference voltages for the converters. The two ADCs are of a 2-stage subranging type.

2.1.5. Digitally Controlled Clock Oscillator

The clock generation is also a part of the analog front end. The crystal oscillator is controlled digitally by the control processor; the clock frequency can be adjusted within ±150 ppm.

2.1.6. Analog Video Output

The input signal of the Luma ADC is available at the analog video output pin. The signal at this pin must be buffered by a source follower. The output voltage is 2 V, thus the signal can be used to drive a 75 Ω line. The magnitude is adjusted with an AGC in 8 steps together with the main AGC.

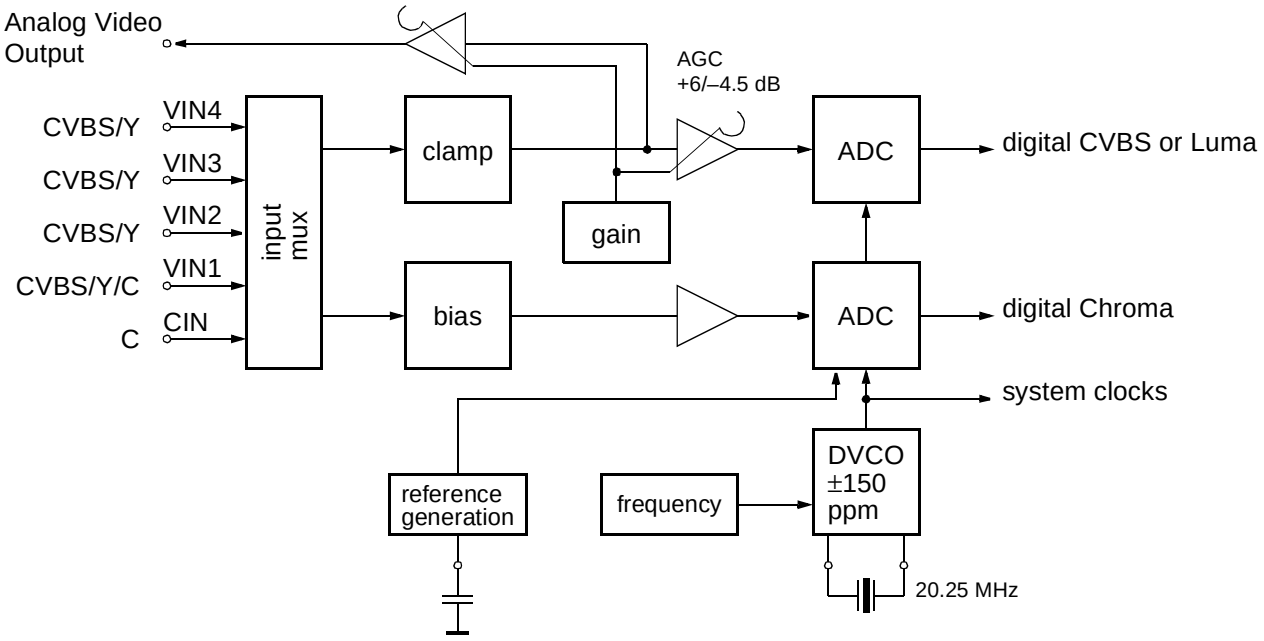


Fig. 2–1: Analog front-end

2.2. Adaptive Comb Filter

The 4H adaptive comb filter is used for high-quality luminance/chrominance separation for PAL or NTSC composite video signals. The comb filter improves the luminance resolution (bandwidth) and reduces interferences like cross-luminance and cross-color. The adaptive algorithm eliminates most of the mentioned errors without introducing new artifacts or noise.

A block diagram of the comb filter is shown in Fig. 2–2. The filter uses four line delays to process the information of three video lines. To have a fixed phase relationship of the color subcarrier in the three channels, the system clock (20.25 MHz) is fractionally locked to the color subcarrier. This allows the processing of all color standards and substandards using a single crystal frequency.

The CVBS signal in the three channels is filtered at the subcarrier frequency by a set of bandpass/notch filters. The output of the three channels is used by the adaption logic to select the weighting that is used to reconstruct the luminance/chrominance signal from the 4 bandpass/notch filter signals. By using soft mixing of the 4 signals switching artifacts of the adaption algorithm are completely suppressed.

The comb filter uses the middle line as reference, therefore, the comb filter delay is two lines. If the comb filter is switched off, the delay lines are used to pass the luma/chroma signals from the A/D converters to the luma/chroma outputs. Thus, the processing delay is always two lines.

In order to obtain the best-suited picture quality, the user has the possibility to influence the behavior of the adaption algorithm going from moderate combing to strong combing. Therefore, the following three parameters may be adjusted:

– HDG (horizontal difference gain)

– VDG (vertical difference gain)

– DDR (diagonal dot reducer)

HDG typically defines the comb strength on horizontal edges. It determines the amount of the remaining cross-luminance and the sharpness on edges respectively. As HDG increases, the comb strength, e. g. cross luminance reduction and sharpness, increases.

VDG typically determines the comb filter behavior on vertical edges. As VDG increases, the comb strength, e. g. the amount of hanging dots, decreases.

After selecting the combfilter performance in horizontal and vertical direction, the diagonal picture performance may further be optimized by adjusting DDR. As DDR increases, the dot crawl on diagonal colored edges is reduced.

To enhance the vertical resolution of the picture, the VPC provides a vertical peaking circuitry. The filter gain is adjustable between 0 – +6 dB and a coring filter suppresses small amplitudes to reduce noise artifacts. In relation to the comb filter, this vertical peaking widely contributes to an optimal two-dimensional resolution homogeneity.

2.3. Color Decoder

In this block, the standard luma/chroma separation and multi-standard color demodulation is carried out. The color demodulation uses an asynchronous clock, thus allowing a unified architecture for all color standards.

A block diagram of the color decoder is shown in Fig. 2–4. The luma as well as the chroma processing, is shown here. The color decoder also provides several special modes, e.g. wide band chroma format which is intended for S-VHS wide bandwidth chroma. Also, filter settings are available for processing a PAL+ helper signal.

If the adaptive comb filter is used for luma chroma separation, the color decoder uses the S-VHS mode processing. The output of the color decoder is YC_rC_b in a 4:2:2 format.

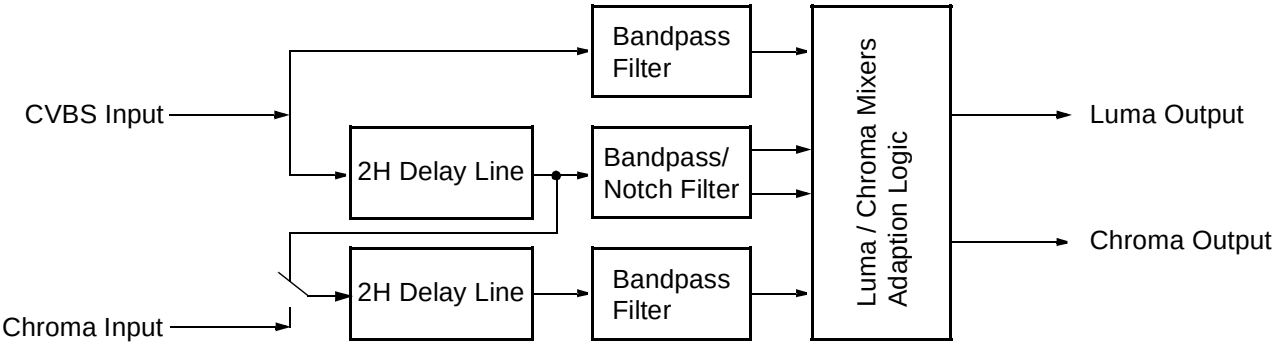


Fig. 2–2: Block diagram of the adaptive comb filter (PAL mode)

2.3.1. IF-Compensation

With off-air or mistuned reception, any attenuation at higher frequencies or asymmetry around the color subcarrier is compensated. Four different settings of the IF-compensation are possible (see Fig. 2–3):

– flat (no compensation)

– 6 dB/octave

– 12 dB/octave

– 10 dB/MHz

The last setting gives a very large boost to high frequencies. It is provided for SECAM signals that are decoded using a SAW filter specified originally for the PAL standard.

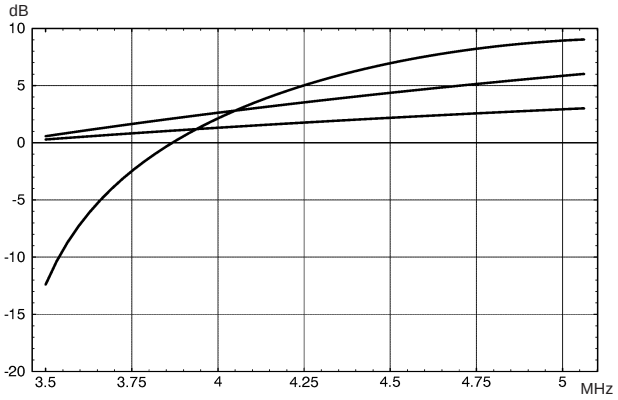


Fig. 2–3: Frequency response of chroma IF-compensation

2.3.2. Demodulator

The entire signal (which might still contain luma) is quadrature-mixed to the baseband. The mixing frequency is equal to the subcarrier for PAL and NTSC, thus achieving the chroma demodulation. For SECAM, the mixing frequency is 4.286 MHz giving the quadrature baseband components of the FM modulated chroma. After the mixer, a lowpass filter selects the chroma components; a downsampling stage converts the color difference signals to a multiplexed half rate data stream.

The subcarrier frequency in the demodulator is generated by direct digital synthesis; therefore, substandards such as PAL 3.58 or NTSC 4.43 can also be demodulated.

2.3.3. Chrominance Filter

The demodulation is followed by a lowpass filter for the color difference signals for PAL/NTSC. SECAM requires a modified lowpass function with bell filter characteristic. At the output of the lowpass filter, all luma information is eliminated.

The lowpass filters are calculated in time multiplex for the two color signals. Three bandwidth settings (narrow, normal, broad) are available for each standard (see Fig. 2–5). For PAL/NTSC, a wide band chroma filter can be selected. This filter is intended for high bandwidth chroma signals, e.g. a nonstandard wide bandwidth S-VHS signal.

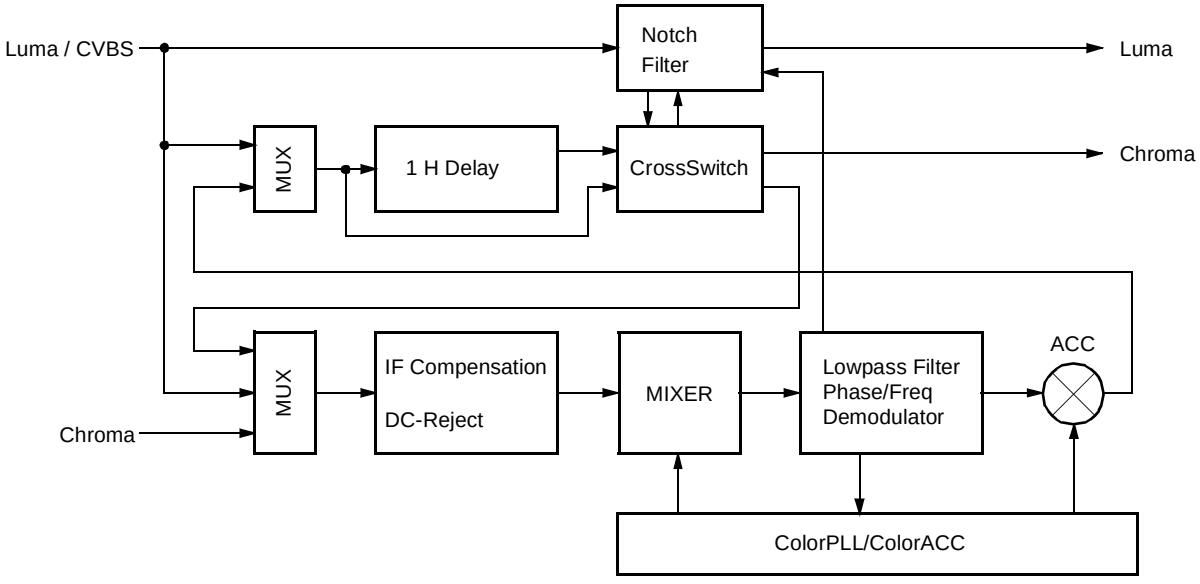


Fig. 2–4: Color decoder

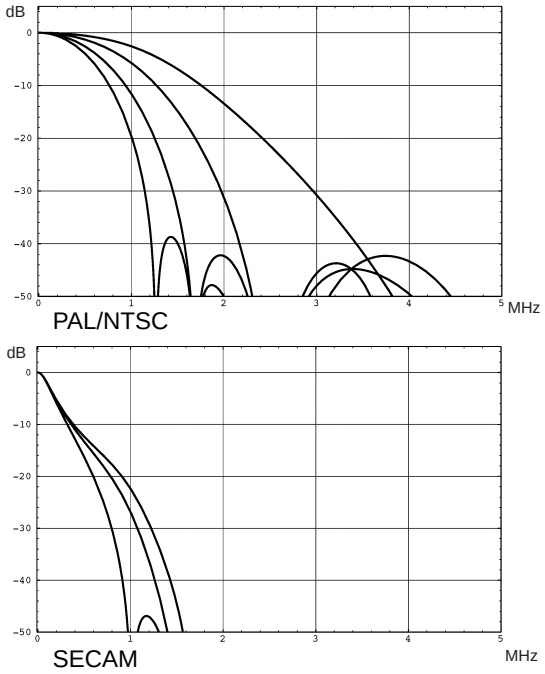


Fig. 2–5: Frequency response of chroma filters

2.3.4. Frequency Demodulator

The frequency demodulator for demodulating the SECAM signal is implemented as a CORDIC-structure. It calculates the phase and magnitude of the quadrature components by coordinate rotation.

The phase output of the CORDIC processor is differentiated to obtain the demodulated frequency. After the deemphasis filter, the Dr and Db signals are scaled to standard C_rC_b amplitudes and fed to the cross-over-switch.

2.3.5. Burst Detection / Saturation Control

In the PAL/NTSC system the burst is the reference for the color signal. The phase and magnitude outputs of the CORDIC are gated with the color key and used for controlling the phase-locked loop (APC) of the demodulator and the automatic color control (ACC) in PAL/NTSC.

The ACC has a control range of +30 ... –6 dB.

Color saturation is adjustable independently of the color standard. In PAL/NTSC it is used as reference for the ACC. In SECAM the necessary gains are calculated automatically.

For SECAM decoding, the frequency of the burst is measured. Thus, the current chroma carrier frequency can be identified and is used to control the SECAM processing. The burst measurements also control the color killer operation; they are used for automatic standard detection as well.

2.3.6. Color Killer Operation

The color killer uses the burst-phase/burst-frequency measurement to identify a PAL/NTSC or SECAM color signal. For PAL/NTSC, the color is switched off (killed) as long as the color subcarrier PLL is not locked. For SECAM, the killer is controlled by the toggle of the burst frequency. The burst amplitude measurement is used to switch off the color if the burst amplitude is below a programmable threshold. Thus, color will be killed for very noisy signals. The color amplitude killer has a programmable hysteresis.

2.3.7. Automatic Standard Recognition

The burst-frequency measurement is also used for automatic standard recognition (together with the status of horizontal and vertical locking) thus allowing a completely independent search of the line and color standard of the input signal. The following standards can be distinguished:

PAL B,G,H,I; NTSC M; SECAM; NTSC 44; PAL M; PAL N; PAL 60

For a preselection of allowed standards, the recognition can be enabled/disabled via I^2C bus for each standard separately.

If at least one standard is enabled, the VPC 323xD checks regularly the horizontal and vertical locking of the input signal and the state of the color killer. If an error exists for several adjacent fields a new standard search is started. Depending on the measured line number and burst frequency the current standard is selected.

For error handling, the recognition algorithm delivers the following status information:

– search active (busy)

– search terminated, but failed

– found standard is disabled

– vertical standard invalid

– no color found

2.3.8. PAL Compensation/1-H Comb Filter

The color decoder uses one fully integrated delay line. Only active video is stored.

The delay line application depends on the color standard:

– NTSC: 1-H comb filter **or** color compensation

– PAL: color compensation

– SECAM: crossover switch

In the NTSC compensated mode, Fig. 2–6 c), the color signal is averaged for two adjacent lines. Thus, cross-color distortion and chroma noise is reduced. In the NTSC 1-H comb filter mode, Fig. 2–6 d), the delay line is in the composite signal path, thus allowing reduction of cross-color components, as well as cross-luminance. The loss of vertical resolution in the luminance channel is compensated by adding the vertical detail signal with removed color information. If the 4H adaptive comb filter is used, the 1-H NTSC comb filter has to be deselected.

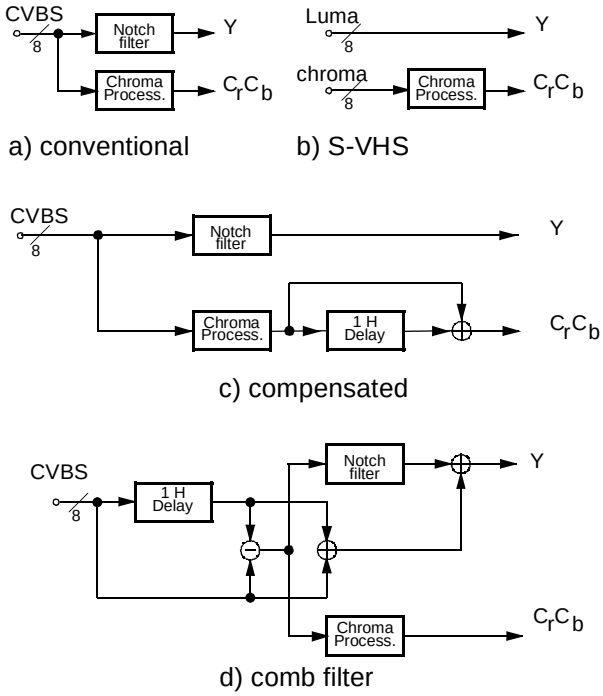


Fig. 2–6: NTSC color decoding options

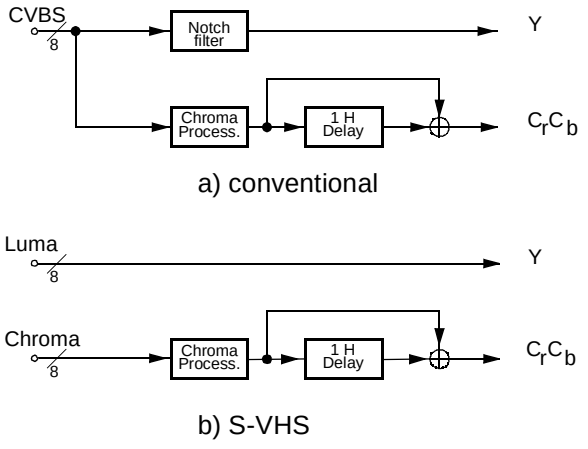


Fig. 2–7: PAL color decoding options

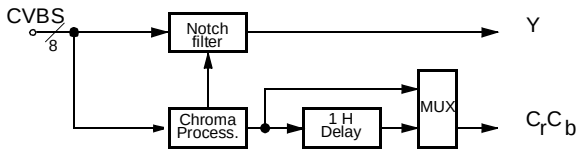
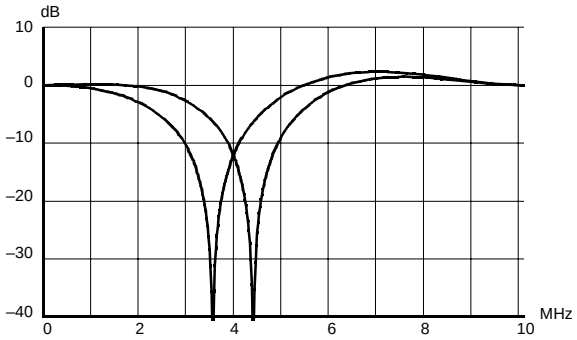


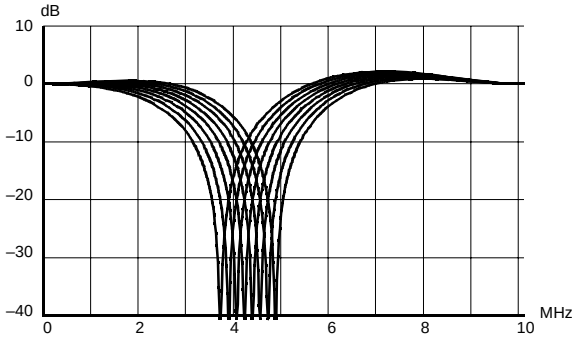
Fig. 2–8: SECAM color decoding

2.3.9. Luminance Notch Filter

If a composite video signal is applied, the color information is suppressed by a programmable notch filter. The position of the filter center frequency depends on the subcarrier frequency for PAL/NTSC. For SECAM, the notch is directly controlled by the chroma carrier frequency. This considerably reduces the cross-luminance. The frequency responses for all three systems are shown in Fig. 2–9.



PAL/NTSC notch filter



SECAM notch filter

Fig. 2–9: Frequency responses of the luma notch filter for PAL, NTSC, SECAM

2.3.10. Skew Filtering

The system clock is free-running and not locked to the TV line frequency. Therefore, the ADC sampling pattern is not orthogonal. The decoded YC_rC_b signals are converted to an orthogonal sampling raster by the skew filters, which are part of the scaler block.

The skew filters are controlled by a skew parameter and allow the application of a group delay to the input signals without introducing waveform or frequency response distortion.

The amount of phase shift of this filter is controlled by the horizontal PLL1. The accuracy of the filters is 1/32 clocks for luminance and 1/4 clocks for chroma. Thus the 4:2:2 YC_rC_b data is in an orthogonal pixel format even in the case of nonstandard input signals such as VCR.

2.4. Component Interface Processor CIP

This block (see Fig. 2–10) contains all the necessary circuitry dedicated to external analog components (YC_rC_b_cip) such as RGB or YC_rC_b signals from DVD players, or other RGB sources with Fast Blank for real time insertion on the main picture (YC_rC_b_main).

2.4.1. Component Analog Front-End

VPC 323xD provides two analog RGB/YC_rC_b input ports, one with Fast Blank capability and one without.

Analog component signals contain high-frequency components (e. g. OSD) and/or high-frequency clock residues. Thus, it is recommended to implement analog anti-alias low-pass filters on each input, including FB (e. g. –3 dB at 5…6 MHz). While all signals are coupled by 220 nF clamping capacitors, the Fast Blank input requires DC coupling.

The selected signal channel is further converted into a digital form by three high-quality ADCs running at 20.25 MHz with a resolution of 8 bit. The FB input is digitized with a resolution of 6 bit.

Note: The VPC 323xD is synchronized always by the main CVBS/Y ADC input. In component mode, the sync signal has to be fed to this input accordingly.

2.4.2. Matrix

The RGB signals are converted to the YC_rC_b format by a matrix operation:

$$Y = 0.299R + 0.587G + 0.114B$$
$$(R–Y)= 0.701R – 0.587G – 0.114B$$
$$(B–Y)=–0.299R – 0.587G + 0.886B$$

In case of YC_rC_b input the matrix is bypassed.

2.4.3. Component YC_rC_b Control

The VPC 323xD supports the following picture adjustment parameters on the component signal:

– $0 \le$ contrast $\le 63/32$

– $-128 \le$ brightness ≤ 127

– $0 \le$ saturation $C_r \le 63/32$

– $0 \le$ saturation $C_b \le 63/32$

– $-20 \le$ tint ≤ 20 degrees

Table 2–1 shows the settings to achieve exact level matching between YC_rC_b_cip and YC_rC_b_main channel.

Table 2–1: Standard picture settings

input format	contrast	brightness	satCr	satCb
RGB	**27**	**68**	**29**	**23**
YC_rC_b	**27**	**68**	**40**	**40**

Note: R, G, B, C_r, C_b, = 0.7 V_{pp}, Y(+ sync) 1 V_{pp}

2.4.4. Softmixer

After an automatic delay matching, the component signals and the upsampled main video signal are gathered onto a unique YC_rC_b channel by means of a versatile 4:4:4 softmixer (see also Fig. 2–10).

The softmixer circuit consists of a Fast Blank (FB) processing block supplying a mixing factor k (0...64) to a high quality signal mixer achieving the output function:

YC_rC_b_mix=(k*YC_rC_b_main+ (64-k)*YC_rC_b_cip)/64

The softmixer supports several basic modes that are selected via I^2C bus (see Table 2–2).

2.4.4.1. Static Switch Mode

In its simplest and most common application the softmixer is used as a static switch between YC_rC_b_main and YC_rC_b_cip. This is for instance the adequate way to handle a DVD component signal.

The factor k is clamped to 0 or 64, hence selecting YC_rC_b_main or the component input YC_rC_b_cip (see Table 2–2).

2.4.4.2. Static Mixer Mode

The signal YC_rC_b_main and the component signal YC_rC_b_cip may also be statically mixed. In this environment, k is manually controlled via I^2C registers FBGAIN and FBOFFS according to the following expression:

$$k = FBGAIN*(31–FBOFFS) + 32$$

All the necessary limitation and rounding operation are built-in to fit the range: $0 \leq k \leq 64$.

In the static mixer mode as well as in the previously mentioned static switch mode (see Table 2–2), the softmixer operates independently of the analog Fast Blank input.

2.4.4.3. Dynamic Mixer Mode

In the dynamic mixer mode, the mixer is controlled by the Fast Blank signal. The VPC 323xD provides a linear mixing coefficient

$$k=kl = FBGAIN*(FB–FBOFFS) + 32$$

(FB is the digitized Fast Blank), and a non-linear mixing coefficient knl=F(kl), which results from a further non-linear processing of kl.

While the linear mixing coefficient is used to insert a full-screen video signal, the non-linear coefficient is well-suited to insert Fast Blank related signals like text.

The non-linear mixing reduces disturbing effects like over/undershoots at critical Fast Blank edges.

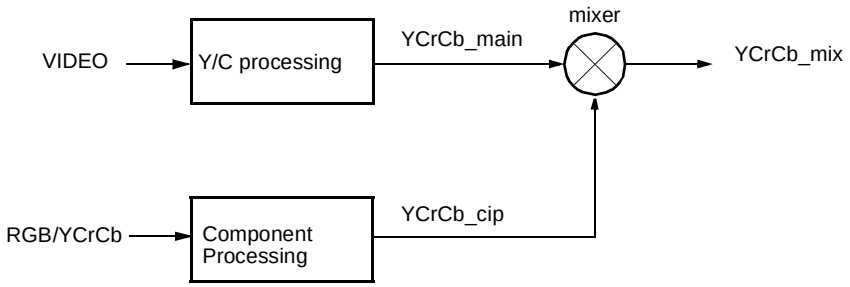


Fig. 2–10: Block diagram of the component mixer

Table 2–2: CIP softmixer modes

I^2C CIP mode	SELLIN	RGB DLY	FBCLP	FB MODE
Force YC_rC_b main	0	0	x	11
Force RGB/ YC_rC_b	0	0	x	x0
Static Mixer	0	0	1	01
FB Linear	0	0	0	01
FB non-Linear	1	1	0	01

2.4.5. 4:4:4 to 4:2:2 Downsampling

After the mixer, the 4:4:4 YC_rC_b_mix data stream is downsampled to the 4:2:2 format. For this sake, a chroma lowpass filter is provided to eliminate high-frequency components above 5-6 Mhz which may typically be present on inserted high resolution RGB/ YC_rC_b sources.

In case of main video processing (loop-through) only, it is recommended to bypass this filter by using the I^2C bit CIPCFBY.

2.4.6. Fast Blank and Signal Monitoring

The analog Fast Blank state is monitored by means of four I^2C readable bits. These bits may be used by the TV controller for SCART signal ident:

– FBHIGH: set by FB high, reset by register read at FB low

– FBSTAT: FB status at register read

– FBRISE: set by FB rising edge, reset by register read

– FBFALL: set by FB falling edge, reset by register read

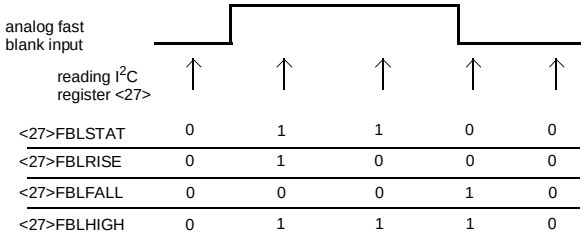


Fig. 2–11: Fast Blank Monitor

An additional monitoring bit is also provided for the RGB/YC_rC_b signal; it indicates whether the ADCs inputs are clipped or not. In case of clipping conditions (1Vpp RGB input for example) the ADC range can be extended by 3db by using the XAR bit.

– CLIPD: set by RGB/YC_rC_b input clip, reset by register read

2.5. Horizontal Scaler

The 4:2:2 YC_rC_b signal from the mixer output is processed by the horizontal scaler. It contains a lowpass filter, a prescaler, a scaling engine and a peaking filter. The scaler block allows a linear or nonlinear horizontal scaling of the input signal in the range of 1/32 to 4. Nonlinear scaling, also called “panorama vision”, provides a geometrical distortion of the input picture. It is used to fit a picture with 4:3 format on a 16:9 screen by stretching the picture geometry at the borders. Also, the inverse effect - called water glass - can be produced by the scaler. A summary of scaler modes is given in Table 2–3.

2.5.1. Horizontal Lowpass-filter

The luma filter block applies anti-aliasing lowpass filters. The cutoff frequencies are selectable and have to be adapted to the horizontal scaling ratio.

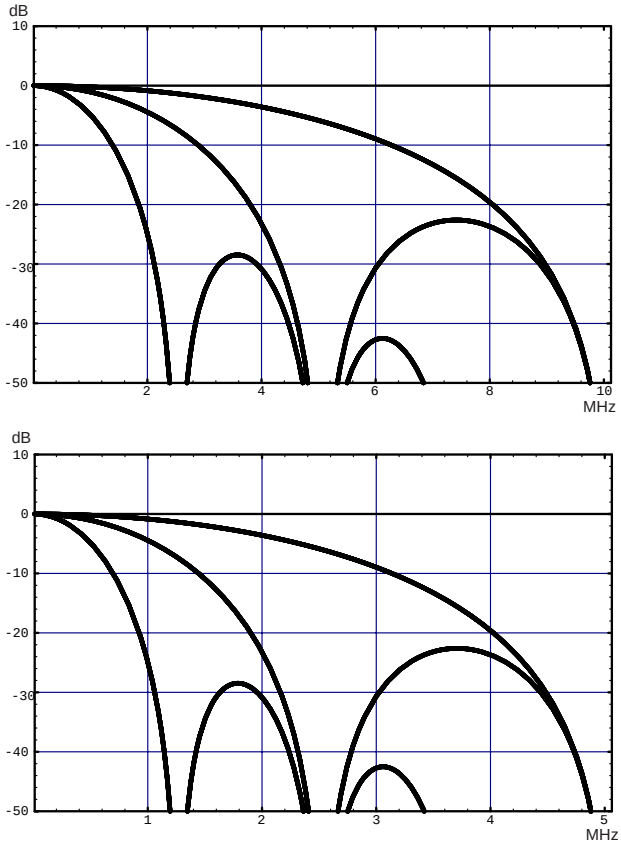


Fig. 2–12: YC_rC_b downsampling lowpass-filter

2.5.2. Horizontal Prescaler

To achieve a horizontal compression ratio between 1/4 and 1/32 (e. g. for double window or PIP operation) a linear downsampler resamples the input signal by 1 (=no presampling), 2, 4, and 8.

2.5.3. Horizontal Scaling Engine

The scaler contains a programmable decimation filter, a 1-H FIFO memory, and a programmable interpolation filter. The scaler input filter is also used for pixel skew correction, see 2.3.10. The decimator/interpolator structure allows optimal use of the FIFO memory. It allows a linear or nonlinear horizontal scaling of the input video signal in the range of 0.25 to 4. The controlling of the scaler is done by the internal Fast Processor.

Table 2–3: Scaler modes

Mode	Scale Factor	Description
Compression 4:3 → 16:9	0.75 linear	4:3 source displayed on a 16:9 tube, with side panels
Panorama 4:3 →16:9	non-linear compr	4:3 source displayed on a 16:9 tube, Borders distorted
Zoom 4:3 → 4:3	1.33 linear	Letterbox source (PAL+) displayed on a 4:3 tube, vertical overscan with cropping of side panels
Water glass 16:9 → 4:3	non-linear zoom	Letterbox source (PAL+) displayed on a 4:3 tube, vertical overscan, borders distorted, no cropping
20.25 → 13.5 MHz	0.66	sample rate conversion to line-locked clock

2.5.4. Horizontal Peaking-filter

The horizontal scaler block offers an extra peaking filter for sharpness control. The center frequency of the peaking filter automatically adopts to the horizontal scaling ratio. Three center frequencies are selectable (see Fig. 2–13:)

– center at sampling rate / 2

– center at sampling rate / 4

– center at sampling rate / 6

The filter gain is adjustable between 0 – +10 dB and a coring filter suppresses small amplitudes to reduce noise artifacts.

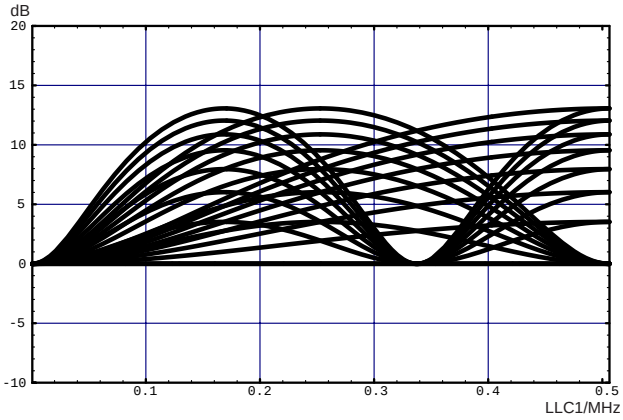


Fig. 2–13: Peaking characteristics

2.6. Vertical Scaler

For PIP operation, the vertical scaler compresses the incoming 4:2:2 YC_rC_b active video signal in vertical direction. It supports a vertical compression ratio of 1(= no compression), 2, 3, 4 and 6.

In case of a vertical compression of 2, 4 and 6, the filter performs the PAL compensation automatically and the standard PAL delay line should be bypassed (see 2.3.8.).

2.7. Contrast and Brightness

The VPC 323xD provides a selectable contrast and brightness adjustment for the luma samples. The control ranges are:

– 0 ≤contrast ≤63/32

– −128 ≤ brightness ≤ 127

Note: for ITU-R luma output code levels (16 ... 240), contrast has to be set to 48 and brightness has to be set to 16!

2.8. Blackline Detector

In case of a letterbox format input video, e.g. Cinemascope, PAL+ etc., black areas at the upper and lower part of the picture are visible. It is suitable to remove or reduce these areas by a vertical zoom and/or shift operation.

The VPC 323xD supports this feature by a letterbox detector. The circuitry detects black video lines by measuring the signal amplitude during active video. For every field the number of black lines at the upper and lower part of the picture are measured, compared to the previous measurement and the minima are stored in the I^2C register BLKLIN. To adjust the picture amplitude, the external controller reads this register, calculates the vertical scaling coefficient and transfers the new settings, e.g. vertical sawtooth parameters, horizontal scaling coefficient etc., to the VPC.

Letterbox signals containing logos on the left or right side of the black areas are processed as black lines, while subtitles, inserted in the black areas, are processed as non-black lines. Therefore the subtitles are visible on the screen. To suppress the subtitles, the vertical zoom coefficient is calculated by selecting the larger number of black lines only. Dark video scenes with a low contrast level compared to the letterbox area are indicated by the BLKPIC bit.

2.9. Control and Data Output Signals

The VPC 323xD supports two output modes: In DIGIT3000 mode, the output interfaces run at the main system clock, in line-locked mode, the VPC generates an asynchronous line-locked clock that is used for the output interfaces. The VPC delivers either a YC_rC_b 4:2:2 or a YC_rC_b 4:1:1 data stream, each with separate sync information. In case of YC_rC_b 4:2:2 format, the VPC 323xD also provides an interface with embedded syncs according to ITU-R656.

2.9.1. Line-Locked Clock Generation

An on-chip rate multiplier is used to synthesize any desired output clock frequency of 13.5/16/18 MHz. A double clock frequency output is available to support 100 Hz systems. The synthesizer is controlled by the embedded RISC controller, which also controls all front-end loops (clamp, AGC, PLL1, etc.). This allows the generation of a line-locked output clock regardless of the system clock (20.25 MHz) which is used for comb filter operation and color decoding. The control of scaling and output clock frequency is kept independent to allow aspect ratio conversion combined with sample rate conversion. The line-locked clock circuity generates control signals, e.g. horizontal/vertical sync, active video output, it is also the interface from the internal (20.25 MHz) clock to the external line-locked clock system.

If a line-locked clock is not required, i.e. in the DIGIT3000 mode, the system runs at the 20.25 MHz main clock. The horizontal timing reference in this mode is provided by the front-sync signal. In this case, the line-locked clock block and all interfaces run from the 20.25 MHz main clock. The synchronization signals from the line-locked clock block are still available, but for every line the internal counters are reset with the main-sync signal. A double clock signal is not available in DIGIT3000 mode.

2.9.2. Sync Signals

The front end will provide a number of sync/control signals which are output with the output clock. The sync signals are generated in the line-locked clock block.

– Href: horizontal sync
– AVO: active video out (programmable)
– HC: horizontal clamp (programmable)
– Vref: vertical sync
– INTLC: interlace

All horizontal signals are not qualified with field information, i.e. the signals are present on all lines. The horizontal timing is shown in Fig. 2–16. Details of the horizontal/vertical timing are given in Fig. 2–20.

Note: In the ITU-R656 compliant output format, the sync information is embedded in the data stream.

2.9.3. DIGIT3000 Output Format

The picture bus format between all DIGIT3000 ICs is 4:2:2 YC_rC_b with 20.25 MHz samples/s. Only active video is transferred, synchronized by the system main sync signal (MSY) which indicates the start of valid data for each scan line and which initializes the color multiplex. The video data is orthogonally sampled YC_rC_b, the output format is given in Table 2–4. The number of active samples per line is 1080 for all standards (525 and 625).

The output can be switched to 4:1:1 mode with the output format according to Table 2–5.

Via the MSY line, serial data is transferred which contains information about the main picture such as current line number, odd/even field etc.). It is generated by the deflection circuitry and represents the orthogonal timebase for the entire system.

Table 2–4: Orthogonal 4:2:2 output format

Luma	Y_1	Y_2	Y_3	Y_4
Chroma	C_{b1}	C_{r1}	C_{b3}	C_{r3}

2.9.4. Line-Locked 4:2:2 Output Format

In line-locked mode, the VPC 323xD provides the industry standard pixel stream for YC_rC_b data. The difference to DIGIT3000 native mode is only the number of active samples, which of course, depends on the chosen scaling factor. Thus, Table 2–4 is valid for both 4:2:2 modes.

2.9.5. Line-Locked 4:1:1 Output Format

The orthogonal 4:1:1 output format is compatible to the industry standard. The YC_rC_b samples are skew-corrected and interpolated to an orthogonal sampling raster (see Table 2–5).

Table 2–5: 4:1:1 Orthogonal output format

Luma Chroma	Y_1	Y_2	Y_3	Y_4
C_3, C_7	C_{b1}^7	C_{b1}^5	C_{b1}^3	C_{b1}^1
C_2, C_6	C_{b1}^6	C_{b1}^4	C_{b1}^2	C_{b1}^0
C_1, C_5	C_{r1}^7	C_{r1}^5	C_{r1}^3	C_{r1}^1
C_0, C_4	C_{r1}^6	C_{r1}^4	C_{r1}^2	C_{r1}^0

note: $C^*_x{}^Y$ (x = pixel number and y = bit number)

2.9.6. ITU-R 656 Output Format

This interface uses a YC_rC_b 4:2:2 data stream at a line-locked clock of 13.5 MHz. Luminance and chrominance information is multiplexed to 27 MHz in the following order:

$$C_{b1}, Y_1, C_{r1}, Y_2, \ldots$$

Timing reference codes are inserted into the data stream at the beginning and the end of each video line:

– a ‘Start of active video’-Header (SAV) is inserted before the first active video sample
– a ‘End of active video’-code (EAV) is inserted after the last active video sample.

The incoming videostream is limited to a range of 1...254 since the data words 0 and 255 are used for identification of the reference headers. Both headers contain information about the field type and field blanking. The data words occurring during the horizontal blanking interval between EAV and SAV are filled with 0x10 for luminance and 0x80 for chrominance information. Table 2–6 shows the format of the SAV and EAV header.

For activation of this output format, the following selections must be assured:

– 13.5 MHz line locked clock
– double-clock mode enabled
– ITU-R656-mode enabled
– binary offset for C_r/C_b data

Note that the following changes and extensions to the ITU-R656 standard have been included to support horizontal and vertical scaling:

– Both the length and the number of active video lines varies with the selected window parameters. For compliance with the ITU-R656 recommendation, a size of 720 samples per line must be selected for each window.
– During blanked video lines SAV/EAV headers are suppressed in pairs. To assure vertical sync detection the V-flag in the EAV header of the last active video line is set to 1. Additionally, during field blanking all SAV/EAV headers (with the V-flag set to 1) are inserted.

Table 2–6: Coding of the SAV/EAV-header

Word	Bit No. MSB							LSB
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
First	1	1	1	1	1	1	1	1
Second	0	0	0	0	0	0	0	0
Third	0	0	0	0	0	0	0	0
Fourth	T	F	V	H	P3	P2	P1	P0
F = 0 during field 1,F = 1 during field 2 V = 0 during active linesV = 1 during vertical field blanking H = 0 in SAV,H = 1 in EAV T = 1 (video task only)								

The bits P0, P1, P2, and P3 are Hamming-coded protection bits.

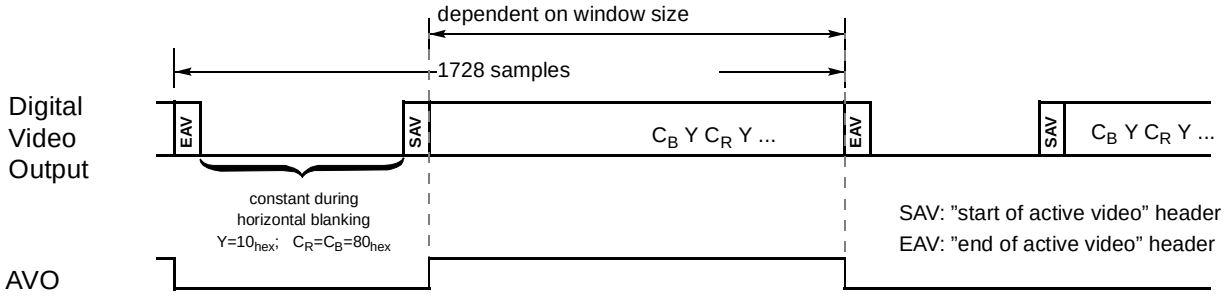


Fig. 2–14: Output of video data with embedded reference headers (@27 MHz)

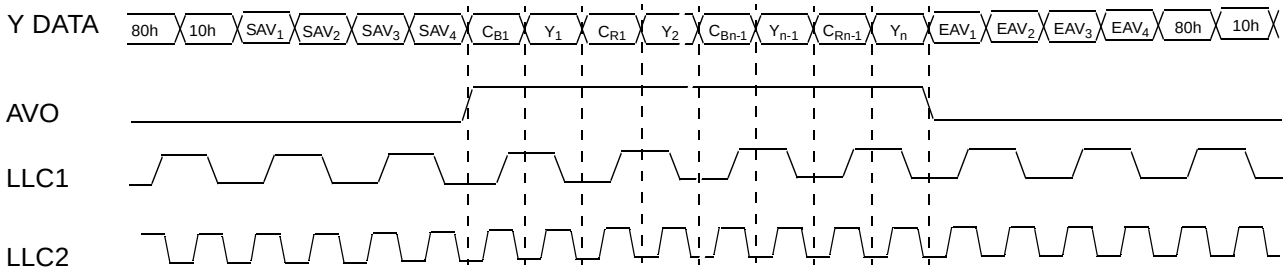


Fig. 2–15: Detailed data output (double-clock on)

Table 2–7: Output signals corresponding to the different formats

Format	dblclk	enable656	HSync	VSync	AVO	Y-Data	C-Data
16 bit YC_rC_b422	0	0	PAL/NTSC	PAL/NTSC	marks active pixels	4:2:2	4:2:2
8 bit YC_rC_b422	1	0	PAL/NTSC	PAL/NTSC	marks active pixels	4:2:2	tri-stated
ITU-R 656	1	1	not used	not used	not used	ITU-R 656	tri-stated

The multiplex of luminance and chrominance information and the embedding of 656-headers can be enabled independently. An overview of the resulting output formats and the corresponding signals is given in Table 2–7.

2.9.7. Output Code Levels

Output Code Levels correspond to ITU-R code levels:
Y = 16...240
Black Level = 16
C_rC_b = 128±112
An overview over the output code levels is given in Table 2–8.

2.9.8. Output Ports

All data and sync pins operate at TTL compliant levels and can be tri-stated via I^2C registers.

Additionally, the data outputs can be tri-stated via the YCOE output enable pin immediately. This function allows the digital insertion of a 2nd digital video source (e. g. MPEG aso.).

To ensure optimum EMI performance data and clock outputs automatically adopt the driver strength depending on their specific external load (max. 50pF). Therefore no external resistors and/or inductors should be connected to these pins. Sync and Fifo control pins have to be adjusted manually via an I^2C register.

2.9.9. Test Pattern Generator

The YC_rC_b outputs can be switched to a test mode where YC_rC_b data are generated digitally in the VPC 323xD. Test patterns include luma/chroma ramps, flat field and a pseudo color bar.

2.10. PAL+ Support

For PAL+, the VPC 323xD provides basic helper preprocessing:

- A/D conversion (shared with the existing ADCs)
- mixing with subcarrier frequency
- lowpass filter 2.5 MHz
- gain control by chroma ACC
- delay compensation to composite video path
- output at the luma output port

Helper signals are processed like the main video luma signals, i.e. they are subject to scaling, sample rate conversion and orthogonalization if activated. The adaptive comb filter processing is switched off for the helper lines.

It is expected that further helper processing (e.g. nonlinear expansion, matched filter) is performed outside the VPC.

2.10.1. Output Signals for PAL+/Color+ Support

For a PAL+/Color+ signal, the 625 line PAL image contains a 16/9 core picture of 431 lines which is in standard PAL format. The upper and lower 72 lines contain the PAL+ helper signal, and line 23 contains signalling information for the PAL+ transmission.

For PAL+ mode, the Y signal of the core picture, which is during lines 60–274 and 372–586, is replaced by the orthogonal composite video input signal. In order to fit the signal to the 8-bit port width, the ADC signal amplitudes are used. During the helper window, which is in lines 24–59, 275–310, 336–371, 587–622, the demodulated helper is signal processed by the horizontal scaler and the output circuitry. It is available at the luma output port. The processing in the helper reference lines 23 and 623 is different for the wide screen signaling part and the black reference and helper burst signals. The code levels are given in detail in Table 2–8, the output signal for the helper reference line is shown in Fig. 2–17.

Table 2–8: Output signal code levels for a PAL/PAL+ signal

Output Signal	Luma Outputs Y[7:0]			Chroma Outputs C[7:0]	
	Output Format	Black/Zero Level	Amplitude	Output Format	Amplitude
Standard YC_rC_b (100% Chroma)	binary	16	224	offset binary	128±112
				signed	±112
CVBS, C_rC_b	binary	64	149 (luma)	offset binary	128±112
				signed	±112
Demodulated Helper	signed	0	±109	–	–
Helper WSS	binary	68	149 (WSS:106)	–	–
Helper black level, Ref. Burst	offset binary	128	19 (128–109)	–	–

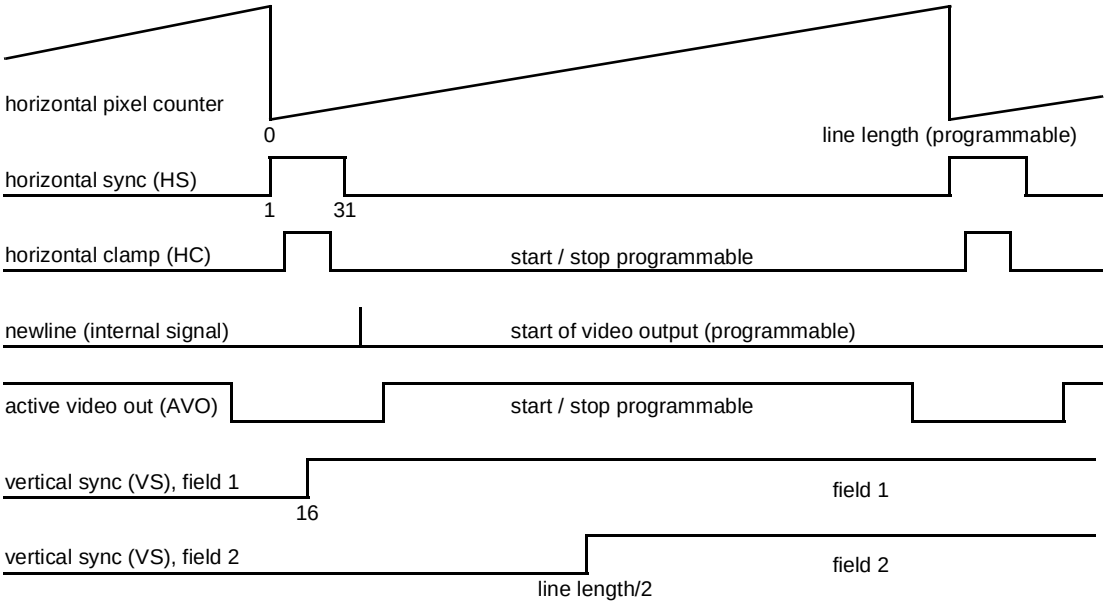


Fig. 2–16: Horizontal timing for line-locked mode

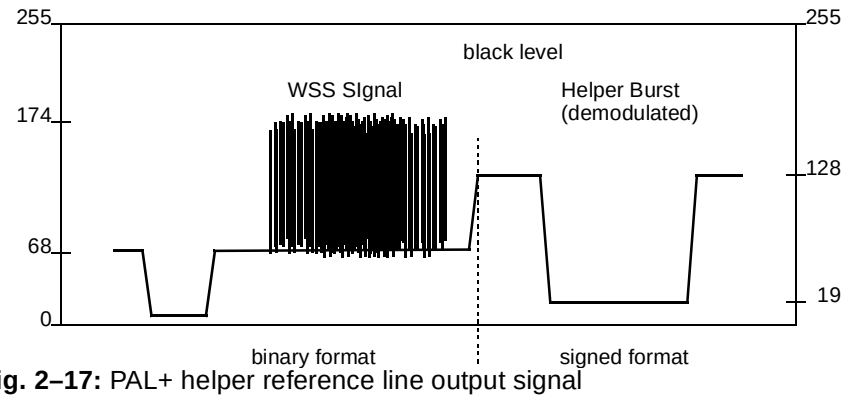


Fig. 2–17: PAL+ helper reference line output signal

2.11. Video Sync Processing

Fig. 2–18 shows a block diagram of the front-end sync processing. To extract the sync information from the video signal, a linear phase lowpass filter eliminates all noise and video contents above 1 MHz. The sync is separated by a slicer; the sync phase is measured. A variable window can be selected to improve the noise immunity of the slicer. The phase comparator measures the falling edge of sync, as well as the integrated sync pulse.

The sync phase error is filtered by a phase-locked loop that is computed by the FP. All timing in the front-end is derived from a counter that is part of this PLL, and it thus counts synchronously to the video signal.

A separate hardware block measures the signal back porch and also allows gathering the maximum/minimum of the video signal. This information is processed by the FP and used for gain control and clamping.

For vertical sync separation, the sliced video signal is integrated. The FP uses the integrator value to derive vertical sync and field information.

The information extracted by the video sync processing is multiplexed onto the hardware front sync signal (FSY) and is distributed to the rest of the video processing system. The format of the front sync signal is given in Fig. 2–19.

Frequency and phase characteristics of the analog video signal are derived from PLL1. The results are fed to the scaler unit for data interpolation and orthogonalization and to the clock synthesizer for line-locked clock generation. Horizontal and vertical syncs are latched with the line-locked clock.

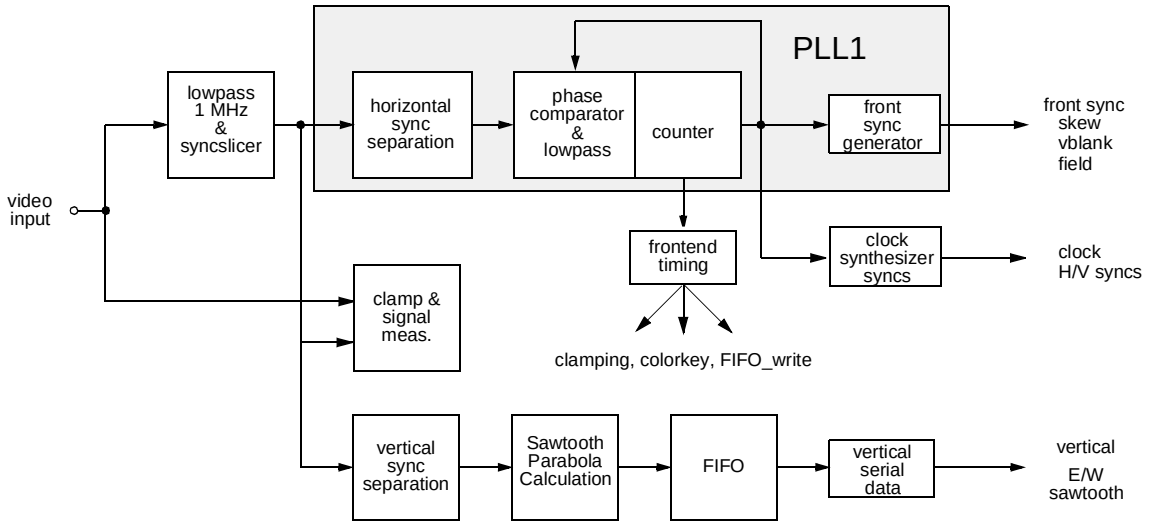


Fig. 2–18: Sync separation block diagram

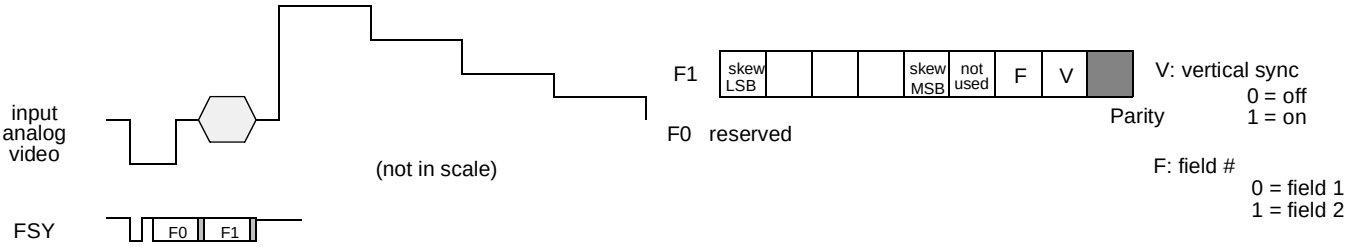
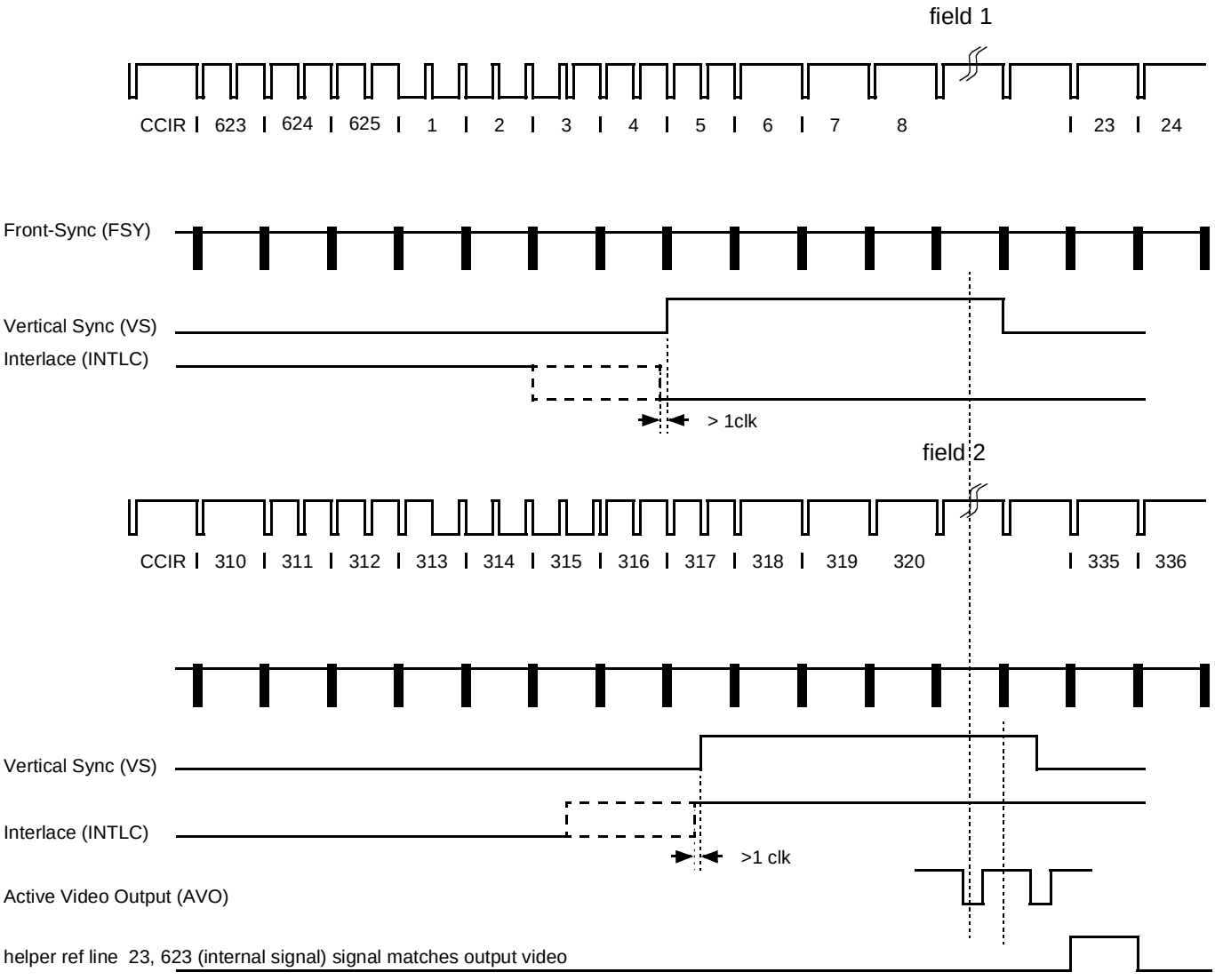


Fig. 2–19: Front sync format



The following signals are identical for field1 / field2

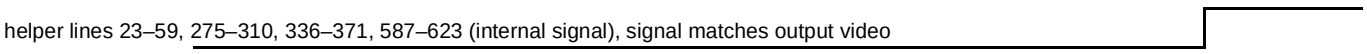


Fig. 2–20: Vertical timing of VPC 323xD shown in reference to input video.
Video output signals are delayed by 3-h for comb filter version (VPC 323xD).

2.12. Picture in Picture (PIP) Processing and Control

2.12.1. Configurations

To support PIP and/or scan rate conversion (SRC) applications, the VPC 323xD provides several control signals for an external field memory IC.

Fig. 2–21 demonstrates two applications with a single VPC 323xD. In these cases the VPC_{single} writes the main picture or one of several inset picture(s) into the field memory. Only one of these pictures is displayed live. These configurations are suitable for features such as turner scan, still picture, still in picture and simple scan rate conversion.

Fig. 2–22 shows an enhanced configuration with two VPC 323xD's. In this case, one live and several still pictures are inserted into the main live video signal. The VPC_{pip} processes the inset picture and writes the original or decimated picture into the field memory. The VPC_{main} delivers the main picture, combines it with the inset picture(s) from the field memory and stores the combined video signal into a second field memory for the SRC.

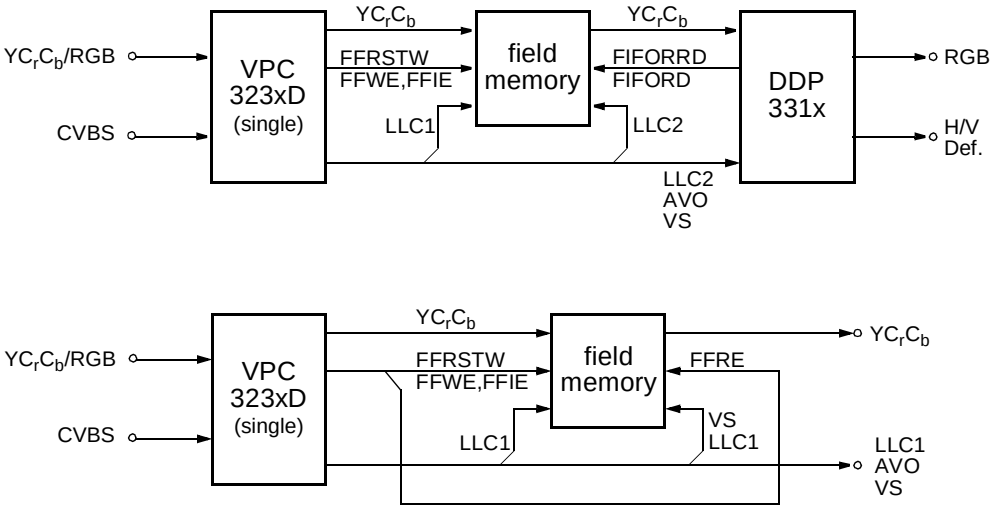
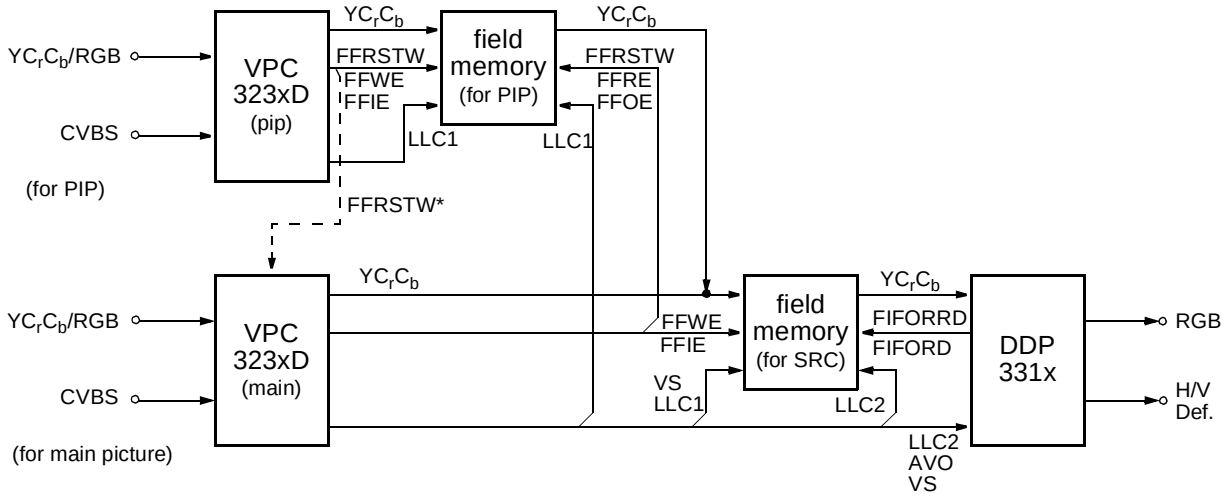


Fig. 2–21: Typical configurations with single VPC 323xD



* only used in the field-buffer-extension mode and the double-windows-extension mode

Fig. 2–22: Enhanced configuration with two VPC 323xD

A summary of VPC modes is given in Table 2–9.

Table 2–9: VPC 323xD modes for PIP applications

Working mode	Function
pip	- decimate the video signal for the inset pictures - write the inset pictures into the field memory - write the frame and background into the field memory
main	- deliver the video signal for the main picture - read the inset pictures from the field memory and insert them into the main picture - write the resulting video signal into the field memory for the scan rate conversion (SRC)
single	- decimate the video signal for the main or the inset picture(s) - write the inset pictures into the field memory - write the frame and background into the field memory - write the main picture part outside the inset pictures into the field memory - read the field memory (optional)

2.12.2. PIP Display Modes

To minimize the programming effort, 15 predefined PIP modes are already implemented, including double windows, single and multi-PIP (Fig. 2–23 and 2–24). In addition an expert mode is available for advanced PIP applications. In this case the inset picture size, as well as the PIP window arrangements are fully programmable.

Examples for the PIP mode programming are given in 5.2.

2.12.3. Predefined Inset Picture Size

The predefined PIP display modes are based on four fixed inset picture sizes (see Table 2–10). The corresponding picture resizing is achieved by the integrated horizontal and vertical scaler of VPC 323xD, which must be programmed accordingly (see Table 2–11 to 2–13).

The inset pictures are displayed with or without a frame controlled by I^2C. The fixed frame width is 4 pixels and 4 lines.

Table 2–10: Inset picture size (without frame) in the predefined PIP modes

size	horizontal [pixel/line]				vertical [line/field]	
	4:3 screen		16:9 screen		625 line	525 line
	13.5 MHz	16 MHz	13.5 MHz	16 MHz		
1/2	332	392	248	292	132	110
1/3	220	260	164	196	88	74
1/4	164	196	124	148	66	56
1/6	112	132	84	96	44	36

Table 2–11: Scaler Settings for predefined PIP modes at 13.5 MHz

PIP size	4:3				16:9			
	SCINC1 FP h'43	FFLIM FP h'42	SCPIP FP h'41	SCBRI FP h'52	SCINC1 FP h'43	FFLIM FP h'42	SCPIP FP h'41	SCBRI FP h'52
full	h'600	h'2d0	h'00	h'010	h'800	h'21c	h'00	h'010
1/2	h'600	h'168	h'11	h'110	h'400	h'10e	h'1a	h'210
1/3	h'480	h'f0	h'16	h'210	h'600	h'b4	h'1b	h'210
1/4	h'600	h'b4	h'1a	h'210	h'400	h'87	h'1b	h'310
1/6	h'480	h'78	h'1f	h'310	h'600	h'5a	h'1f	h'310
double win	h'600	h'168	h'01	h'110	h'600	h'168	h'01	h'110

Note: BR=16 in register SC-BRI!:

Table 2–12: Scaler Settings for predefined PIP modes at 16 MHz

PIP size	4:3				16:9			
	SCINC1 FP h'43	FFLIM FP h'42	SCPIP FP h'41	SCBRI FP h'52	SCINC1 FP h'43	FFLIM FP h'42	SCPIP FP h'41	SCBRI FP h'52
full	h'510	h'354	h'00	h'010	h'6c0	h'27f	h'00	h'010
1/2	h'510	h'1aa	h'11	h'110	h'6c0	h'140	h'11	h'110
1/3	h'798	h'11c	h'15	h'110	h'510	h'd4	h'16	h'210
1/4	h'510	h'd5	h'1a	h'210	h'6c0	h'a0	h'1a	h'210
1/6	h'798	h'8e	h'1e	h'210	h'510	h'6a	h'1f	h'310
double win	h'510	h'1aa	h'01	h'110	h'510	h'1aa	h'01	h'110

Note: BR=16 in register SC-BRI!:

Table 2–13: Settings for NEWLIN, AVSTRT and AVSTOP

PIP size	13.5 MHz				16.0 MHz			
	NEWLIN I^2C h'22		AVSTRT I^2C h'28	AVSTOP I^2C h'29	NEWLIN I^2C h'22		AVSTRT I^2C h'28	AVSTOP I^2C h'29
	VPC_{single} or VPC_{pip}	VPC_{main}			VPC_{single} or VPC_{pip}	VPC_{main}		
full	h'86	h'86	h'86	h'356	h'a8	h'a8	h'a8	h'3f0
1/2...1/6	h'194	h'86	h'86	h'356	h'1de	h'a8	h'a8	h'3f0
double win	h'86	h'86	h'86	h'356	h'a8	h'a8	h'a8	h'3f0

Note: NEWLIN and AVSTRT must be > 47, if FIFOTYPE=0 or 1

.

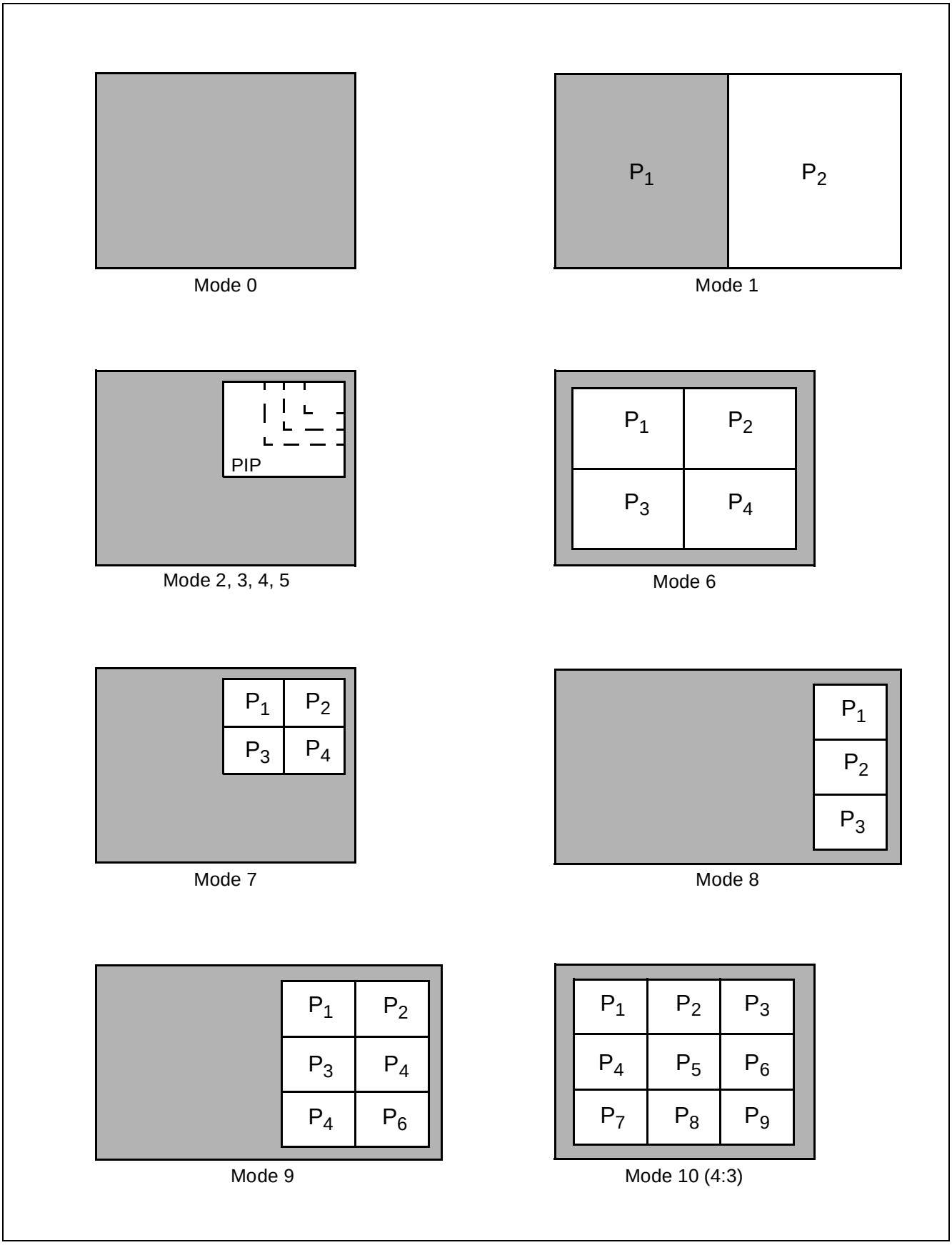


Fig. 2–23: Predefined PIP Modes

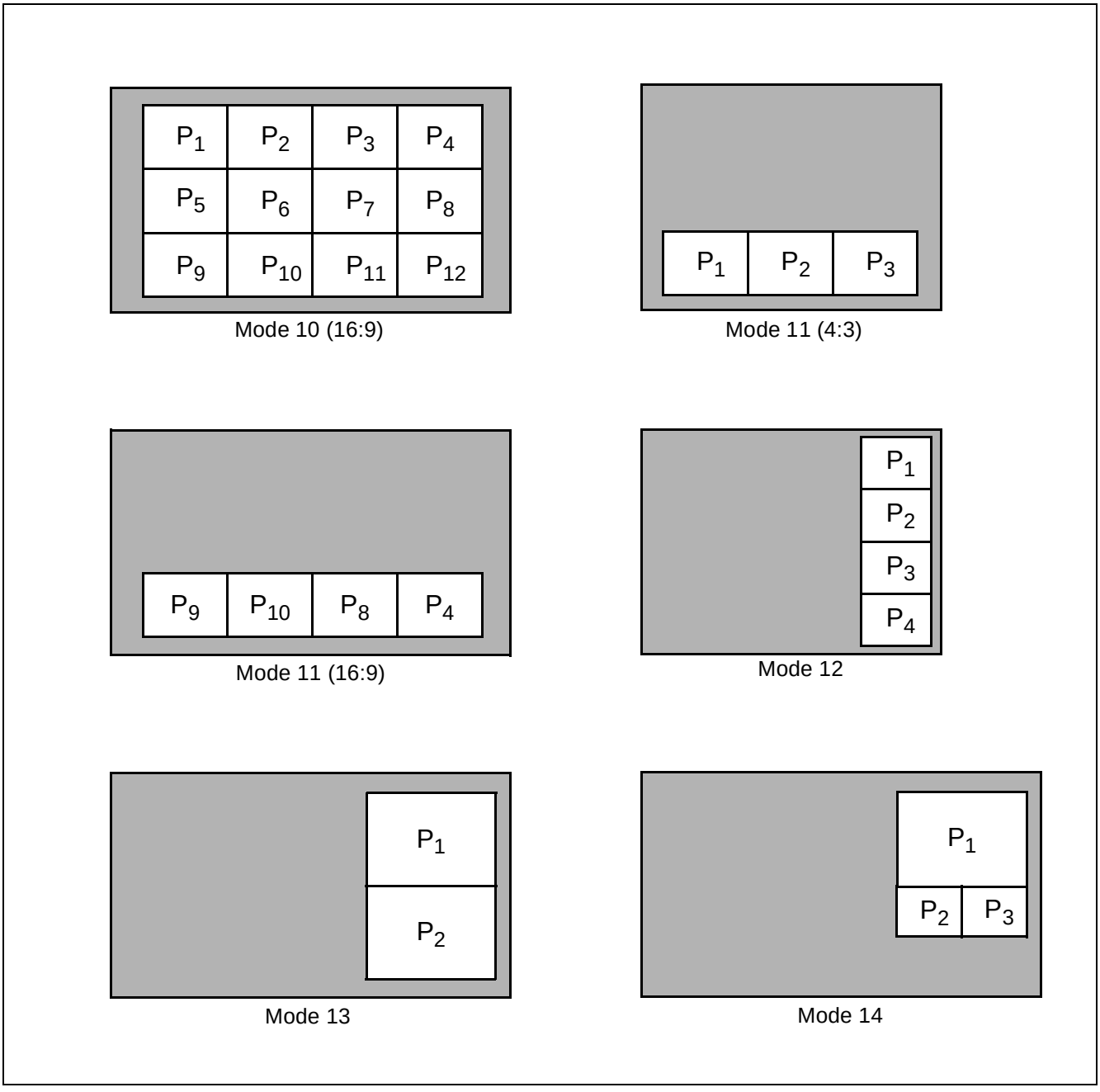


Fig. 2–24: Predefined PIP Modes (continued)

2.12.4. Acquisition and Display Window

The acquisition window defines the picture area of the input active video to be displayed as a inset picture on the screen.

The display window defines the display position of the inset picture(s) on the screen.

The acquisition and display windows are controlled by I^2C parameters HSTR, VSTR, NPIX and NLIN (see Fig. 2–25 and 2–26). They indicate the coordinate of the upper-left corner and the horizontal and vertical size of the active video area. In VPC_{pip} or VPC_{single} mode, these four parameters define the acquisition window in the decimated pixel grid, while in VPC_{main} mode they define the display window.

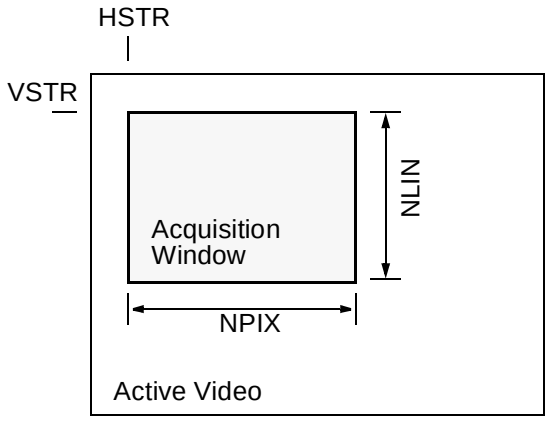


Fig. 2–25: Definition of the acquisition window

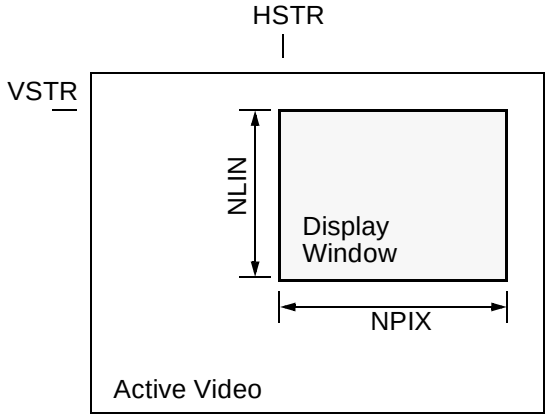


Fig. 2–26: Definition of the display window

2.12.5. Frame and Background Color

Two programmable frame colors COLFR1 and COLFR2 are available to high-light a particular inset picture.

Instead of displaying the main picture it is possible to fill the background with a programmable color COLBGD (set SHOWBGD=1 in the register PIPMODE), e. g. for multi PIP displays on the full screen (see mode 6 and 10).

COLFR1, COLFR2 and COLBGD are 16 bits wide each. Therefore 65536 colors are programmable.

2.12.6. Vertical Shift of the Main Picture

The VPC_{main} mode supports vertical up-shifting of the main picture (e. g. letterbox format) to enable bottom insets (see mode 11). The vertical shift is programmable by VOFFSET.

2.12.7. Free Running Display Mode

In this mode a free running sync raster is generated to guarantee a stable display in critical cases like tuner scan. Therefore the LLC should be disabled (see Table 2–14).

2.12.8. Frame and Field Display Mode

In frame display mode, every field is written into the field memory. In the field display mode every second field is written into the field memory. This configuration is suitable for multi picture insets and freeze mode, since it avoids motion artifacts. On the other hand, the frame display mode guarantees maximum vertical and temporal resolution for animated insets.

In the predefined mode the setting of frame/field mode is done automatically to achieve the best performance.

Table 2–14: Settings for Free-Running Mode

Control bit	Function	VPC_{single}		VPC_{pip}	VPC_{main}	
		write PIP	write main pic.		predef. mode 6, 10	all other modes
LLC_CLKC (bit[11] of FP h'6d)	enable/disable LLC PLL	1	0	0	1	0 or 1[2)]
FLW (bit[15] of I^2C h'28)	enable/disable free-running sync mode	1	0	0	1	0 or 1[2)]
VS_LOCK[1)] (bit[14] of I^2C h'84)	synchronize PIP control to input video/ free-running sync signals	0	0	0	1	0 or 1[2)]

1) VS_LOCK has to be enabled, before enable of FLW.
2) In case of "no input video" for VPC_{main}, it is recommended to enable the free running mode for stable PIP display.

2.12.9. External Field Memory

The requirements of the external field memory are:

– FIFO type access with reset
– write mask function: The increasing of the write address pointer and the over writing of the data should be controlled separately.
– output disable function: tri-state table outputs

For PIP applications, VPC 323xD supports 4:1:1 or 4:2:2 chrominance format. Table 2–15 shows the typical memory size for a 13.5 and 16 MHz system clock application.

Table 2–15: Word length and minimum size of the field memory

Chrominance format	Word length	Memory size	
	[bit]	[word]	[bit]
4:1:1	12	245376	2944512
4:2:2	16	245376	3926016

The following 5 signals are generated by VPC 323xD to control the external field memory:

RSTWR (reset write/read) resets the internal write/ read address pointer to zero.

WE (write enable) is used to enable or disable incrementing of the internal write address pointer.

IE (input enable) is used to enable writing data from the field memory input pins into the memory core, or to disable writing and thereby preserving the previous content of the memory (write mask function).

RE (read enable) is used to enable or disable incrementing the internal read address pointer.

OE (output enable) is used to enable or disable data output to the output pins.

As serial write and serial read clock (**SWCK** and **SRCK**, respectively) of the field memory the line locked clocks LLC1 and/or LLC2 are used.

2.12.10. Field-Buffer-Extension Mode

The field-buffer-extension mode provides a joint lines free display of the inset picture for the single PIP modes. In this mode, two frames (four fields) of the inset picture are stored in the external field memory. The write/read controlling detects timing conflicts causing joint lines artifacts and suppresses these conflicts automatically.

Therefore, the output pin FFRSTW of VPC_{pip} has to be connected to the input pin RSTWPIP (see Fig. 2–22)

For the predefined PIP modes 2…5, the field-buffer-extension mode is enabled by FBEXT=1, in expert mode by FBEXT=1, TWOFB=1 and FRAMOD=1. The function of the I^2C bits TWOFB and FRAMOD is shown in Table 2-24

Table 2–16: Function of the I^2C bits TWOFB and FRAMOD

FBEXT	TWOFB	FRAMOD	Function
x	0	0	use one field buffer, write only one input field of a frame into it
x	0	1	use one field buffer, write both input fields of a frame into it
0	1	x	use two field buffers, write two input fields of a frame alternate into them
1	1	0	use two field buffers, write input fields of a frame alternate into them, update the PIP frame while writing the inset picture
1	1	1	use four field buffers, write input fields of two frame alternate into them, update the PIP frame while writing the inset picture

2.12.11. Double-Windows-Extension Mode

The double-windows-extension mode provides a joint fields free display of the second picture in Double-Window mode. The write/read controlling detects timing conflicts causing joint fields and suppresses these conflicts automatically by delaying the read control signals.

The output pin FFRSTW of VPC_{pip} should be connected to the input pin RSTWPIP (see Fig. 2–22)

3. Serial Interface

3.1. I²C-Bus Interface

Communication between the VPC and the external controller is done via I²C-bus. The VPC has an I²C-bus slave interface and uses I²C clock synchronization to slow down the interface if required. The I²C-bus interface uses one level of subaddress: one I²C-bus address is used to address the IC and a subaddress selects one of the internal registers. For multi VPC 323xD applications the following three I²C-bus chip addresses are selectable via I2CSEL pin:

A6	A5	A4	A3	A2	A1	A0	R/W	I2CSEL
1	0	0	0	1	1	1	1/0	V_{SUP}
1	0	0	0	1	1	0	1/0	VRT
1	0	0	0	1	0	0	1/0	GND

The registers of the VPC have 8 or 16-bit data size; 16-bit registers are accessed by reading/writing two 8-bit data words.

Figure 3–1 shows I²C-bus protocols for read and write operations of the interface; the read operation requires an extra start condition and repetition of the chip address with read command set.

3.2. Control and Status Registers

Table 3–1 gives definitions of the VPC control and status registers. The number of bits indicated for each register in the table is the number of bits implemented in hardware, i.e. a 9-bit register must always be accessed using two data bytes but the 7 MSB will be ‘don’t care’ on write operations and ‘0’ on read operations. Write registers that can be read back are indicated in Table 3–1.

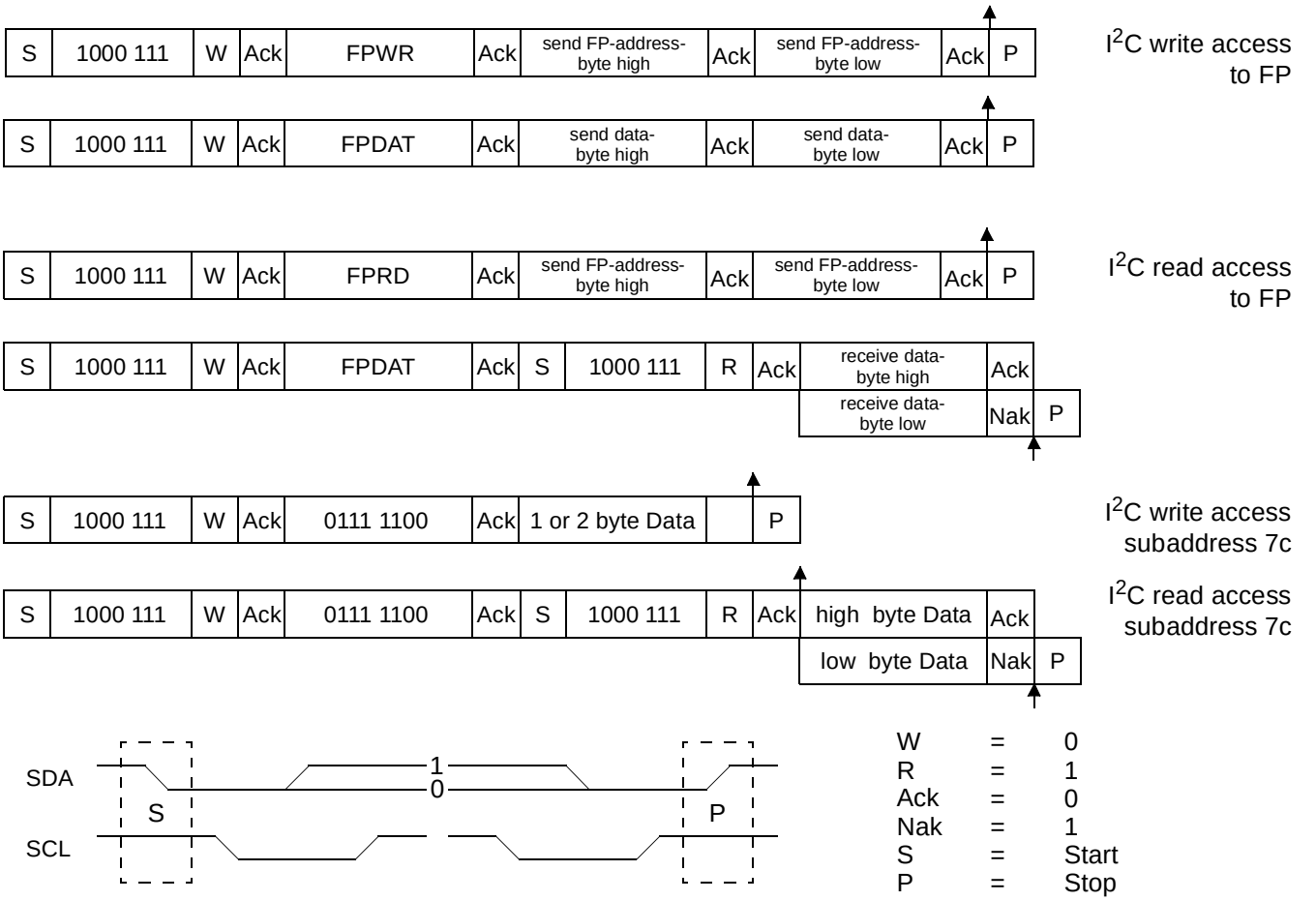


Fig. 3–1: I²C-bus protocols

A hardware reset initializes all control registers to 0. The automatic chip initialization loads a selected set of registers with the default values given in Table 3–1.

The register modes given in Table 3–1 are

– w: write only register
– w/r: write/read data register
– r: read data from VPC
– v: register is latched with vertical sync

The mnemonics used in the Micronas VPC demo software are given in the last column.

Table 3–1: Control and status registers

I²C Sub-address	Number of bits	Mode	Function	Default	Name
			FP Interface		
h'35	8	r	FP status bit [0] write request bit [1] read request bit [2] busy	–	FPSTA
h'36	16	w	bit[8:0] 9-bit FP read address bit[11:9] reserved, set to zero	–	FPRD
h'37	16	w	bit[8:0] 9-bit FP write address bit[11:9] reserved, set to zero	–	FPWR
h'38	16	w/r	bit[11:0] FP data register, reading/writing to this register will autoincrement the FP read/ write address. Only 16 bit of data are transferred per I²C telegram.	–	FPDAT
			Black Line Detector		
h'12	16	w/r	read only register, do not write to this register! After reading, LOWLIN and UPLIN are reset to 127 to start a new measurement. bit[6:0] number of lower black lines bit[7] always 0 bit[14:8] number of upper black lines bit[15] 0/1 normal/black picture	–	BLKLIN LOWLIN UPLIN BLKPIC
			Pin Circuits		
h'1F	16	w/r	SYNC PIN CONTROL: bit[2:0] 0 reserved (set to 0) bit[3] 0/1 push-pull/tri-state for AVO Pin bit[4] 0/1 push-pull/tri-state for other video SYNC Pins bit[5] 0 reserved (set to 0) CLOCK/FIFO PIN CONTROL: bit[6] 0/1 push-pull/tri-state for LLC1 bit[7] 0/1 push-pull/tri-state for LLC2 bit[8] 0/1 push-pull/tri-state for CLK20 bit[9] 0/1 push-pull/tri-state for FIFO control pins LUMA/CHROMA DATA PIN (LB[7:0], CB[7:0]) CONTROL: bit[10] 0/1 **tri-state**/push-pull for Chroma Data pins bit[11] 0/1 **tri-state**/push-pull for Luma Data pins bit[15:12] reserved (set to 0)	 0 0 0 0 0 0 0 0 0 0 0	TRPAD AVODIS SNCDIS LLC1DIS LLC2DIS CLK20DIS FFSNCDIS CDIS YDIS
h'20	8	w/r	SYNC GENERATOR CONTROL: bit[1:0] 00 AVO and active Y/C data at same time 01 AVO precedes Y/C data one clock cycle 10 AVO precedes Y/C data two clock cycles 11 AVO precedes Y/C data three clock cycles bit[2] 0/1 positive/negative polarity for HS signal bit[3] 0/1 positive/negative polarity for HC signal bit[4] 0/1 positive/negative polarity for AVO signal bit[5] 0/1 positive/negative polarity for VS signal bit[6] 0 reserved (set to 0) bit[7] 0/1 positive/negative polarity for INTLC signal	 0 0 0 0 0 0 0	SYNCMODE AVOPRE HSINV HCINV AVOINV VSINV INTLCINV

Table 3–1: Control and status registers

I²C Sub-address	Number of bits	Mode	Function	Default	Name
h'23	16	w/r	OUTPUT STRENGTH:		OUTSTR
			bit[3:0] 0..15 output pin strength (0 = strong, 15 = weak)	0	PADSTR
			bit[9:4] address of output pin	0	PADADD
			32 FIFO control pins FFIE, FFOE, FFWR, FFRE and FFRSTWR		
			33 SYNC pins AVO, HS, HC, INTERLACE,VS		
			bit[10] 0/1 read/write output strength	0	PADWR
			bit[15:11] reserved (set to 0)	0	
h'30	8	w/r	V-SYNC DELAY CONTROL:		VSDEL
			bit[7:0] VS delay (8 LLC clock cycles per LSB)	0	VSDEL
656 Interface					
h'24	8	w/r	656 OUTPUT INTERFACE		OUT656
			bit [0] 1 disable hor. & vert. blanking of invalid data in 656 mode	0	DBLNK
			bit [1] 0 use vertical window as VFLAG	0	VSMODE
			1 use vsync as VFLAG		
			bit [2] enable suppression of 656-headers during invalid video lines	0	HSUP
			bit [3] enable ITU-656 output format	0	656enable
			bit [4] 0/1 LLC1/LLC2 used as reference clock	0	DBLCLK
			bit [5] 0/1 output mode: DIGIT 3000 / LLC	1	OMODE
Sync Generator					
h'21	16	w/r	LINE LENGTH:		
			bit[10:0] LINE LENGTH register In LLC mode, this register defines the cycle of the sync counter which generates the SYNC pulses. In LLC mode, the synccounter counts from 0 to LINE LENGTH, so this register has to be set to "number of pixels per line –1". In DIGIT3000 mode, LINE LENGTH has to be set to 1295 for correct adjustment of vertical signals.	1295	LINLEN
			bit[15:11] reserved (set to 0)		
h'26	16	w/r	HC START:		
			bit[10:0] HC START defines the beginning of the HC signal in respect to the value of the sync counter.	50	HCSTRT
			bit[13:11] reserved (set to 0)		
			bit[14] 0/1 select pos./neg. polarity of HSYA/VSYA	0	HVSYAPOL
			bit[15] 0/1 dis-/enable Front-End horizontal and vertical sync outputs HSYA/VSYA	0	HVSYA
h'27	16	w/r	bit[10:0] HC STOP defines the end of the HC signal in respect to the value of the sync counter.	800	HCSTOP
			bit[15:11] reserved (set to 0)		

Table 3–1: Control and status registers

I²C Sub-address	Number of bits	Mode	Function	Default	Name
h'28	16	w/r	AVO START:		
			bit[10:0] AVO START defines the beginning of the AVO signal in respect to the value of the sync counter.	60	AVSTRT
			bit[11] reserved (set to 0)		
			bit[12] 0/1 dis-/enable suppression of AVO during VBI and invalid video lines	0	AVOGATE
			bit[13] 0/1 vertical standard for flywheel (312/262 lines) used if FLW is set	0	FLWSTD
			bit[14] 0/1 disable interlace for flywheel		DIS_INTL
			bit[15] 0/1 enable vertical free run mode (flywheel)	0	FLW
h'29	16	w/r	AVO STOP:		
			bit[10:0] AVO STOP defines the end of the AVO signal in respect to the value of the sync counter.	0	AVSTOP
			bit[15:11] reserved for test picture generation (set to 0 in normal operation)		
			bit[11] 0/1 disable/enable test pattern generator	0	COLBAREN
			bit[13:12] luma output mode:	0	LMODE
			00 Y = ramp (240 ... 17)		
			01 Y = 16		
			10 Y = 90		
			11 Y = 240		
			bit[14] 0/1 chroma output: 422/411 mode	0	M411
			bit[15] 0/1 chroma output: pseudo color bar/zero if LMODE = 0	0	CMODE
h'22	16	w/r	NEWLINE:		
			bit[10:0] NEWLINE defines the readout start of the next line in respect to the value of the sync counter. The value of this register must be greater than 34 for correct operation and should be identical to AVOSTART (recommended). In case of 1H-bypass mode for scaler block, NEWLINE has no function.	50	NEWLIN
			bit[15:11] reserved (set to 0)		

Table 3–1: Control and status registers

I²C Sub-address	Number of bits	Mode	Function	Default	Name
PIP Control					
h'84	16	w/r	VPC MODE: bit[0] 0/1 dis-/enable field memory control for PIP bit[1] 0/1 double/single VPC application bit[2] 0/1 select VPC_{pip}/VPC_{main} mode bit[3] 0/1 4:3/16:9 screen bit[4] 0/1 13.5/16 MHz output pixel rate bit[5] 0/1 vertical PIP window size is based on a 625/525 line video bit[7:6] field memory type 00 reserved 01 PHILIPS SAA 4955TJ 10 reserved 11 other (OKI MSM5412222, ...) *bit[11:8] are evaluated only, if bit[7:6]=11* bit[8] 0/1 delay the video output compared to WE for 0/1 LLC1 clock, if DBLCLK=0 0/1 LLC2 clock, if DBLCLK=1 bit[9] 0/1 pos/neg polarity for WE and RE signals bit[10] 0/1 pos/neg polarity for IE and OE signals bit[11] 0/1 pos/neg polarity for RSTWR signal bit[12] reserved (set to 0) bit[13] 0/1 vertical PIP position synchronized by input video/vertical sync in case of no video input, FLW=0 and LLC PLL disabled. For VPC_{main} combined with a feature-box without read/write mask only! bit[14] 0/1 vertical PIP position synchronized by input video/free running sync raster FLW bit[15] reserved (set to 0) This register is updated when the PIPOPER register is written.	0	VPCMODE ENA_PIP SINGVPC MAINVPC F16TO9 F16MHZ W525 FIFOTYPE VIDEODEL WEREINV IEOEINV RSTWRINV AV_LOCK VS_LOCK

Table 3–1: Control and status registers

I²C Sub-address	Number of bits	Mode	Function	Default	Name
h'85	16	w/r	PIP MODE: bit[3:0] 0 - 14 select predefined PIP mode 15 select expert mode *bit[5:4] are used for expert mode only* bit[4] 0/1 write one/both input field(s) of a frame into the field buffer in case TWOFB=0 bit[5] 0/1 use one/two field buffer(s) **Note:** please see 2.12.10 for detailed description of FRAMOD and TWOFB in field-buffer-extension mode bit[6] 0/1 show video/the background color in the picture *bit[13:7] are used for VPC_{main} only* bit[7] 0/1 dis-/enable the vertical up-shifting of the main picture bit[13:8] 0...62 number of lines for vertical up-shift bit[14] 0/1 dis-/enable the field-buffer-extension mode, only used for VPC_{pip} and VPC_{main} in single PIP Modes bif[15] 0/1 dis-/enable the double-window-extension mode, only used for VPC_{main} in predefined mode 1 This register is updated when the PIPOPER register is written.	0	PIPMODE MODSEL FRAMOD TWOFB SHOWBGD VSHIFT VOFFSET FBEXT DWEXT

Table 3–1: Control and status registers

I²C Sub-address	Number of bits	Mode	Function	Default	Name
h'83	8	w/r	PIP OPERATION: *For VPC_{pip} or VPC_{single}:* bit[1:0] the number of the inset picture to be accessed in the x-direction bit[3:2] the number of the inset picture to be accessed in the y-direction bit[6:4] 000 start to write the inset picture with a frame 001 stop writing 010 fill the frame with the color COLFR1 011 fill the frame with the color COLFR2 100 fill the inset picture with a frame using the color COLBGD 101 fill the inset picture w/o a frame using the color COLBGD 110 start to write the inset picture w/o a frame 111 write the main picture (VPC_{single}only) *For VPC_{main}:* bit[3:0] reserved set to 0 bit[6:4] 000 start to display PIP 001 stop to display PIP 010 enable still main picture[1)] 011 disable still main picture[1)] 100 enable still PIP[1)] 101 disable still PIP[1)] other reserved set to 0 bit[7] 0/1 processed/new command flag, normally write 1. After the new PIP setting takes effect, this bit is set to 0 to indicate operation complete. 1) This Mode is available only in combination with a FIFO type field memory (see Section 2.12.9.) for scan rate conversion.	0	PIPOPER NSPX NSPY WRPIC WRSTOP WRFRCOL1 WRFRCOL2 WRBGD WRBGDNF WRPICNF WRMAIN DISSTART DISSTOP STMAINON STMAINOFF STPIPON STPIPOFF NEWCMD
h'80	16	w/r	BACKGROUND COLOR: in binary offset bit[[4:0] bit b_7 to b_3 of the chrominance component C_R bit[9:5] bit b_7 to b_3 of the chrominance component C_B bit[15:10] bit b_7 to b_2 of the luminance component Y (all other bits of YC_BC_R are set to 0) This register is updated when the PIPOPER register is written.	0	COLBGD
h'81	16	w/r	FRAME COLOR 1: in binary offset *Only used for VPC_{pip} or VPC_{single}:* bit[[4:0] bit b_7 to b_3 of the chrominance component C_R bit[9:5] bit b_7 to b_3 of the chrominance component C_B bit[15:10] bit b_7 to b_2 of the luminance component Y (all other bits of YC_BC_R are set to 0) This register is updated when the PIPOPER register is written.	h'3e0	COLFR1

Table 3–1: Control and status registers

I²C Sub-address	Number of bits	Mode	Function	Default	Name
h'82	16	w/r	FRAME COLOR 2: in binary offset *only used for VPC_{pip} or VPC_{single}:* bit[[4:0] bit b_7 to b_3 of the chrominance component C_R bit[9:5] bit b_7 to b_3 of the chrominance component C_B bit[15:10] bit b_7 to b_2 of the luminance component Y (all other bits of YC_BC_R are set to 0) This register is updated when the PIPOPER register is written.	h'501f	COLFR2
h'86	16	w/r	LINE OFFSET: *Only used for VPC_{pip} or VPC_{single}:* bit[8:0] line offset of the upper-left corner of the inset picture with NSPX=0 and NSPY=0 in the display window bit[9] 0/1 use the internal default/external setting via bit[8:0] bit[15:10] reserved (set to 0) This register is updated when the PIPOPER register is written.	0	LINOFFS
h'89	16	w/r	PIXEL OFFSET: *Only used for VPC_{pip} or VPC_{single}:* bit[7:0] quarter of the pixel offset of the upper-left corner of the inset picture with NSPX=0 and NSPY=0 in the display window bit[8] 0/1 use the internal default/external setting via bit[7:0] bit[15:9] reserved (set to 0) This register is updated when the PIPOPER register is written.	0	PIXOFFS

Table 3–1: Control and status registers

I²C Sub-address	Number of bits	Mode	Function	Default	Name
h'87	16	w/r	VERTICAL START: bit[8:0] *For VPC_{pip} and VPC_{single}:* vertical start of the active video segment to be used as a inset picture *For VPC_{main} :* vertical start of the inset picture(s) in the main picture **Exception:** bit[8:0] 0...3 *For VPC_{main} in predefined mode 1 and DWEXT=1:* length (in lines) of the FIFO read-write conflict interval 0 length = 1 1 length = 1 2 length = 2 3 length = 3 =1 for PHILIPS SAA 4955TJ, OKI MSM541222,... bit[9] 0/1 use the internal default/external setting via bit[8:0] *Only used for predefined mode 1 and DWEXT=1:* bit[11:10] start position (in line number) of the the FIFO read-write conflict interval 00 PHILIPS SAA 4955TJ 01 OKI MSM541222,... bit[15:12] defines max. drift (in LLC1 clocks) between the rstwr impulses of *VPC_{pip} and VPC_{main}*, where the double-window-extension mode is active.	0 0 0	VSTR VSTR_JF DIFLIM
h'8a	16	w/r	HORIZONTAL START: bit[7:0] *For VPC_{pip} and VPC_{single}:* horizontal start of the active video segment to be used as a inset picture *For VPC_{main}:* horizontal start of the inset picture(s) in the main picture In both cases HSTR is given by the number of 4-pixel-groups. bit[8] 0/1 use the internal default/external setting via bit[7:0] bit[15:9] reserved (set to 0)	0	HSTR
h'88	16	w/r	NUMBER OF LINES: *Only used in the expert modes:* bit[8:0] *For VPC_{pip} and VPC_{single}:* number of lines of the active video segment to be used as a inset picture *For VPC_{main}:* number of lines of the inset picture(s) bit[15:9] reserved (set to 0) This register is updated when the PIPOPER register is written.	0	NLIN

Table 3–1: Control and status registers

I²C Sub-address	Number of bits	Mode	Function	Default	Name
h'8b	8	w/r	NUMBER OF PIXEL PER LINE: *Only used in the expert modes:* bit[7:0] *For VPC_{pip} and VPC_{single}:* quarter of the number of pixels per line in the active video segment to be used as a inset picture *For VPC_{main}:* quarter of the number of pixels per line of the inset picture(s) This register is updated when the PIPOPER register is written.	0	NPIX
h'8c	16	w/r	NUMBER OF PIXEL PER LINE IN THE FIELD BUFFER(S): bit[7:0] quarter of the number of allocated pixels per line in the field buffer(s) bit[8] 0/1 use the internal default/external setting via bit[7:0] (must be set in the expert mode, optional in the predefined modes) bit[15:9] reserved (set to 0) This register is updated when the PIPOPER register is written.	0	NPFB
h'8d-h'8f			reserved, don't write		
CIP Control					
h'90	16	w/r	SATURATION OF THE RGB/YC_rC_b COMPONENT INPUT: bit[5:0] saturation Cb(0..63) bit[11:6] saturation Cr(0..63) bit[15:12] reserved (set to 0)	 23 29	CIPSAT SATCb SATCr
h'91	8	w/r	TINT CONTROL OF THE RGB/YUV COMPONENT INPUT: bit[5:0] tint (–20..+20 in degrees) bit[7:6] reserved (set to 0)	 0	 CIPTNT
h'92	16	w/r	BRIGHTNESS OF THE RGB/YUV COMPONENT INPUT: bit[7:0] brightness (–128..+127) CONTRAST OF THE RGB/YUV COMPONENT INPUT: bit[13:8] contrast (0..63) bit[15:14] reserved (set to 0)	 68 27	CIPBRCT CIPBR CIPCT
h'94	8	w/r	SOFTMIXER CONTROL: bit[0] 0/1 rgb/main video delay (0:normal 1:dynamic) bit[1] 0/1 linear (0)/nonlinear(1) mixer select bit[7:4] fastblank gain (–7 .. +7) bit[3:2] reserved (set to 0)	 0 0 –1	CIPMIX1 RGBDLY SELLIN FBGAIN
h'95	8	w/r	SOFTMIXER CONTROL: bit[5:0] fastblank offset correction (0..63) (fb –> fb–FBOFFS) bit[7:6] fastblank mode: x0 force rgb to cip out (equ. fb=0) 01 normal mode (fb active) 11 force main yuv to cip out (equ. fb=64)	 32 11	CIPMIX2 FBOFFS FBMODE

Table 3–1: Control and status registers

I²C Sub-address	Number of bits	Mode	Function	Default	Name
h'96	8	w/r	ADC RANGE : bit[0] reserved (set to 0) bit[1] 0/1 0/+3dB extended ADC range INPUT PORT SELECT : bit[2] 0/1 1/2 input port select SOFTMIXER CONTROL: bit[5] 0/1 clamp fb to a programable value (0:normal 1: fb=31–FBOFFS) bit[6] 0/1 bypass chroma 444–>422 decimation filter RGB/YUV SELECT: bit[7] 0/1 rgb/yuv input select bit[4:3] reserved (set to 0)	 0 0 0 1 0	CIPCNTL XAR RGBSEL FBCLP CIPCFBY YUV
h'97	8	r	FB MONITOR: bit[0] 0/1 set by fb high, reset by reg. read and fb low bit[1] 0/1 set by fb falling edge, reset by reg. read bit[2] 0/1 set by fb rising edge, reset by reg. read bit[3] 0/1 fb status at register read CLIP DETECTOR: bit[4] 0/1 rgb/yuv input clip detect, reset by read	 – – – – –	CIPMON FBHIGH FBFALL FBRISE FBSTAT CLIPD
Hardware ID					
h'9f	16	r	Hardware version number bit[7:0] 0/255 hardware id 1=A, 2=B aso. bit[11:8] 0/3 product code 0 VPC32x0D 1 VPC32x1D 2 VPC32x2D 3 VPC32x3D bit[15:12] 0/15 product code 3 VPC323xD 100Hz version 4 VPC324xD 50Hz version	read only	

Table 3–2: Control Registers of the Fast Processor

– default values are initialized at reset
– * indicates: register is initialized according to the current standard when SDT register is changed.

FP Sub-address	Function	Default	Name
	Standard Selection		
h'20	Standard select:		SDT
	bit[2:0] standard	0	
	0 PAL B,G,H,I (50 Hz) 4.433618		PAL
	1 NTSC M (60 Hz) 3.579545		NTSC
	2 SECAM (50 Hz) 4.286		SECAM
	3 NTSC44 (60 Hz) 4.433618		NTSC44
	4 PAL M (60 Hz) 3.575611		PALM
	5 PAL N (50 Hz) 3.582056		PALN
	6 PAL 60 (60 Hz) 4.433618		PAL60
	7 NTSC COMB (60 Hz) 3.579545		NTSCC
	bit[3] 0/1 MOD standard modifier PAL modified to simple PAL NTSC modified to compensated NTSC SECAM modified to monochrome 625 NTSCC modified to monochrome 525	0	SDTMOD
	bit[4] 0/1 PAL+ mode off/on	0	PALPLUS
	bit[5] 0/1 4-H COMB mode	0	COMB
	bit[6] 0/1 S-VHS mode: The S-VHS/COMB bits allow the following modes: 00 composite input signal 01 comb filter active 10 S-VHS input signal 11 CVBS mode (composite input signal, no luma notch)	0	SVHS
	Option bits allow to suppress parts of the initialization; this can be used for color standard search:		
	bit[7] no hpll setup bit[8] no vertical setup bit[9] no acc setup bit[10] 4-H comb filter setup only	0	SDTOPT
	bit[11] status bit, normally write 0. After the FP has switched to a new standard, this bit is set to 1 to indicate operation complete. Standard is automatically initialized when the insel register is written.		

FP Sub-address	Function	Default	Name
h’148	Enable automatic standard recognition bit[0] 0/1 PAL B,G,H,I (50 Hz) 4.433618 bit[1] 0/1 NTSC M (60 Hz) 3.579545 bit[2] 0/1 SECAM (50 Hz) 4.286 bit[3] 0/1 NTSC44 (60 Hz) 4.433618 bit[4] 0/1 PAL M (60 Hz) 3.575611 bit[5] 0/1 PAL N (50 Hz) 3.582056 bit[6] 0/1 PAL 60 (60 Hz) 4.433618 bit[10:7] reserved set to 0 bit[11] 1 reset status information bit ‘switch’ in register ‘asr_status’ (cleared automatically) 0: disable recognition; 1: enable recognition Note: For correct operation don’t change FP reg. 20h and 21h, while ASR is enabled!	0	ASR_ENABLE
h’14e	Status of automatic standard recognition bit[0] 1 error of the vertical standard (neither 50 nor 60 Hz) bit[1] 1 detected standard is disabled bit[2] 1 search active bit[3] 1 search terminated, but failed bit[4] 1 no color found bit[5] 1 standard has been switched (since last reset of this flag with bit[11] of asr_enable) bit[4:0] 00000 all ok 00001 search not started, because vwin error detected (no input or SECAM L) 00010 search not started, because detected vert. standard not enabled 0x1x0 search started and still active 01x00 search failed (found standard not correct) 01x10 search failed, (detected color standard not enabled) 10100 no color found (monochrome input or switch betw. CVBS/SVHS necessary)	0	ASR_STATUS VWINERR DISABLED BUSY FAILED NOCOLOR SWITCH

FP Sub-address	Function	Default	Name
h'21	Input select: writing to this register will also initialize the standard		INSEL
	bit[1:0] luma selector	0	VIS
	00 VIN3		
	01 VIN2		
	10 VIN1		
	11 VIN4		
	bit[2] chroma selector	1	CIS
	0/1 VIN1/CIN		
	bit[4:3] IF compensation	0	IFC
	00 off		
	01 6 dB/Okt		
	10 12 dB/Oct		
	11 10 dB/MHz only for SECAM		
	bit[6:5] chroma bandwidth selector	2	CBW
	00 narrow		
	01 normal		
	10 broad		
	11 wide		
	bit[7] 0/1 adaptive/fixed SECAM notch filter	0	FNTCH
	bit[8] 0/1 enable luma lowpass filter	0	LOWP
	bit[10:9] hpll speed	3	HPLLMD
	00 no change		
	01 terrestrial		
	10 vcr		
	11 mixed		
	bit[11] status bit, write 0, this bit is set to 1 to indicate operation complete.		
h'22	picture start position: This register sets the start point of active video and can be used e.g. for panning. The setting is updated when 'sdt' register is updated or when the scaler mode register 'scmode' is written.	0	SFIF
h'23	luma/chroma delay adjust. bit[5:0] reserved, set to zero bit[11:6] luma delay in clocks, allowed range is +1 ... –7 The setting is updated when 'sdt' register is updated.	0	LDLY
h'29	helper delay register (PAL+ mode only) bit[11:0] delay adjust for helper lines adjustable from –96...96, 1 step corresponds to 1/32 clock	0	HLP_DLY
h'27	component input to main video input delay matching bit[5:0] reserved, set to zero bit[11:6] delay adjust cip/main 0...18 clocks, 9=matched The setting is updated when 'sdt' register is updated.	9	CIP_MATCH
h'2f	VGA mode select, pull-in range is limited to 2%		VGA_C
	bit[1:0] 0 31.5 kHz		
	1 35.2 kHz	0	VGAMODE
	2 37.9 kHz		
	3 reserved		
	is set to 0 by FP if VGA = 0		
	bit[10] 0/1 disable/enable VGA mode	0	VGA
	bit[11] status bit, write 0, this bit is set to 1 to indicate operation complete.		

FP Sub-address	Function	Default	Name
	Comb Filter		
h'28	comb filter control register bit[1:0] notch filter select 00 flat frequency characteristic 01 min. peaked 10 med. peaked 11 max. peaked bit[3:2] diagonal dot reduction 00 min. reduction ... 11 max. reduction bit[4:5] horizontal difference gain 00 min. gain ... 11 max. gain bit[7:6] vertical difference gain 00 max. gain ... 11 min. gain bit[11:8] vertical peaking gain 0 no vertical peaking... 15 max. vertical peaking	h'e7 3 1 2 3 0	COMB_UC NOSEL DDR HDG VDG VPK
h'55	comb filter test register bit[1:0] reserved, set ot 0 bit[2] 0/1 disable/enable vertical peaking DC rejection filter bit[3] 0/1 disable/enable vertical peaking coring bit[11:4] reserved, set to 0	 0 0	CMB_TST DCR COR
	Color Processing		
h'30	Saturation control bit[11:0] 0...4094 (2070 corresponds to 100% saturation) 4095 reserved	2070	ACC_SAT
h'17a	bit[10:0] 0...2047 CR-attenuation or PAL+ Helper gain adjust (1591 corresponds to 100% helper gain 2047 corresponds to 100% CR gain) bit[11] 0 select Helper gain (CR-attenuation disabled) 1 select CR-attenuation	1591 0	CR_ATT CR_ATT_ENA
h'17d	ACC multiplier value for PAL+ Helper Signal b[10:0] eeemmmmmmmm m * 2^{-e}	1280	ACCH
h'39	bit[10:0] 0..2047 amplitude killer level (0:killer disabled)	25	KILVL
h'3a	amplitude killer hysteresis	5	KILHY
h'16c	automatic helper disable for nonstandard signals bit[11:0] 0 automatic function disabled bit[1:0] 01 enable bit[11:2] 1..50 number of fields to switch on helper signal	0	HLPDIS
h'dc	NTSC tint angle, ±512 = ±π/4	0	TINT

FP Sub-address	Function	Default	Name
	DVCO		
h'f8	crystal oscillator center frequency adjust, –2048 ... 2047	–720	DVCO
h'f9	crystal oscillator center frequency adjustment value for line-lock mode, true adjust value is DVCO – ADJUST. For factory crystal alignment, using standard video signal: disable autolock mode, set DVCO = 0, set lock mode, read crystal offset from ADJUST register and use negative value for initial center frequency adjustment via DVCO.	read only	ADJUST
h'f7	crystal oscillator line-locked mode, lock command/status write: 100 enable lock 0 disable lock read: 0 unlocked >2047 locked	0	XLCK
h'b5	crystal oscillator line-locked mode, autolock feature. If autolock is enabled, crystal oscillator locking is started automatically. bit[11:0] threshold, 0:autolock off	400	AUTOLCK

FP Sub-address	Function	Default	Name
	FP Status Register		
h'12	general purpose control bits bit[2:0] reserved, do not change bit[3] vertical standard force bit[8:4] reserved, do not change bit[9] disable flywheel interlace bit[11:10] reserved, do not change to enable vertical free run mode set vfrc to 1 and dflw to 0	 0 1	 VFRC DFLW
h'13	standard recognition status bit[0] 1 vertical lock bit[1] 1 horizontally locked bit[2] 1 no signal detected bit[3] 1 color amplitude killer active bit[4] 1 disable amplitude killer bit[5] 1 color ident killer active bit[6] 1 disable ident killer bit[7] 1 interlace detected bit[8] 1 no vertical sync detection bit[9] 1 spurious vertical sync detection bit[12:10] reserved	–	ASR
h'14	input noise level, available only for VPC 323xC	read only	NOISE
h'cb	number of lines per field, P/S: 312, N: 262	read only	NLPF
h'15	vertical field counter, incremented per field	read only	VCNT
h'74	measured sync amplitude value, nominal: 768 (PAL), 732 (NTSC)	read only	SAMPL
h'36	measured burst amplitude	read only	BAMPL
h'f0	firmware version number bit[7:0] internal revision number bit[11:8] firmware release hardware id see I^2C register h'9f	read only	–
h'170	status of macrovision detection bit[0] AGC pulse detected bit[1] pseudo sync detected	read only	MCV_STATUS

FP Sub-address	Function	Default	Name
	Scaler Control Register		
h'40	scaler mode register bit[1:0] scaler mode 0 linear scaling mode 1 nonlinear scaling mode, 'panorama' 2 nonlinear scaling mode, 'waterglass' 3 reserved bit[2] reserved, set to 0 bit[3] color mode select 0/1 4:2:2 mode / 4:1:1 mode bit[4] scaler bypass bit[5] reserved, set to 0 bit[6] luma output format 0 ITU-R luma output format (16–240) 1 CVBS output format bit[7] chroma output format 0/1 ITU-R (offset binary) / signed bit[10:8] reserved, set to 0 bit[11] 0 scaler update command, when the registers are updated the bit is set to 1	0	SCMODE PANO S411 BYE YOF COF
h'41	pip control register bit[1:0] horizontal downsampling 0 no downsampling 1 downsampling by 2 2 downsampling by 4 3 downsampling by 8 bit[3:2] vertical compression for PIP 0 compression by 2 1 compression by 3 2 compression by 4 3 compression by 6 bit[4] vertical filter enable bit[5] interlace offset for vertical filter (NTSC mode only) 0 start in line 283 of 2nd field (ITUR 656 spec) 1 start in line 282 of 2nd field (NTSC spec) this register is updated when the scaler mode register is written	0	SCPIP DOWNSAMP PIPSIZE PIPE INTERLACE_OFF
h'42	active video length for 1H-FIFO bit[11:0] length in pixels D3000 mode (1296/h)1080 LLC mode (864/h)720 this register is updated when the scaler mode register is written	1080	FFLIM
h'43	scaler1 coefficient: This scaler compresses the signal. For compression by a factor c, the value c*1024 is required. bit[11:0] allowed values from 1024... 4095 This register is updated when the scaler mode register is written.	1024	SCINC1
h'44	scaler2 coefficient: This scaler expands the signal. For expansion by a factor c, the value 1/c*1024 is required. bit[11:0] allowed values from 256..1024 This register is updated when the scaler mode register is written.	1024	SCINC2
h'45	scaler1/2 nonlinear scaling coefficient This register is updated when the scaler mode register is written.	0	SCINC

FP Sub-address	Function	Default	Name
h'47 – h'4b	scaler1 window controls, see table 5 12-bit registers for control of the nonlinear scaling This register is updated when the scaler mode register is written.	0	SCW1_0 – 4
h'4c – h'50	scaler2 window controls, see table 5 12-bit registers for control of the nonlinear scaling This register is updated when the scaler mode register is written.	0	SCW2_0 – 4
h'52	brightness register bit[7:0] luma brightness –128...127 ITU-R output format: 16 CVBS output format: –4 bit[9:8] horizontal lowpass filter for Y/C 0 bypass 1 filter 1 2 filter 2 3 filter 3 bit[10] horizontal lowpass filter for highresolution chroma 0/1 bypass/filter enabled bit[11] 0/1 dis-/enable luma limited to 16 this register is updated when the scaler mode register is written	16 16 0 0 0	SCBRI BR LPF2 CBW2 YLIM16
h'53	contrast register bit[5:0] luma contrast 0..63 ITU-R output format: 48 bit[7:6] horizontal peaking filter 0 narrow 1 med 2 broad bit[10:8] peaking gain 0 no peaking... 7 max. peaking bit[11] peaking filter coring enable 0/1 bypass/coring enabled this register is updated when the scaler mode register is written	48 48 0 0 0	SCCT CT PFS PK PKCOR
LLC Control Register			
h'65	vertical freeze start freeze llc pll for llc_start < line number < llc_stop bit[11:0] allowed values from –156...+156	–10	LLC_START
h'66	vertical freeze stop freeze llc pll for llc_start < line number < llc_stop bit[11:0] allowed values from –156...+156	4	LLC_STOP
h'69 h'6a	20 bit llc clock center frequency 12.27 MHz –79437 = h'FEC9B2 13.5 MHz 174763 = h'02AAAB 14.75 MHz 194181 = h'02F685 16 MHz –135927 = h'FDED08 18 MHz 174763 = h'02AAAB	42 = h'02A 2731 = h'AAB	LLC_CLOCKH LLC_CLOCKL

FP Sub-address	Function	Default	Name
h'61	pll frequency limiter, 8% 12.27 MHz 30 13.5 MHz 54 14.75 MHz 62 16 MHz 48 18 MHz 54	54	LLC_DFLIMIT
h'6d	llc clock generator control word bit[5:0] hardware register shadow llc_clkc = 5Æ12.27 MHz llc_clkc = 5Æ13.5 MHz llc_clkc = 35Æ14.75 MHz llc_clkc = 3Æ16 MHz llc_clkc = 3Æ18 MHz bit[10:6] reserved bit[11] 0/1 enable/disable llc pll	2053	LLC_CLKC

3.2.1. Calculation of Vertical and East-West Deflection Coefficients

In Table 3–3 the formula for the calculation of the deflection initialization parameters from the polynominal coefficients a,b,c,d,e is given for the vertical and East-West deflection. Let the polynomial be

$$P \div a + b(x - 0.5) + c(x - 0.5)^2 + d(x - 0.5)^3 + e(x - 0.5)^4$$

The initialization values for the accumulators a0..a3 for vertical deflection and a0..a4 for East-West deflection are 12-bit values. The coefficients that should be used to calculate the initialization values for different field frequencies are given below, the values must be scaled by 128, i.e. the value for a0 of the 50 Hz vertical deflection is

$$a0 = (a \cdot 128 - b \cdot 1365.3 + c \cdot 682.7 - d \cdot 682.7) \div 128$$

3.2.2. Scaler Adjustment

In case of linear scaling, most of the scaler registers need not be set. Only the scaler mode, active video length, and the fixed scaler increments (scinc1/scinc2) must be written.

The adjustment of the scaler for nonlinear scaling modes should use the parameters given in table 3–4. An example for ‘panorama vision’ mode with 13.5 MHz line-locked clock is depicted in Fig. 3–2. The figure shows the scaling of the input signal and the variation of the scaling factor during the active video line. The scaling factor starts below 1, i.e. for the borders the video data is expanded by scaler 2. The scaling factor becomes one and compression scaling is done by scaler 1. When the picture center is reached, the scaling factor is held constant. At the second border the scaler increment is inverted and the scaling factor changes back symmetrically. The picture indicates the function of the scaler increments and the scaler window parameters. The correct adjustment requires that pixel counts for the respective windows are always in number of output samples of scaler 1 or 2.

Table 3–3: Tables for the Calculation of Initialization values for Vertical Sawtooth and East-West Parabola

Vertical Deflection 50 Hz				
	a	**b**	**c**	**d**
a0	128	–1365.3	+682.7	–682.7
a1		899.6	–904.3	+1363.4
a2			296.4	–898.4
a3				585.9
Vertical Deflection 60 Hz				
	a	**b**	**c**	**d**
a0	128	–1365.3	+682.7	–682.7
a1		1083.5	–1090.2	+1645.5
a2			429.9	–1305.8
a3				1023.5

East-West Deflection 50 Hz					
	a	**b**	**c**	**d**	**e**
a0	128	–341.3	1365.3	–85.3	341.3
a1		111.9	–899.6	84.8	–454.5
a2			586.8	–111.1	898.3
a3				72.1	–1171.7
a4					756.5
East-West Deflection 60 Hz					
	a	**b**	**c**	**d**	**e**
a0	128	–341.3	1365.3	–85.3	341.3
a1		134.6	–1083.5	102.2	–548.4
a2			849.3	–161.2	1305.5
a3				125.6	–2046.6
a4					1584.8

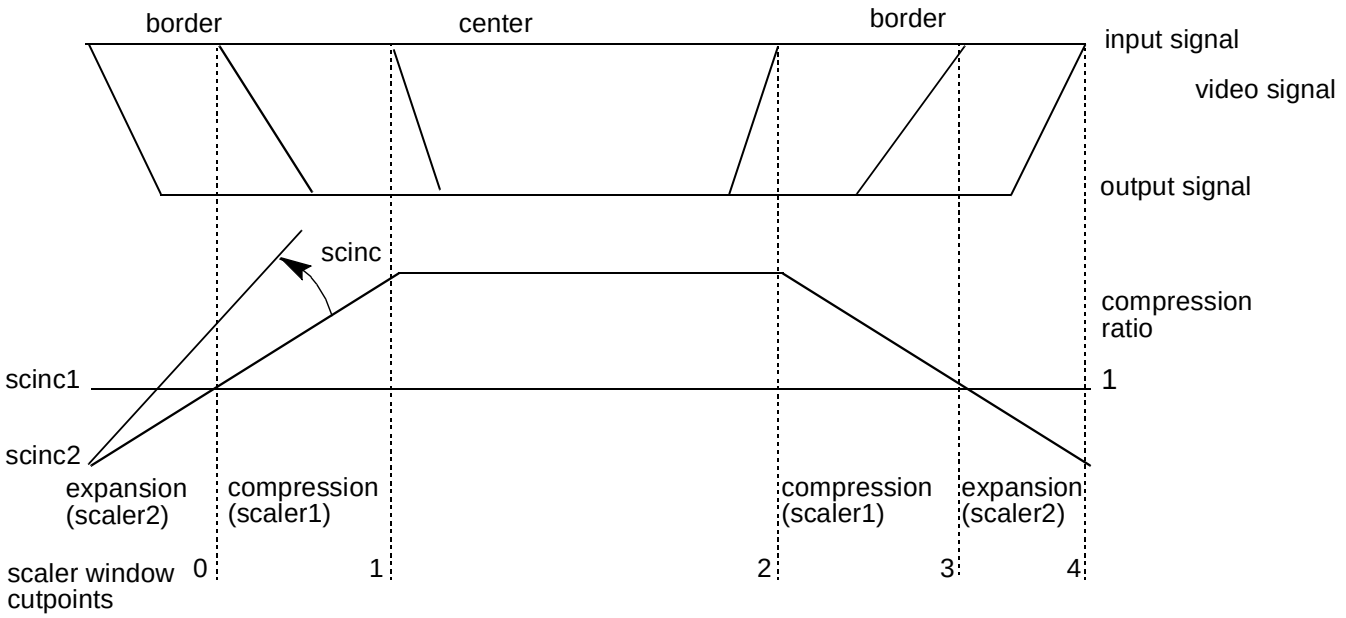


Fig. 3–2: Scaler operation for ‘panorama’ mode at 13.5 MHz

Table 3–4: Set-up values for nonlinear scaler modes

Mode	DIGIT3000 (20.25 MHz)				LLC (13.5 MHz)			
	‘waterglass’ border 35%		‘panorama’ border 30%		‘waterglass’ border 35%		‘panorama’ border 30%	
Register	center 3/4	center 5/6	center 4/3	center 6/5	center 3/4	center 5/6	center 4/3	center 6/5
scinc1	1643	1427	1024	1024	2464	2125	1024	1024
scinc2	1024	1024	376	611	1024	1024	573	914
scinc	90	56	85	56	202	124	190	126
fflim	945	985	921	983	719	719	681	715
scw1 – 0	110	115	83	94	104	111	29	13
scw1 – 1	156	166	147	153	104	111	115	117
scw1 – 2	317	327	314	339	256	249	226	241
scw1 – 3	363	378	378	398	256	249	312	345
scw1 – 4	473	493	461	492	360	360	341	358
scw2 – 0	110	115	122	118	104	111	38	14
scw2 – 1	156	166	186	177	104	111	124	118
scw2 – 2	384	374	354	363	256	249	236	242
scw2 – 3	430	425	418	422	256	249	322	346
scw2 – 4	540	540	540	540	360	360	360	360

4. Specifications

4.1. Outline Dimensions

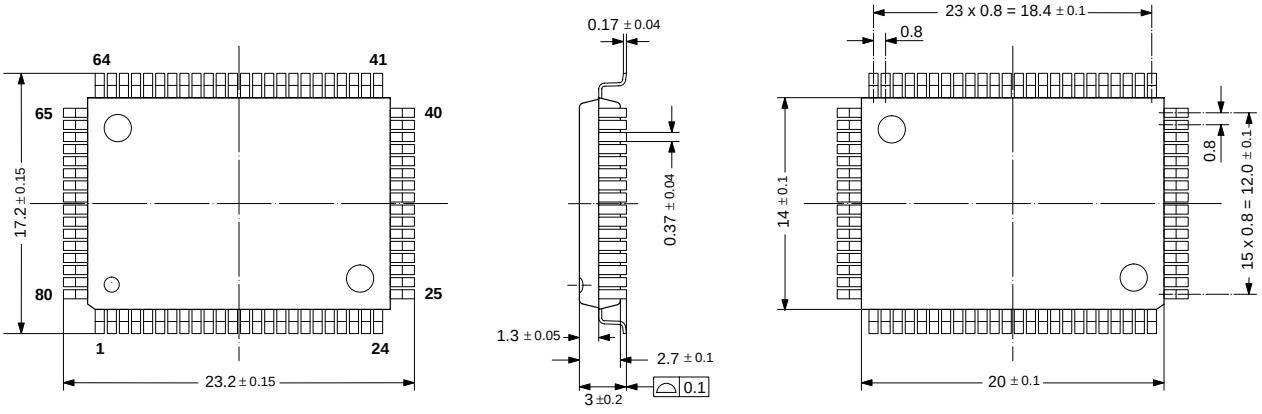


Fig. 4–1: 80-Pin Plastic Quad Flat Package **(PQFP80)**
Weight approximately 1.61 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram
SUPPLYA = 4.75...5.25 V, SUPPLYD = 3.15...3.45 V

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
1	B1/CB1IN	IN	VREF	Blue1/Cb1 Analog Component Input
2	G1/Y1IN	IN	VREF	Green1/Y1 Analog Component Input
3	R1/CR1IN	IN	VREF	Red1/Cr1 Analog Component Input
4	B2/CB2IN	IN	VREF	Blue2/Cb2 Analog Component Input
5	G2/Y2IN	IN	VREF	Green2/Y2 Analog Component Input
6	R2/CR2IN	IN	VREF	Red2/Cr2 Analog Component Input
7	ASGF		X	Analog Shield GND_F
8	FFRSTWIN	IN	LV or GND_D	FIFO Reset Write Input **
9	V_{SUPCAP}	OUT	X	Digital Decoupling Circuitry Supply Voltage
10	V_{SUPD}	SUPPLYD	X	Supply Voltage, Digital Circuitry
11	GND_D	SUPPLYD	X	Ground, Digital Circuitry
12	GND_{CAP}	OUT	X	Digital Decoupling Circuitry GND
13	SCL	IN/OUT	X	I^2C Bus Clock

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
14	SDA	IN/OUT	X	I^2C Bus Data
15	RESQ	IN	X	Reset Input, Active Low
16	TEST	IN	GND_D	Test Pin, connect to GND_D
17	VGAV	IN	GND_D	VGAV Input
18	YCOEQ	IN	GND_D	Y/C Output Enable Input, Active Low
19	FFIE	OUT	LV	FIFO Input Enable
20	FFWE	OUT	LV	FIFO Write Enable
21	FFRSTW	OUT	LV	FIFO Reset Write/Read
22	FFRE	OUT	LV	FIFO Read Enable
23	FFOE	OUT	LV	FIFO Output Enable
24	CLK20	IN/OUT	LV	Main Clock Output 20.25 MHz
25	GND_{PA}	OUT	X	Pad Decoupling Circuitry GND
26	V_{SUPPA}	OUT	X	Pad Decoupling Circuitry Supply Voltage
27	LLC2	OUT	LV	Double Clock Output
28	LLC1	IN/OUT	LV	Clock Output
29	V_{SUPLLC}	SUPPLYD	X	Supply Voltage, LLC Circuitry
30	GND_{LLC}	SUPPLYD	X	Ground, LLC Circuitry
31	Y7	OUT	GND_Y	Picture Bus Luma (MSB)
32	Y6	OUT	GND_Y	Picture Bus Luma
33	Y5	OUT	GND_Y	Picture Bus Luma
34	Y4	OUT	GND_Y	Picture Bus Luma
35	GND_Y	SUPPLYD	X	Ground, Luma Output Circuitry
36	V_{SUPY}	SUPPLYD	X	Supply Voltage, Luma Output Circuitry
37	Y3	OUT	GND_Y	Picture Bus Luma
38	Y2	OUT	GND_Y	Picture Bus Luma
39	Y1	OUT	GND_Y	Picture Bus Luma
40	Y0	OUT	GND_Y	Picture Bus Luma (LSB)
41	C7	OUT	GND_C	Picture Bus Chroma (MSB)
42	C6	OUT	GND_C	Picture Bus Chroma
43	C5	OUT	GND_C	Picture Bus Chroma
44	C4	OUT	GND_C	Picture Bus Chroma

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
45	V_{SUPC}	SUPPLYD	X	Supply Voltage, Chroma Output Circuitry
46	GND_C	SUPPLYD	X	Ground, Chroma Output Circuitry
47	C3	OUT	GND_C	Picture Bus Chroma
48	C2	OUT	GND_C	Picture Bus Chroma
49	C1	OUT	GND_C	Picture Bus Chroma
50	C0	OUT	GND_C	Picture Bus Chroma (LSB)
51	GND_{SY}	SUPPLYD	X	Ground, Sync Pad Circuitry
52	V_{SUPSY}	SUPPLYD	X	Supply Voltage, Sync Pad Circuitry
53	INTLC	OUT	LV	Interlace Output
54	AVO	OUT	LV	Active Video Output
55	FSY/HC/HSYA	OUT	LV	Front Sync/ Horizontal Clamp Pulse/Front-End Horizontal Sync Output **
56	MSY/HS	IN/OUT	LV	Main Sync/Horizontal Sync Pulse
57	VS	OUT	LV	Vertical Sync Pulse
58	FPDAT/VSYA	IN/OUT	LV	Front-End/Back-End Data/Front-End Vertical Sync Output **
59	V_{STBY}	SUPPLYA	X	Standby Supply Voltage
60	CLK5	OUT	LV	CCU 5 MHz Clock Output
62	XTAL1	IN	X	Analog Crystal Input
63	XTAL2	OUT	X	Analog Crystal Output
64	ASGF		X	Analog Shield GND_F
65	GND_F	SUPPLYA	X	Ground, Analog Front-End
66	VRT	OUTPUT	X	Reference Voltage Top, Analog
67	I2CSEL	IN	X	I^2C Bus Address Select
68	ISGND	SUPPLYA	X	Signal Ground for Analog Input, connect to GND_F
69	V_{SUPF}	SUPPLYA	X	Supply Voltage, Analog Front-End
70	VOUT	OUT	LV	Analog Video Output
71	CIN	IN	LV*	Chroma / Analog Video 5 Input
72	VIN1	IN	VRT*	Video 1 Analog Input
73	VIN2	IN	VRT	Video 2 Analog Input
74	VIN3	IN	VRT	Video 3 Analog Input
75	VIN4	IN	VRT	Video 4 Analog Input

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
76	V_{SUPAI}	SUPPLYA	X	Supply Voltage, Analog Component Inputs Front-End
77	GND_{AI}	SUPPLYA	X	Ground, Analog Component Inputs Front-End
78	VREF	OUTPUT	X	Reference Voltage Top, Analog Component Inputs Front-End
79	FB1IN	IN	VREF	Fast Blank Input
80	AISGND	SUPPLYA	X	Signal Ground for Analog Component Inputs, connect to GND_{AI}
61	NC	–	LV OR GND_D	Not connected

*****) chroma selector must be set to 1 (CIN chroma select)

**) available since VPC 323xD-C5

4.3. Pin Descriptions (pin numbers for PQFP80 package)

Pins 1-3 – Analog Component Inputs RGB1/YC_rC_b1 (Fig. 4–11)
These are analog component inputs with fast blank control. A RGB or YC_rC_b signal is converted using the component AD converter. The input signals must be AC-coupled.

Pins 4-6 – Analog Component Inputs RGB2/YC_rC_b2 (Fig. 4–11)
These are analog component inputs without fastblank control. A RGB or YC_rC_b signal is converted using the component AD converter. The input signals must be AC-coupled.

Pin 7, 64 – Ground, Analog Shield Front-End GND_F

Pin 8 – FIFO Reset Write Input FFRSTWIN (Fig. 4–3)
In case of a two VPCD application, this pin connects to the FFRSTW pin of the $VPCD_{pip}$.

Pin 9 – Supply Voltage, Decoupling Circuitry V_{SUPCAP}
This pin is connected with 220 nF/1.5 nF/390 pF to $GND_{CAP.}$

Pin 10 – Supply Voltage, Digital Circuitry V_{SUPD}

Pin 11 – Ground, Digital Circuitry GND_D

Pin 12 – Ground, Decoupling Circuitry GND_{CAP}

Pin 13– I^2C Bus Clock SCL (Fig. 4–13)
This pin connects to the I^2C bus clock line.

Pin 14– I^2C Bus Data SDA (Fig. 4–13)
This pin connects to the I^2C bus data line.

Pin 15 – Reset Input RESQ (Fig. 4–3)
A low level on this pin resets the VPC 323xD.

Pin 16 – Test Input TEST (Fig. 4–3)
This pin enables factory test modes. For normal operation, it must be connected to ground.

Pin 17 – VGAV-Input (Fig. 4–3)
This pin is connected to the vertical sync signal of a VGA signal.

Pin 18 – YC Output Enable Input YCOEQ (Fig. 4–3)
A low level on this pin enables the luma and chroma outputs.

Pin 19 – FIFO Input Enable FFIE (Fig. 4–4)
This pin is connected to the IE pin of the external field memory.

Pin 20 – FIFO Write Enable FFWE (Fig. 4–4)
This pin is connected to the WE pin of the external field memory.

Pin 21 – FIFO Reset Write/Read FFRSTW (Fig. 4–4)
This pin is connected to the RSTW pin of the external field memory.

Pin 22 – FIFO Read Enable FFRE (Fig. 4–4)
This pin is connected to the RE pin of the external field memory.

Pin 23 – FIFO Output Enable FFOE (Fig. 4–4)
This pin is connected to the OE pin of the external field memory.

Pin 24 – Main Clock Output CLK20 (Fig. 4–4)
This is the 20.25 MHz main clock output.

Pin 25 – Ground, Analog Pad Circuitry GND_{PA}

Pin 26 – Supply Voltage, Analog Pad Circuitry V_{SUPPA}
This pin is connected with 47 nF/1.5 nF to GND_{PA}

Pin 27 – Double Output Clock, LLC2 (Fig. 4–4)

Pin 28 – Output Clock, LLC1 (Fig. 4–4)
This is the clock reference for the luma, chroma, and status outputs.

Pin 29 – Supply Voltage, LLC Circuitry V_{SUPLLC}
This pin is connected with 68 nF to GND_{LLC}

Pin 30 – Ground, LLC Circuitry GND_{LLC}

Pins 31 to 34, 37 to 40 – Luma Outputs Y7 – Y0 (Fig. 4–4)
These output pins carry the digital luminance data. The outputs are clocked with the LLC1 clock. In ITUR656 mode, the Y/C data is multiplexed and clocked with LLC2 clock.

Pin 35– Ground, Luma Output Circuitry GND_Y
This pin is connected with 68 nF to GND_Y

Pin 36 – Supply Voltage, Luma Output Circuitry V_{SUPY}

Pins 41 to 44, 47 to 50 – Chroma Outputs C7–C0 (Fig. 4–4) These outputs carry the digital C_rC_b chrominance data. The outputs are clocked with the LL1 clock. The C_rC_b data is sampled at half the clock rate and multiplexed. The C_rC_b multiplex is reset for each TV line. In ITUR656 mode, the chroma outputs can be tri-stated.

Pin 45 – Supply Voltage, Chroma Output Circuitry V_{SUPC}
This pin is connected with 68 nF to GND_C

Pin 46 – Ground, Chroma Output Circuitry GND_C

Pin 51 – Ground, Sync Pad Circuitry GND_{SY}

Pin 52 – Supply Voltage, Sync Pad Circuitry V_{SUPSY}
This pin is connected with 47 nF/1.5 nF to GND_{SY}

Pin 53 – Interlace Output, INTLC (Fig. 4–4)
This pin supplies the interlace information, 0 indicates first field, 1 indicates second field.

Pin 54 – Active Video Output, AVO (Fig. 4–4)
This pin indicates the active video output data. The signal is clocked with the LLC1 clock.

Pin 55 – Front Sync/Horizontal Clamp Pulse/Front-End Horizontal Sync Output, FSY/HC/HSYA (Fig. 4–4)
This signal can be used
a) to clamp an external video signal, that is synchronous to the input signal. The timing is programmable or
b) to synchronize an external video horizontally, that is asynchronous to the input video and stored in an external memory. The timing is fixed.
In DIGIT3000 mode, this pin supplies the front sync information.

Pin 56 – Main Sync/Horizontal Sync Pulse MSY/HS (Fig. 4–4)
This pin supplies the horizontal sync pulse information in line-locked mode. In DIGIT3000 mode, this pin is the main sync input.

Pin 57 – Vertical Sync Pulse, VS (Fig. 4–4)
This pin supplies the vertical sync signal.

Pin 58 – Front-End/Back-End Data/Front-End Vertical Sync Output FPDAT/VSYA (Fig. 4–5)
In DIGIT3000 mode, this pin interfaces to the DDP 331x back-end processor. The information for the deflection drives and for the white drive control, i. e. the beam current limiter, is transmitted by this pin.
In LLC mode, this signal can be used to synchronize an external video vertically, that is asynchronous to the input video and stored in an external memory. The timing is fixed.
If not used, this pin is connected with 10kΩ to V_{SUPSY}.

Pin 59 – Standby Supply Voltage V_{STDBY}
In standby mode, only the clock oscillator is active, GND_F should be ground reference. Please activate RESQ before powering-up other supplies

Pin 60 – CCU 5 MHz Clock Output CLK5 (Fig. 4–10)
This pin provides a clock frequency for the TV microcontroller, e.g. a CCU 3000 controller. It is also used by the DDP 331x display controller as a standby clock.

Pins 62and 63 – XTAL1 Crystal Input and XTAL2 Crystal Output (Fig. 4–7)
These pins are connected to an 20.25 MHz crystal oscillator which is digitally tuned by integrated shunt capacitances. The CLK20 and CLK5 clock signals are derived from this oscillator. An external clock can be fed into XTAL1. In this case, clock frequency adjustment must be switched off.

Pin 65 – Ground, Analog Front-End GND_F

Pin 66 – Reference Voltage Top VRT (Fig. 4–8)
Via this pin, the reference voltage for the A/D converters is decoupled. The pin is connected with 10 µF/47 nF to the Signal Ground Pin.

Pin 67 – I^2C Bus address select I2CSEL (Fig. 4–12)
This pin determines the I^2C bus address of the IC.

Table 4–1: VPC 323xD I^2C address select

I2CSEL	I^2C Add.
GND_F	88/89 hex
VRT	8C/8D hex
V_{SUPF}	8E/8F hex

Pin 68 – Signal GND for Analog Input ISGND (Fig. 4–10) This is the high quality ground reference for the video input signals.

Pin 69 – Supply Voltage, Analog Front-End V_{SUPF} (Fig. 4–8)
This pin is connected with 220 nF/1.5 nF/390 pF to GND_F

Pin 70 – Analog Video Output, VOUT (Fig. 4–6)
The analog video signal that is selected for the main (luma, CVBS) ADC is output at this pin. An emitter follower is required at this pin.

Pin 71 – Chroma Input CIN (Fig. 4–9)
This pin is connected to the S-VHS chroma signal. A resistive divider is used to bias the input signal to the middle of the converter input range. CIN can only be connected to the chroma (Video 2) A/D converter. The signal must be AC-coupled.

Pins 72-75 – Video Input 1–4 (Fig. 4–11)
These are the analog video inputs. A CVBS or S-VHS luma signal is converted using the luma (Video 1) AD converter. The VIN1 input can also be switched to the chroma (Video 2) ADC. The input signal must be AC-coupled.

Pin 76 – Supply Voltage, Analog Component Inputs Front-End V_{SUPAI}
This pin is connected with 220 nF/1.5 nF/390 pF to GND_{AI}

Pin 77 – Ground, Analog Component Inputs Front-End GND_{AI}

Pin 78 – Reference Voltage Top VREF (Fig. 4–8)
Via this pin, the reference voltage for the analog component A/D converters is decoupled. The pin is connected with 10 µF/47 nF to the Analog Component Signal Ground Pin.

Pin 79 – Fast Blank Input FB1IN (Fig. 4–10)
This pin is connected to the analog fast blank signal. It controls the insertion of the RGB1/YC_rC_b1 signals. The input signal must be DC-coupled.

Pin 80 – Signal GND for Analog Component Inputs AISGND (Fig. 4–10)
This is the high quality ground reference for the component input signals.

4.4. Pin Configuration

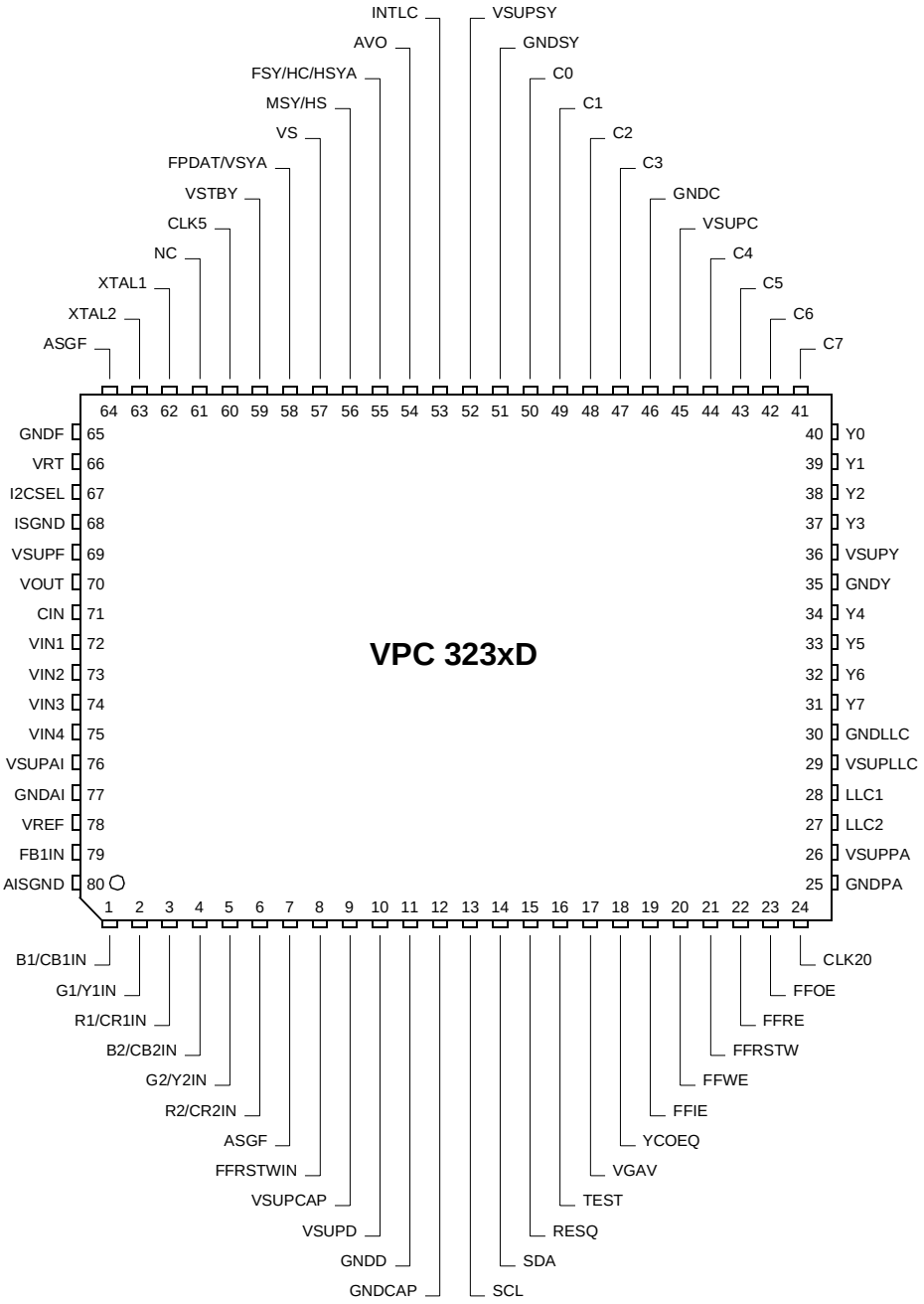


Fig. 4–2: 80-pin PQFP package

4.5. Pin Circuits

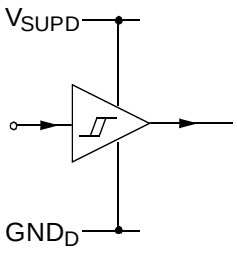


Fig. 4–3: Input pins RESQ, TEST, VGAV, YCOEQ, FFRSTWRIN

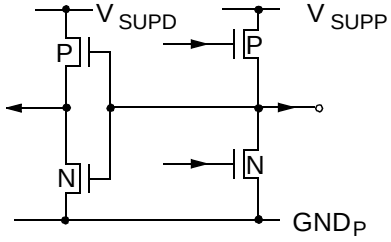


Fig. 4–4: Output pins C0–C7, Y0–Y7, FSY, MSY, HC, AVO, VS, INTLC, HS, LLC1, LLC2, CLK20, FFWE, FFRE, FFIE, FFRD, RSTWR

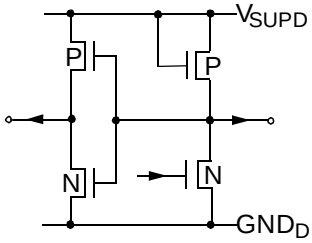


Fig. 4–5: Input/Output pin FPDAT

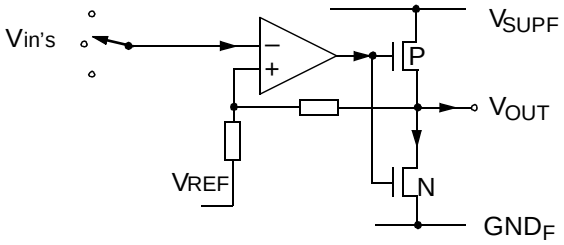


Fig. 4–6: Output pin VOUT

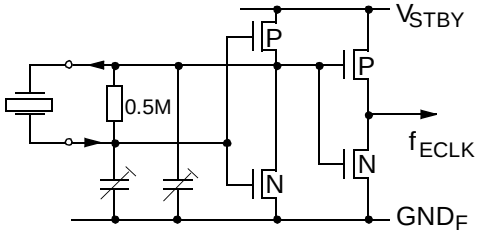


Fig. 4–7: Input/Output Pins XTAL1, XTAL2

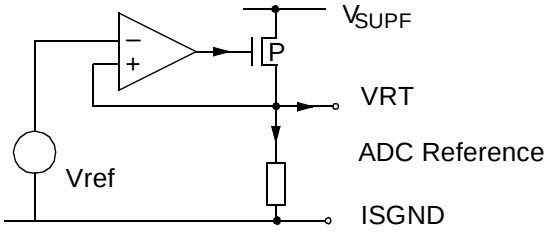


Fig. 4–8: Pins VRT, ISGND and VREF, AISGND

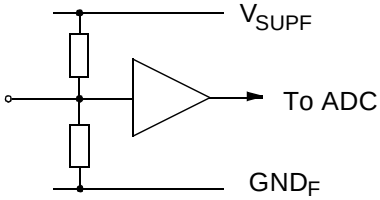


Fig. 4–9: Chroma input CIN

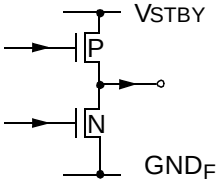


Fig. 4–10: Output pin CLK5

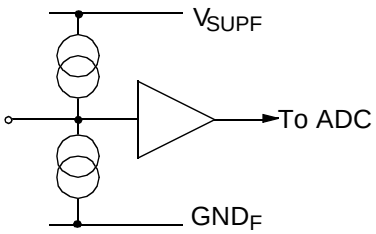


Fig. 4–11: Input pins VIN1–VIN4, RGB/YC$_r$C$_b$1/2, FB1IN

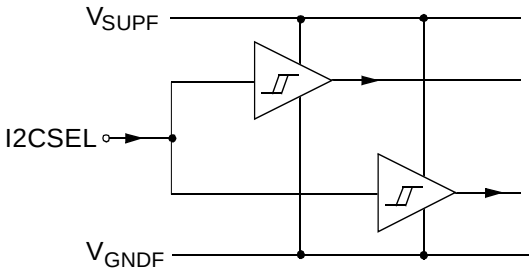


Fig. 4–12: I2CSEL

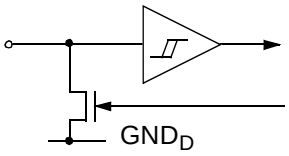


Fig. 4–13: Pins SDA, SCL

4.6. Electrical Characteristics

4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	–40	125	°C
$V_{SUPA/D}$	Supply Voltage, all Supply Inputs		–0.3	6	V
V_I	Input Voltage, all Inputs		–0.3	V_{SUPA}+0.3	V
V_O	Output Voltage, all Outputs		–0.3	V_{SUPD}+0.3	V

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.6.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	–	65	°C
T_C	Case Operating Temperature	–	0	–	105	°C
V_{SUP}	Supply Voltages, all analog Supply Pins	–	4.75	5.0	5.25	V
V_{SUPD}	Supply Voltages, all digital Supply Pins	–	3.15	3.3	3.45	V
f_{XTAL}	Clock Frequency	XTAL1/2	–	20.25	–	MHz

4.6.3. Recommended Crystal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature	0	–	65	°C
f_P	Parallel Resonance Frequency with Load Capacitance **C_L = 13 pF**	–	20.250000	–	MHz
$\Delta f_P/f_P$	Accuracy of Adjustment	–	–	±20	ppm
$\Delta f_P/f_P$	Frequency Temperature Drift	–	–	±30	ppm
R_R	Series Resistance	–	–	25	Ω
C_0	Shunt Capacitance	3	–	7	pF
C_1	Motional Capacitance	20	–	30	fF
Load Capacitance Recommendation					
C_{Lext}	External Load Capacitance [1] from pins to Ground (pin names: Xtal1 Xtal2)	–	3.3	–	pF
DCO Characteristics [2,3]					
$C_{ICLoadmin}$	Effective Load Capacitance @ min. DCO–Position, Code 0, package: 68PLCC	3	4.3	5.5	pF
$C_{ICLoadrng}$	Effective Load Capacitance Range, DCO Codes from 0..255	11	12.7	15	pF

[1] Remarks on defining the External Load Capacitance:

External capacitors at each crystal pin to ground are required. They are necessary to tune the effective load capacitance of the PCBs to the required load capacitance C_L of the crystal. The higher the capacitors, the lower the clock frequency results. The nominal free running frequency should match f_p MHz. Due to different layouts of customer PCBs the matching capacitor size should be determined in the application. The suggested value is a figure based on experience with various PCB layouts. Tuning condition: Code DVCO Register=–720

[2] Remarks on Pulling Range of DCO:

The pulling range of the DCO is a function of the used crystal and effective load capacitance of the IC (C_{ICLoad} +$C_{LoadBoard}$). The resulting frequency f_L with an effective load capacitance of $C_{Leff} = C_{ICLoad} + C_{LoadBoard}$ is:

$$f_L = f_P * \frac{1 + 0.5 * [\, C_1 / (C_0 + C_L)\,]}{1 + 0.5 * [\, C_1 / (C_0 + C_{Leff})\,]}$$

[3] Remarks on DCO codes

The DCO hardware register has 8 bits, the FP control register uses a range of –2048...2047

4.6.4. Characteristics

at T_A = 0 to 65 °C, V_{SUPF} = 4.75 to 5.25 V, V_{SUPD} = 3.15 to 3.45 V, f = 20.25 MHz for min./max. values
at T_C = 60 °C, V_{SUPF} = 5 V, V_{SUPD} = 3.3 V, f = 20.25 MHz for typical values

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
P_{TOT}	Total Power Dissipation		–	720	1000	mW
I_{VSUPA}	Current Consumption	V_{SUPF}	–	75	100	mA
I_{VSUPD}	Current Consumption	V_{SUPD}	–	102	140	mA
I_{VSTDBY}	Current Consumption	V_{STDBY}	–	1	–	mA
I_L	Input / Output Leakage Current	All I/O Pins	–1	–	1	µA

4.6.4.1. Characteristics, 5 MHz Clock Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	CLK5	–	–	0.4	V	I_{OL} = 0.4 mA
V_{OH}	Output High Voltage		4.0	–	V– STDBY	V	$–I_{OL}$ = 0.9 mA
t_{OT}	Output Transition Time		–	50	–	ns	C_{LOAD} = 30 pF

4.6.4.2. Characteristics, 20 MHz Clock Input/Output, External Clock Input (XTAL1)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{DCAV}	DC Average	CLK20	$V_{SUPD}/2$ – 0.3	$V_{SUPD}/2$	$V_{SUPD}/2$ + 0.3	V	C_{LOAD} = 30 pF
V_{PP}	V_{OUT} Peak to Peak		$V_{SUPD}/2$ – 0.3	$V_{SUPD}/2$	$V_{SUPD}/2$ + 0.3	V	C_{LOAD} = 30 pF
t_{OT}	Output Transition Time		–	–	18	ns	C_{LOAD} = 30 pF
V_{IT}	Input Trigger Level		2.1	2.5	2.9	V	only for test purposes
V_I	Clock Input Voltage	XTAL1	1.3	–	–	V_{PP}	capacitive coupling used, XTAL2 open

4.6.4.3. Characteristics, Reset Input, Test Input, VGAV Input, YCOEQ Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	RESQ TEST VGAV YCOEQ	–	–	0.8	V	
V_{IH}	Input High Voltage		2.0	–	–	V	
t_{OEED}	Data Output Enable/Disable Time	YCOEQ	12	–	15	ns	

4.6.4.4. Characteristics, Power-up Sequence

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{Vdel}	Ramp Up Difference of Supplies		-1	–	1	s	
t_{Vrmpl}	Transition Time of Supplies		–	–	50	ms	

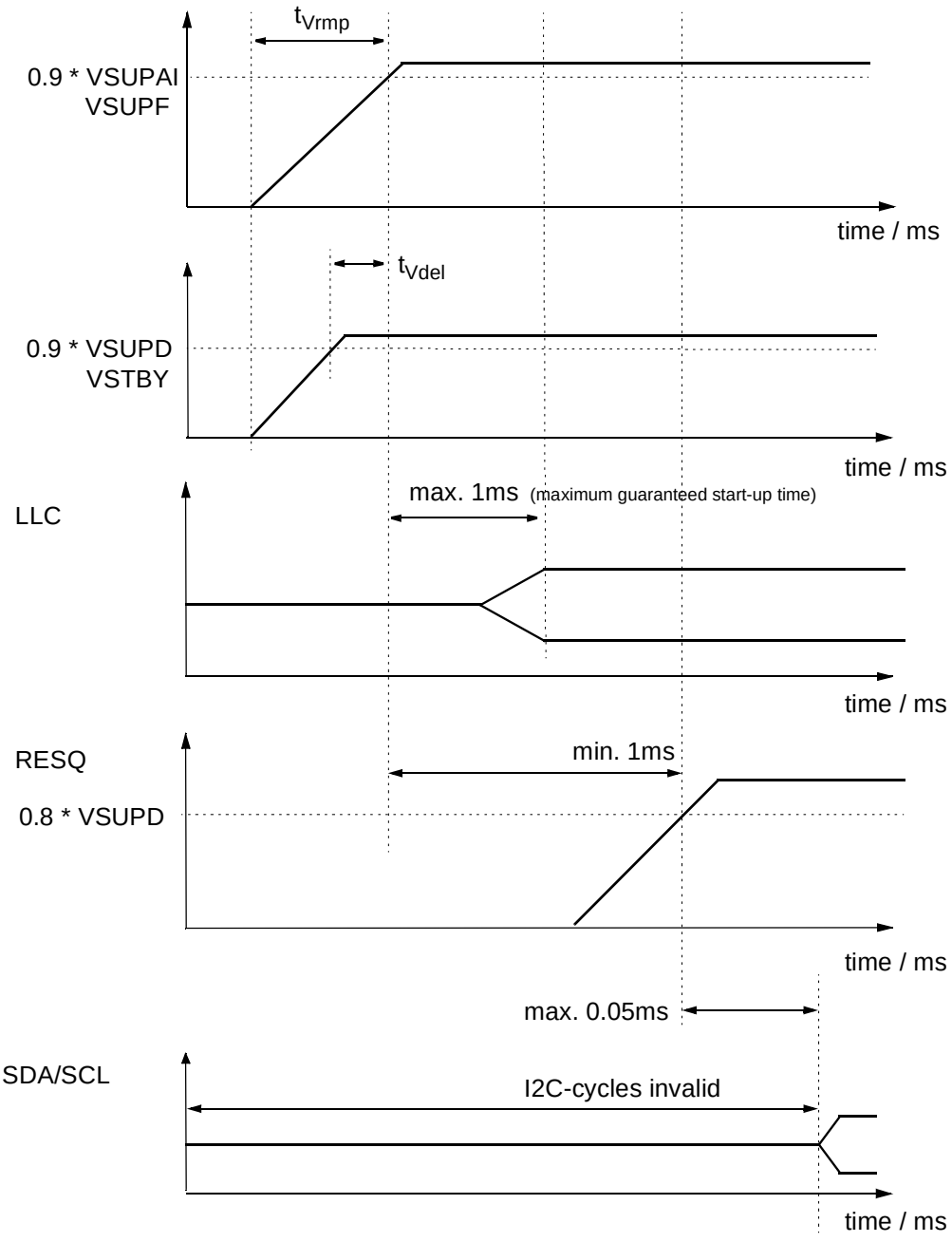


Fig. 4–14: Power-Up sequence

4.6.4.5. Characteristics, FPDAT Input/Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	FPDAT	–	–	0.5	V	I_{OL} = 4.0 mA
t_{OH}	Output Hold Time		6	–	–	ns	
t_{ODL}	Output Delay Time		–	–	35	ns	C_L = 40 pF
V_{IL}	Input Low Voltage		–	–	0.8	V	
V_{IH}	Input High Voltage		1.5	–	–	V	
t_{IS}	Input Setup Time		7	–	–	ns	
t_{IH}	Input Hold Time		5	–	–	ns	
C_L	Load capacitance		–	–	40	pF	

4.6.4.6. Characteristics, I²C Bus Interface

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	SDA, SCL	–	–	1.0	V	
V_{IH}	Input High Voltage		2.0	–	–	V	
V_{OL}	Output Low Voltage		–	–	0.4 0.6	V V	I_I = 3 mA I_I = 6 mA
V_{IH}	Input Capacitance		–	–	5	pF	
t_F	Signal Fall Time		–	–	300	ns	C_L = 400 pF
t_R	Signal Rise Time		–	–	300	ns	C_L = 400 pF
f_{SCL}	Clock Frequency	SCL	0	–	400	kHz	
t_{LOW}	Low Period of SCL		1.3	–	–	µs	
t_{HIGH}	High Period of SCL		0.6	–	–	µs	
$t_{SU\ Data}$	Data Set Up Time to SCL high	SDA	100	–	–	ns	
$t_{HD\ Data}$	DATA Hold Time to SCL low		0	–	0.9	µs	

4.6.4.7. Characteristics, I²C Bus Address Select I2CSEL Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	I2CSEL	GND_F	–	1.3	V	
V_{IH}	Input High Voltage		3.7	–	V_{SUPF}	V	
V_{MED}	Input Medium Voltage		VRT	–	VRT	V	

4.6.4.8. Characteristics, Analog Video and Component Inputs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{VIN}	Analog Input Voltage	VIN1, VIN2 VIN3, VIN4 CIN R1/CR1IN G1/Y1IN B1/CB1IN R2/CR2IN G2/Y2IN B2/CB2IN FBIN	0	–	3.5	V	
C_{CP}	Input Coupling Capacitor Video Inputs	VIN1, VIN2 VIN3, VIN4	–	680	–	nF	
C_{CP}	Input Coupling Capacitor Chroma Input	CIN	–	1	–	nF	
C_{CP}	Input Coupling Capacitor Component Input	R1/CR1IN G1/Y1IN B1/CB1IN R2/CR2IN G2/Y2IN B2/CB2IN	–	220	–	nF	

4.6.4.9. Characteristics, Analog Front-End and ADCs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{VRT}	Reference Voltage Top	VRT VREF	2.4	2.5	2.6	V	10 µF/10 nF, 1 GΩ Probe
Luma – Path							
R_{VIN}	Input Resistance	VIN1 VIN2 VIN3 VIN4	1	–	–	MΩ	Code Clamp–DAC=0
C_{VIN}	Input Capacitance		–	–	4.5	pF	
V_{VIN}	Full Scale Input Voltage	VIN1 VIN2 VIN3 VIN4	1.8	2.0	2.2	V_{PP}	min. AGC Gain
V_{VIN}	Full Scale Input Voltage		0.5	0.6	0.7	V_{PP}	max. AGC Gain
AGC	AGC step width		–	0.166	–	dB	6-Bit Resolution= 64 Steps f_{sig}=1MHz, – 2 dBr of max. AGC–Gain
DNL_{AGC}	AGC Differential Non-Linearity		–		±0.5	LSB	
V_{VINCL}	Input Clamping Level, CVBS	VIN1 VIN2 VIN3 VIN4	–	1.0	–	V	Binary Level = 64 LSB min. AGC Gain
Q_{CL}	Clamping DAC Resolution		–16	–	15	steps	5 Bit – I–DAC, bipolar V_{VIN}=1.5 V
$I_{CL–LSB}$	Input Clamping Current per step		0.7	1.0	1.3	µA	
DNL_{ICL}	Clamping DAC Differential Non-Linearity		–	–	±0.5	LSB	

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Chroma – Path							
R_{CIN}	Input Resistance SVHS Chroma	CIN VIN1	1.4	2.0	2.6	kΩ	
V_{CIN}	Full Scale Input Voltage, Chroma		1.08	1.2	1.32	V_{PP}	
V_{CINDC}	Input Bias Level, SVHS Chroma		–	1.5	–	V	
	Binary Code for Open Chroma Input		–	128	–	–	
Component – Path							
R_{VIN}	Input Resistance	R1/CR1IN G1/Y1IN B1/CB1IN R2/CR2IN G2/Y2IN B2/CB2IN	1	–	–	MΩ	Code Clamp–DAC=0
C_{VIN}	Input Capacitance		–	–	4.5	pF	
V_{VIN}	Full Scale Input Voltage		0.85	1.0	1.1	V_{PP}	min. Gain (XAR=-0)
V_{VIN}	Full Scale Input Voltage		1.2	1.4	1.6	V_{PP}	max. Gain (XAR=-1)
V_{VINCL}	Input Clamping Level RGB, Y		–	1.06	–	V	Binary Level = 16 LSB XAR=-0
V_{VINCL}	Input Clamping Level Cr, Cb		–	1.5	–	V	Binary Level = 128 LSB XAR=-0
	Gain Match		–	1.2	1.7	%	Full Scale at 1 MHz, XAR=-0
Q_{CL}	Clamping DAC Resolution		–32	–	31	steps	6 Bit – I–DAC, bipolar V_{VIN}=1.5 V
$I_{CL–LSB}$	Input Clamping Current per step		0.59	0.85	1.11	µA	
DNL_{ICL}	Clamping DAC Differential Non-Linearity		–	–	±0.5	LSB	
Dynamic Characteristics for all Video-Paths (Luma + Chroma) and Component-Paths							
BW	Bandwidth	VIN1 VIN2 VIN3 VIN4 R1/CR1IN G1/Y1IN B1/CB1IN R2/CR2IN G2/Y2IN B2/CB2IN	8	10	–	MHz	–2 dBr input signal level
XTALK	Crosstalk, any Two Video Inputs		–	–56	–46	dB	1 MHz, –2 dBr signal level
THD	Total Harmonic Distortion		–	–50	–42	dB	1 MHz, 5 harmonics, –2 dBr signal level
SINAD	Signal to Noise and Distortion Ratio		40	45	–	dB	1 MHz, all outputs, –2 dBr signal level
INL	Integral Non-Linearity		–	–	±1	LSB	Code Density, DC-ramp
DNL	Differential Non-Linearity		–	–	±0.8	LSB	
DG	Differential Gain		–	–	±3	%	–12 dBr, 4.4 MHz signal on DC-ramp
DP	Differential Phase		–	–	1.5	deg	

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Analog Video Output							
V_{OUT}	Output Voltage	Out: VOUT In: VIN1 VIN2 VIN3 VIN4	1.7	2.0	2.3	V_{PP}	V_{IN} = 1 V_{PP}, AGC= 0 dB
AGC_{VOUT}	AGC step width, VOUT		–	1.333	–	dB	3 Bit Resolution=7 Steps 3 MSBs of main AGC
DNL_{AGC}	AGC Differential Non-Linearity		–	–	±0.5	LSB	
V_{OUTDC}	DC-level		–	1	–	V	clamped to Back porch
BW	V_{OUT} Bandwidth		8	10	–	MHz	Input: –2 dBr of main ADC range, C_L≤10 pF
THD	V_{OUT} Total Harmonic Distortion		–	–	–40	dB	Input: –2 dBr of main ADC range, C_L≤10 pF 1 MHz, 5 Harmonics
C_{LVOUT}	Load Capacitance	VOUT	–	–	10	pF	
I_{LVOUT}	Output Current		–	–	±0.1	mA	

4.6.4.10.Characteristics, Analog FB Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
R_{FBIN}	Input Resistance	FB1IN	1	–	–	MΩ	Code Clamp–DAC=0
V_{FBIN}	Full Scale Input Voltage		0.85	1.0	1.1	V_{PP}	
V_{THFBMO}	Threshold for FB-Monitor		0.5	0.65	0.8	V_{PP}	
BW_{FBIN}	Bandwidth		8	10		MHz	–2 dBr input signal level
THD_{FBIN}	Total Harmonic Distortion		–	–50	–40	dB	1 MHz, 5 harmonics, –2 dBr signal level
$SINAD_{FBIN}$	Signal to Noise and Distortion Ratio		34	37	–	dB	1 MHz, all outputs, –2 dBr signal level
INL_{FBIN}	Integral Non-Linearity		–	0.3	±1	LSB	Code Density, DC-ramp
DNL_{FBIN}	Differential Non-Linearity		–	0.2	±0.8	LSB	

4.6.4.11.Characteristics, Output Pin Specification

Output Specification for SYNC, CONTROL, and DATA Pins:
Y[7:0], C[7:0], AVO, HS, HC, INTLC, VS, FSY, FFIE, FFWE, FFOE, FFRD, FFRSTWR

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
C_L	Load Capacitance		–	–	50	pF	
V_{OL}	Output Low Voltage		–	–	0.4	V	C_{load} =50pF
V_{OH}	Output High Voltage		2.4	–	–	V	C_{load} =50pF
t_{OH}	Output Hold Time		16	–	–	ns	LLC2=27.0MHz, OMODE=1 DBCLK=0/1
t_{OD}	Output Delay Time		–	–	26	ns	LLC2=27.0MHz, OMODE=1, DBCLK=0/1, NOTE1
t_{OH}	Output Hold Time		16	–	–	ns	LLC2=32.0MHz, OMODE=1, DBCLK=0/1
t_{OD}	Output Delay Time		–	–	22	ns	LLC2=32.0MHz, OMODE=1, DBCLK=0/1, NOTE1
t_{OD}	Output Hold Time		15	–	-	ns	CLK20=20.25MHz, OMODE=0, NOTE1
t_{OD}	Output Delay Time		–	–	35	ns	CLK20=20.25MHz, OMODE=0, NOTE1

NOTE 1: C_{LOAD} depends on the selected driver strength which is I^2C-programable.

Table 4–1: Adjustable driver strength for AVO, HS, HC, INTLC, VS, FFIE, FFWE, FFOE, FFRD, FFRSTWR:

Strength	Load	Strength	Load
0000	< 50 pF	1000	< 30,0pF
0001	< 47,5pF	1001	< 27,5 pF
0010	< 45,0 pF	1010	< 25,0 pF
0011	< 42,5 pF	1011	< 22,5 pF
0100	< 40,0pF	1100	< 20,0pF
0101	< 37,5 pF	1101	< 17,5pF
0110	< 35,0 pF	1110	< 15,0 pF
0111	< 32,5 pF	1111	< 12,5 pF

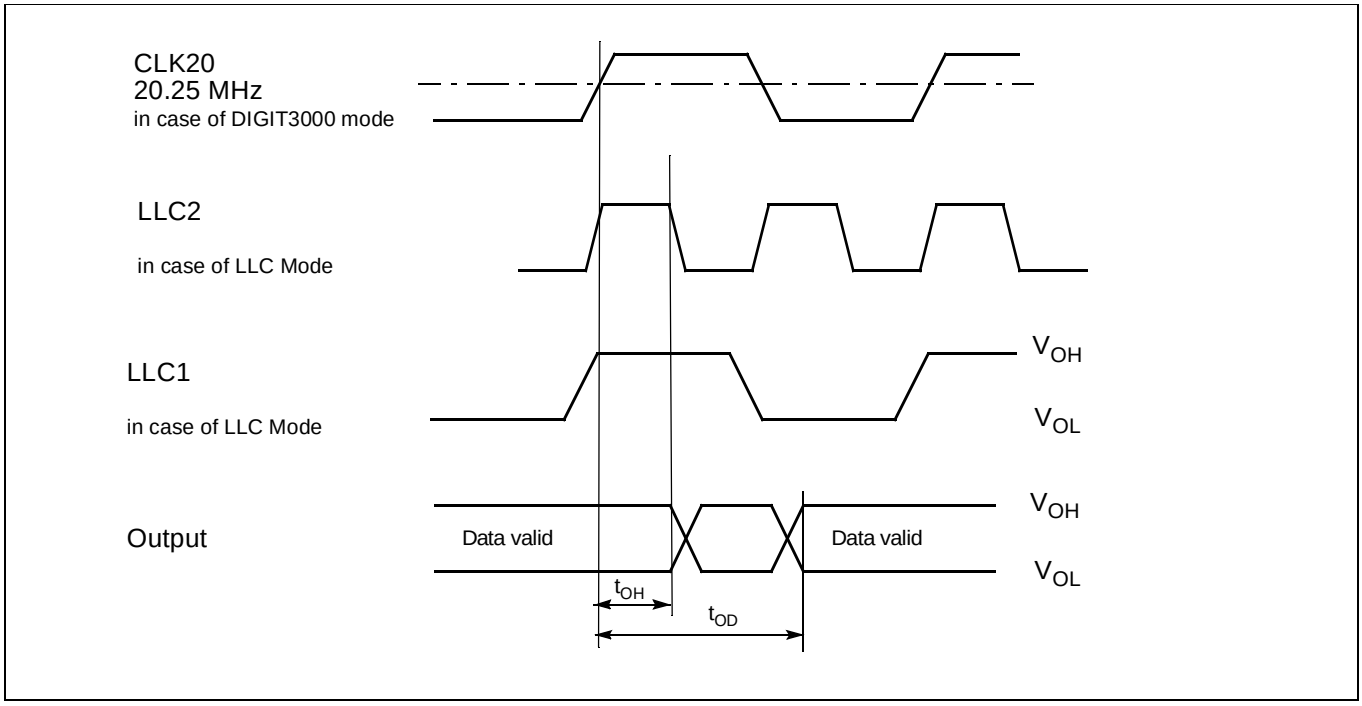


Fig. 4–15: Sync, control, and data outputs

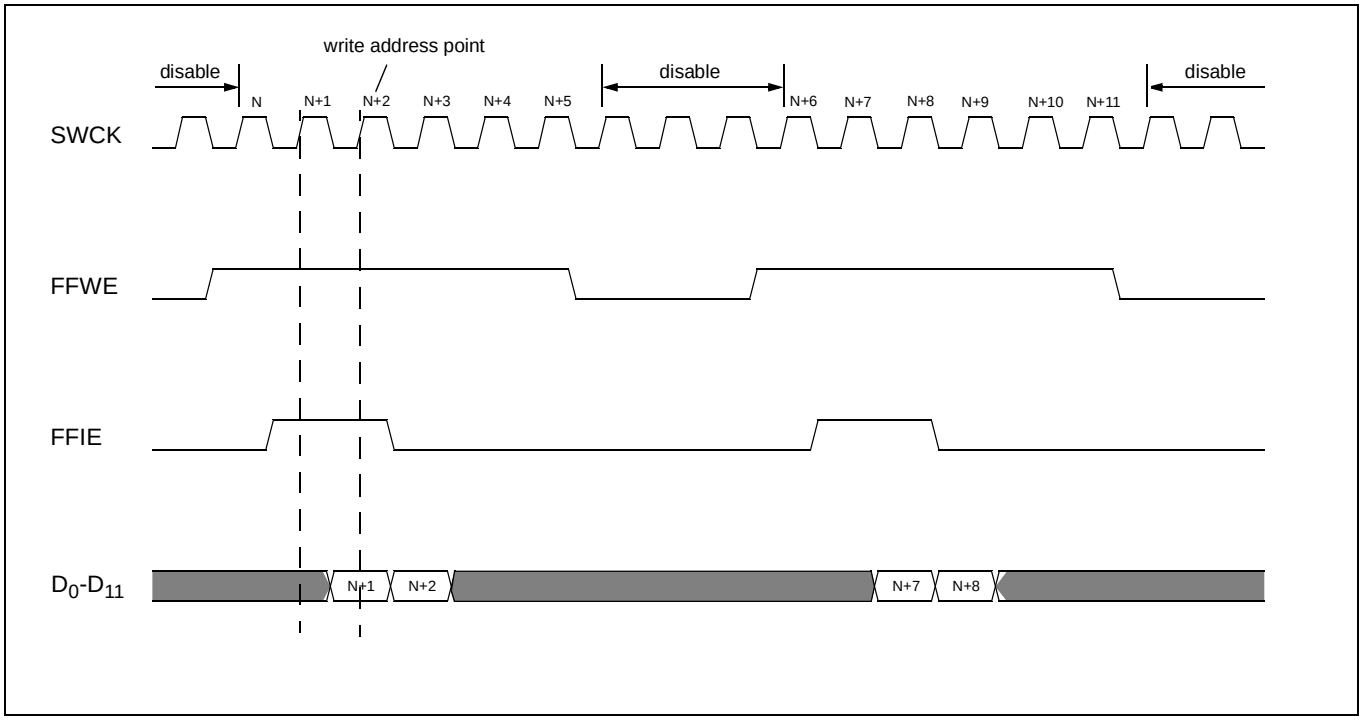


Fig. 4–16: Field memory write cycle timing

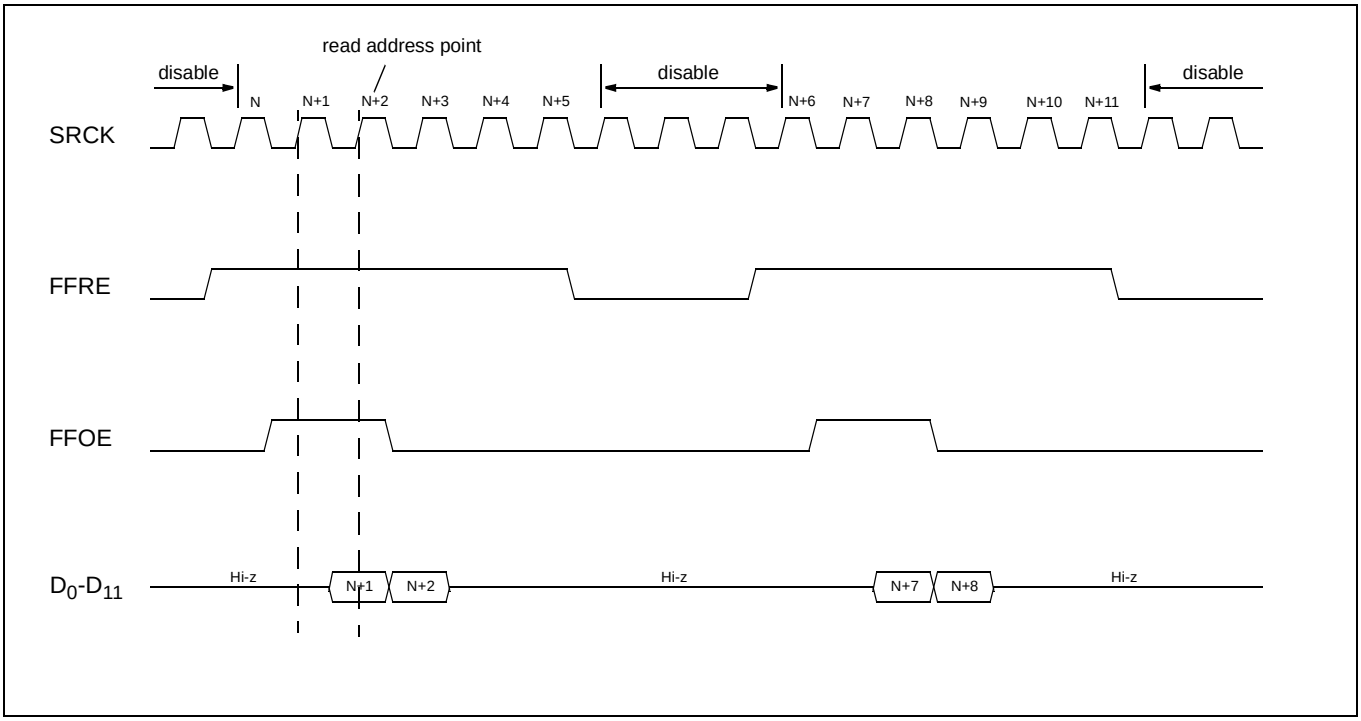


Fig. 4–17: Field memory read cycle timing

4.6.4.12.Characteristics, Input Pin Specification

Input Specification for SYNC, CONTROL, and DATA Pin: MSY (DIGIT3000 mode only)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage		–	–	0.8	V	
V_{IH}	Input High Voltage		1.5	–	–	V	
t_{IS}	Input Setup Time		7	–	–	ns	
t_{IH}	Input Hold Time		5	–	–	ns	

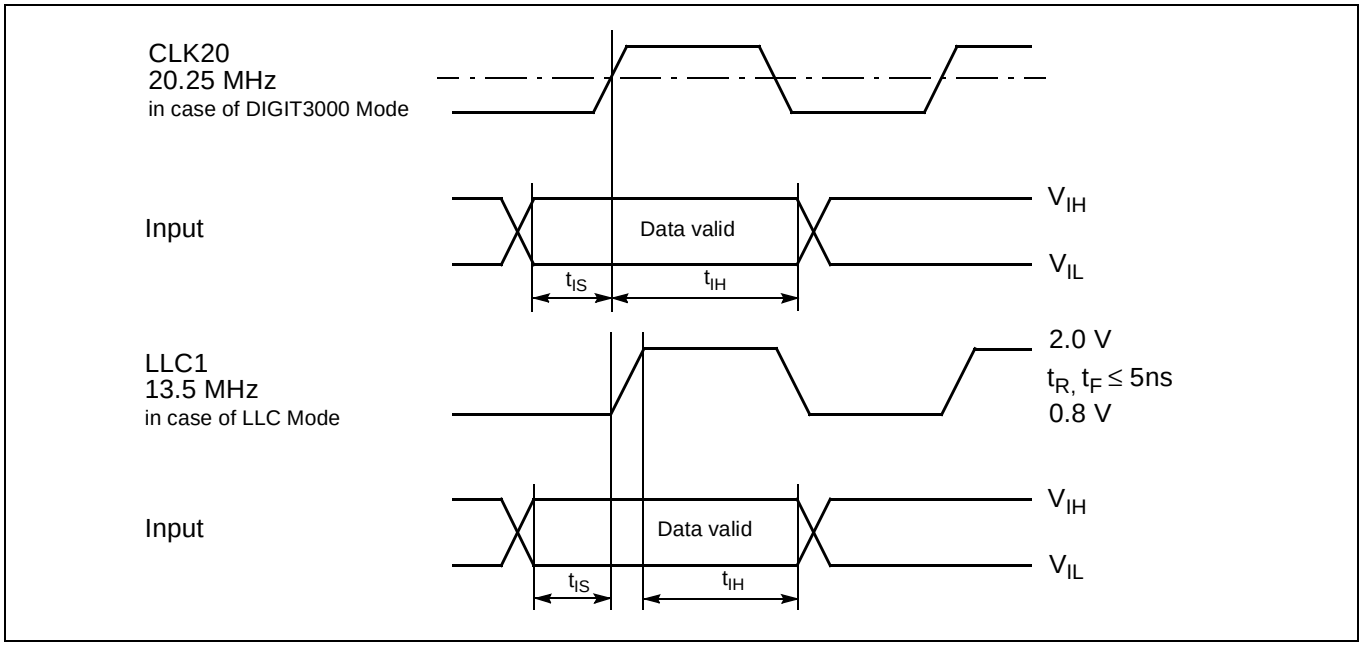


Fig. 4–18: Sync, control, and data inputs

4.6.4.13.Characteristics, Clock Output Specification

Line-Locked Clock Pins: LLC1, LLC2

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
C_L	Load capacitance	LLC1, LLC2	–	–	50	pF	
V_{OL}	Output Low Voltage	LLC1, LLC2	–	–	0.4	V	I_L = 2 mA
V_{OH}	Output High Voltage	LLC1, LLC2	2.4	–	–	V	I_H = –2 mA
13.5 MHz Line Locked Clock							
$1/T_1$	LLC1 Clock Frequency	LLC1	12.5	–	14.5	MHz	
t_{WL1}	LLC1 Clock Low Time	LLC1	25	–	–	ns	C_L = 30 pF
t_{WH1}	LLC1 Clock High Time	LLC1	25	–	–	ns	C_L = 30 pF
t_{R1}, t_{F1}	Clock Rise/Fall Time Clock	LLC1	–	–	5	ns	C_L = 30 pF
$1/T_2$	LLC2 Clock Frequency	LLC2	25	–	29	MHz	
t_{WL2}	LLC2 Clock Low Time	LLC2	5	–	–	ns	C_L = 30 pF
t_{WH2}	LLC2 Clock High Time	LLC2	10	–	–	ns	C_L = 30 pF
t_{R2}, t_{F2}	Clock Rise/Fall TimeClock	LLC2	–	–	8	ns	C_L = 30 pF
16 MHz Line Locked Clock							
$1/T_1$	LLC1 Clock Frequency	LLC1	14.8	–	17.2	MHz	
t_{WL1}	LLC1 Clock Low Time	LLC1	21	–	–	ns	C_L = 30 pF
t_{WH1}	LLC1 Clock High Time	LLC1	21	–	–	ns	C_L = 30 pF
t_{R1}, t_{F1}	Clock Rise/Fall TimeClock	LLC1	–	–	5	ns	C_L = 30 pF
$1/T_2$	LLC2 Clock Frequency	LLC2	29.6	–	34.4	MHz	
t_{WL2}	LLC2 Clock Low Time	LLC2	4	–	–	ns	C_L = 30 pF
t_{WH2}	LLC2 Clock High Time	LLC2	9	–	–	ns	C_L = 30 pF
t_{R2}, t_{F2}	Clock Rise/Fall TimeClock	LLC2	–	–	8	ns	C_L = 30 pF
common timings – all modes							
t_{SKS}	Clock Skew		0	–	4	ns	LLC1=13.5MHz, LLC2=27MHz

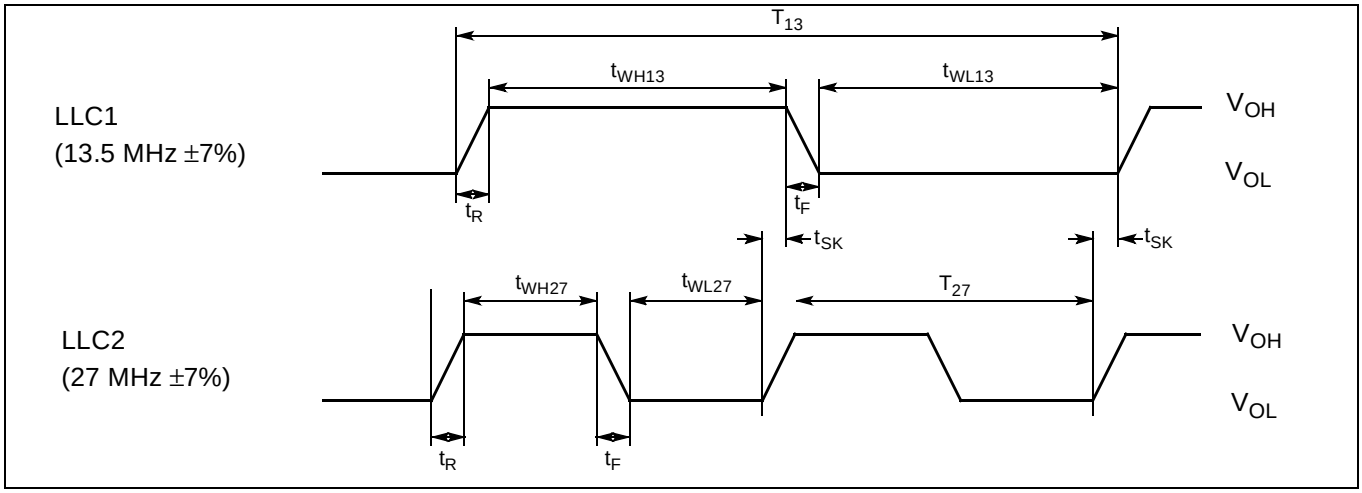
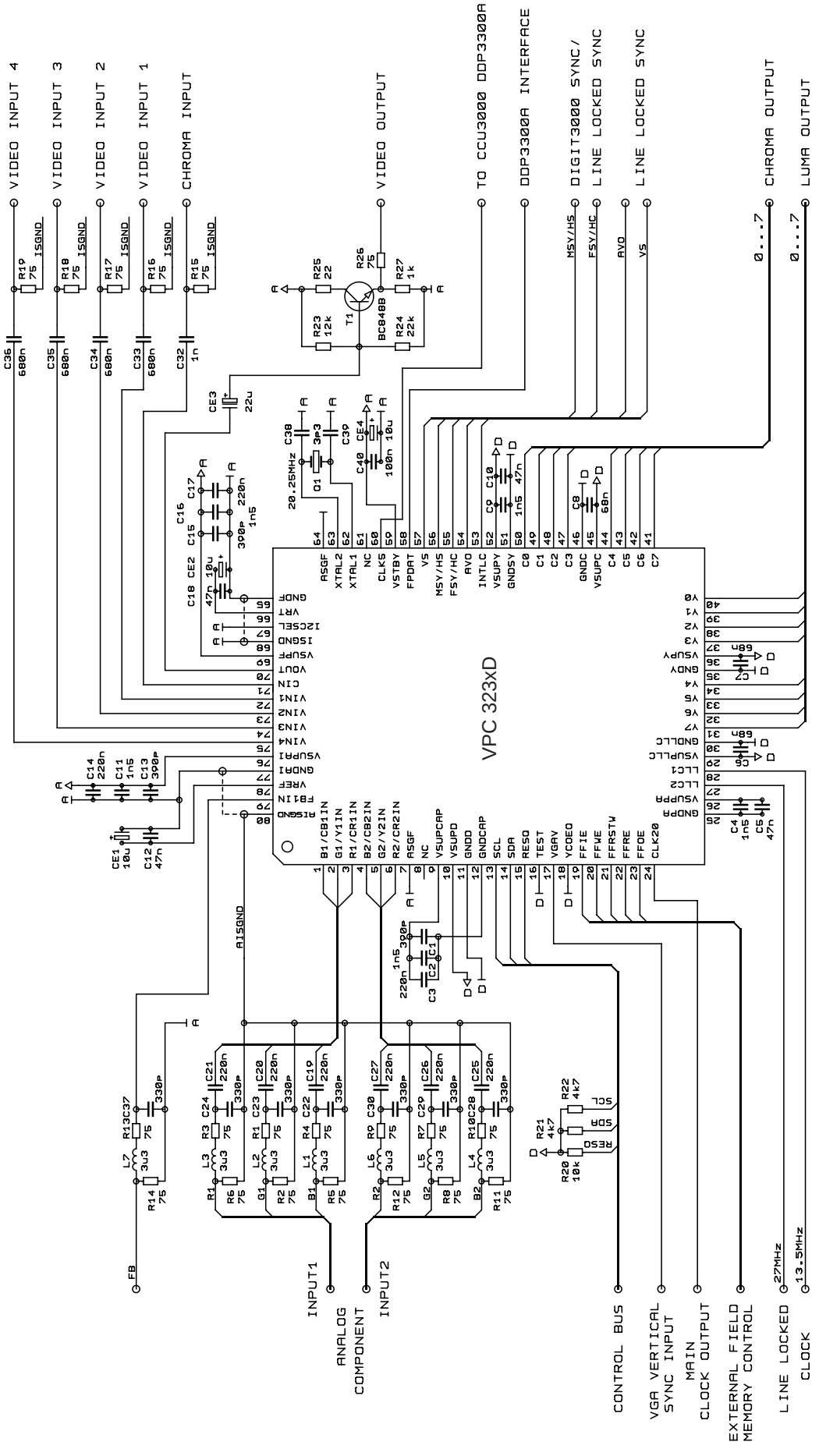


Fig. 4–19: Line-locked clock output pins

5. Application Circuit



5.1. Application Note: VGA mode with VPC 323xD

In 100-Hz TV applications it can be desirable to display a VGA-signal on the TV. In this case, a VGA-graphic card delivers the H, V, and RGB signals. These signals are fed "directly" to the back-end signal processing. The VPC generates a stable line-locked clock for the 100-Hz system in relation to the VGA sync signals.

While the V-sync is connected to the VGAV pin directly, the H-sync has to be pulse-shaped and amplitude adjusted until it is connected to one of the video input pins of the VPC. The recommended circuitry to filter the H sync is given in the figure below.

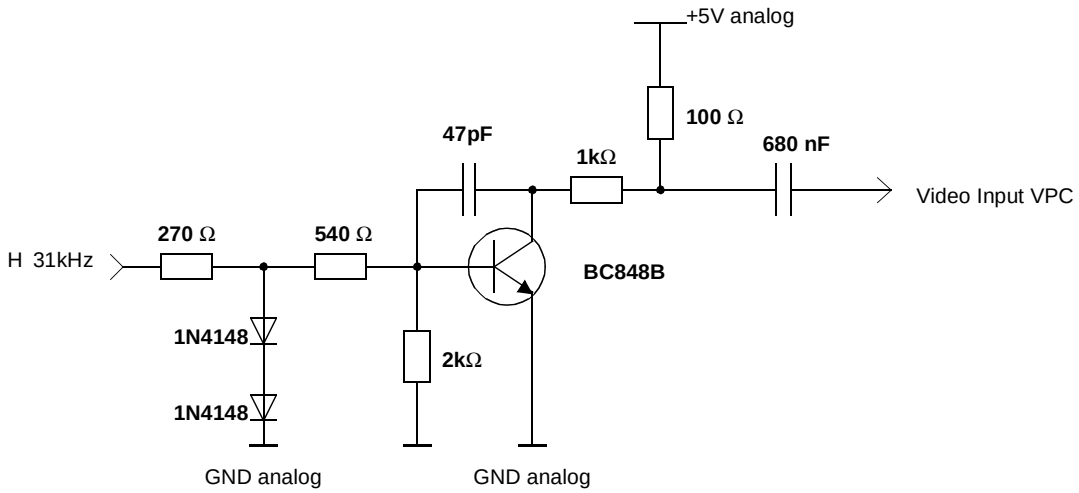


Fig. 5–1: Application circuit for horizontal VGA-input

5.2. Application Note: PIP Mode Programming

5.2.1. Procedure to Program a PIP Mode

For the VPC_{pip} or VPC_{single}:

1. set the scaler according to the PIP size to be used (see Table 2–11).
2. write the registers VPCMODE and PIPMODE according to the mode to be set.
3. in expert mode write the registers NLIN, NPIX and NPFB.
4. write the registers COLBGD, COLFR1, COLFR2, HSTR and VSTR, if a different value as the default one is used.
5. write the registers LINOFFS and PIXOFFS, if a different value as the default one or more than 4 inset pictures in the X or Y direction are used.
6. write the register PIPOPER to fill the frame and background of an inset picture. This step is repeated for all inset pictures in a multi PIP application.

For the VPC_{main}:

7. set the scaler to get a full size video (see Table 2–11).
8. write the registers VPCMODE and PIPMODE according to the mode to be set.
9. in expert mode write the registers NLIN, NPIX and NPFB.
10. write the registers COLBGD, HSTR and VSTR, if a different value as the default one is used.
11. write the register PIPOPER to start displaying PIP.

For the VPC_{pip} or VPC_{single}:

12. write the register PIPOPER to start filling a inset picture with live video.
13. Only for tuner scanning: write the register PIPOPER to stop filling a inset picture with live video and changing the channel.
14. repeat steps 12 and 13 for all inset pictures in a multi PIP application.
15. Only for VPC_{single}: write the register PIPOPER to start filling the main picture part outside the inset picture(s) with live video.

For the VPC_{main}:

16. write the registers HSTR and VSTR, if the PIP position should be changed.
17. write the register PIPOPER, to quit the PIP mode.

In an application with a single VPC, step 7 - 11 and 16 - 17 are dropped. Additionally, the free running mode should be set in the cases shown in Table 2–14.

5.2.2. I^2C Registers Programming for PIP Control

To program a PIP mode, the register VPCMODE, PIPMODE and PIPOPER should be written always, all other registers are used only in the expert mode or if the default values are modified (see Table 5–1).

Table 5–1: I^2C register programing for PIP control

I^2C register	update		
VPCMODE, PIPMODE, PIPOPER	should be written always		
COLBGD, COLFR1, COLFR2, HSTR, VSTR	should be written only, if the default values have to be modified		
LINOFFS, PIXOFFS	VPC_{pip}	VPC_{main}	VPC_{single}
	only used in expert mode, when more than 4 inset pictures in the X or Y direction are used.	not used.	only used if a different value as the default one or more than 4 inset pictures in the X or Y direction are used
NLIN, NPIX, NPFB	should be written, only in the expert mode. (In the predefined modes the default values are used.)		

Table 5–2: Limits of the I^2C register settings for programming a PIP mode

I^2C register	VPC_{main}	VPC_{pip} and VPC_{single}
NPFB	$NPFB \geq NPIX_{main} + X$, (X=2 for TI and X=0 for other field memories) and $NPFB \times NLIN_{main} \leq$ total field memory size	
NPIX	$0 < NPIX \leq NPFB - X$ and $0 < NPIX \leq NPEL_{fp}$	$0 < NPIX \leq NPELsp$
NLIN	$NPFB \times NLIN \leq$ total field memory size and $0 \leq NLIN < NROW_{fp}$	$0 \leq NLIN < NROW_{sp}$
HSTR	$0 \leq 4 \bullet HSTR < NPEL_{fp} - 4 \bullet NPIX_{main}$	$0 \leq HSTR < NPEL_{sp} - NPIX_{PIP}$
VSTR	$0 \leq VSTR < NROW_{fp} - NLIN_{main}$	$0 \leq VSTR < NROW_{sp} - NLIN_{PIP}$
PIXOFFS	not used	$0 \leq PIXOFFS < NPIX_{main}$ - (number of pixels of inset pictures to the right of PIXOFFS)
LINOFFS	not used	$0 \leq LINOFFS < NLIN_{main}$ - (number of lines of inset pictures below LINOFFS)

Notes:
- $NPIX_{main}$ and $NLIN_{main}$: correspond to VPC_{main}
- $NPIX_{PIP}$ and $NLIN_{PIP}$: correspond to VPC_{single} and VPC_{pip}
- $NROW_{fp}$ and $NPEL_{fp}$: number of lines per field and number of pixels per line of a full picture (e.g. $NROW_{fp}$=288, $NPEL_{fp}$= 720 for PAL at 13.5 MHz)
- $NROW_{sp}$ and $NPEL_{sp}$: number of lines per field and number of pixels per line of a inset picture

The limits of the I^2C register settings are given in Table 5–2. No range check and value limitation are carried out in the field memory controller. An illegal setting of these parameters leads to a error behavior of the PIP function.

The PIP display is controlled by the commands written into the register PIPOPER. For the VPC_{main}, the PIP display is turned on or off by the commends DIS-START and DISSTOP. For the VPC_{pip} and VPC_{single}, 8 commands are available:

– WRFRCOL1, WRFRCOL2: to fill the frame of a inset picture with the color COLFR1 or COLFR2,

– WRBGD, WRBGDNF: to fill a inset picture with the background color COLBGD,

– WRPIC, WRPICNF, WRSTOP: to start and stop to write a inset picture with the active video,

– WRMAIN: to start write the main picture part outside the inset picture(s) with the active video (only for VPC_{single}).

While WRPIC, WRSTOP, WRFRCOL1, WRFRCOL2 and WRBGD control a display with a frame (see Fig. 5–2), WRPICNF and WRBGDNF control a display without a frame (see Fig. 5–3). The number of the inset picture addressed by the current commend is given by bits NSPX and NSPY in the register PIPOPER.

In the display window, the coordinate of the upper-left corner of the inset picture with NSPX=0 and NSPY=0 is defined by the registers LINOFFS and PIXOFFS. If maximal 4x4 inset pictures are used, no new setting of these registers is needed. The default setting LINOFFS=0 and PIXOFFS=0 takes effect. If more than 4x4 inset pictures are involved in a PIP application, these inset pictures should be grouped, so that the inset pictures in each group can be addressed by bits NSPX and NSPY. For writing each group, the registers LINOFFS and PIXOFFS should be set correctly (see Fig.5–4).

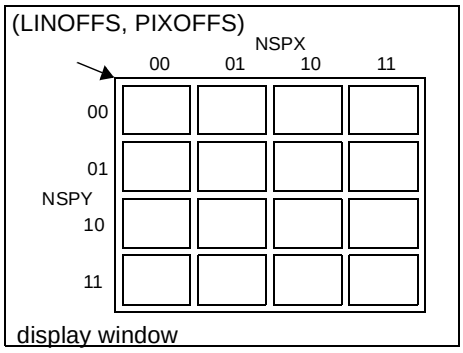


Fig. 5–2: 4x4 inset pictures with frame

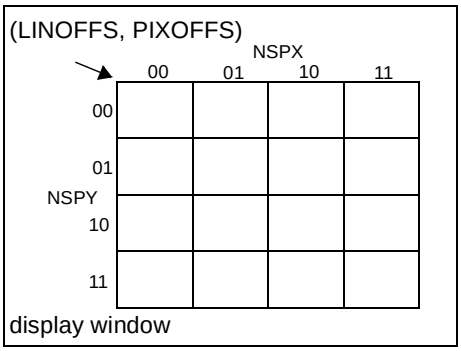


Fig. 5–3: 4x4 inset pictures without frame

5.2.3. Examples

5.2.3.1. Select Predefined Mode 2

Scaler settings for VPC_{pip}:

SCINC1 = h'600
FFLIM = h'168
NEWLIN = h'194
AVSTRT = h'86
AVSTOP = h'356
SC_PIP = h'11
SC_BRI = h'110
SC_CT = h'30
SC_MODE = h'00 (for S411=0)

PIP controller settings to start PIP display:

For the VPCpip:
VPCMODE = h'01
PIPMODE = h'02
PIPOPER = h'c0 (write the background)
wait until NEWCMD = 0
PIPOPER = h'a0 (write the frame)
wait until NEWCMD = 0
PIPOPER = h'80 (start writing PIP)

After that the PIP position can be changed via HSTR and VSTR registers. e.g. HSTR = h'03

For the VPC_{main}:
VPCMODE = h'05
PIPMODE = h'02
PIPOPER = h'80 (start display PIP)

PIP controller settings to stop PIP display:

For the VPC_{main}:
PIPOPER = h'90 (stop display PIP)

5.2.3.2. Select a Strobe Effect in Expert Mode

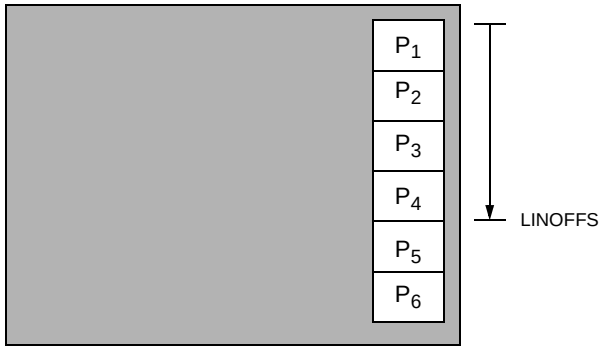


Fig. 5–4: Example of the expert mode

Scaler settings for VPC_{pip}:

SCINC1 = h'480
FFLIM = h'78
NEWLIN = h'194
AVSTRT = h'86
AVSTOP = h'356
SC_PIP = h'1f
SC_BRI = h'310
SC_CT = h'30
SC_MODE = h'00 (for S411=0)

PIP controller settings to show a strobe effect:

For the VPC_{pip}:
VPCMODE = h'01
PIPMODE = h'0f
VSTR = h'202
HSTR = h'101
NPIX = h'1c
NLIN = h'2c
NPFB = h'132

PIPOPER = h'c0 (write the background of P1)
wait until NEWCMD = 0
PIPOPER = h'a0 (write the frame of P1)
wait until NEWCMD = 0
PIPOPER = h'80 (start writing PIP of P1)
wait until NEWCMD = 0

PIPOPER = h'c4 (write the background of P2)
wait until NEWCMD = 0
PIPOPER = h'a4 (write the frame of P2)
wait until NEWCMD = 0
PIPOPER = h'84 (start writing PIP of P2)
wait until NEWCMD = 0

PIPOPER = h'c8 (write the background of P3)
wait until NEWCMD = 0
PIPOPER = h'a8 (write the frame of P3)
wait until NEWCMD = 0
PIPOPER = h'88 (start writing PIP of P3)

wait until NEWCMD = 0

PIPOPER = h'cc (write the background of P4)
wait until NEWCMD = 0
PIPOPER = h'ac (write the frame of P4)
wait until NEWCMD = 0
PIPOPER = h'8c (start writing PIP of P4)
wait until NEWCMD = 0

LINOFFS = h'2b8

PIPOPER = h'c0 (write the background of P5)
wait until NEWCMD = 0
PIPOPER = h'a0 (write the frame of P5)
wait until NEWCMD = 0
PIPOPER = h'80 (start writing PIP of P5)
wait until NEWCMD = 0

PIPOPER = h'c4 (write the background of P6)
wait until NEWCMD = 0
PIPOPER = h'a4 (write the frame of P6)
wait until NEWCMD = 0
PIPOPER = h'84 (start writing PIP of P6)

For the VPC_{main}:
VPCMODE = h'05
PIPMODE = h'0f
VSTR = h'201
HSTR = h'193
NPIX = h'1e
NLIN = h'116
NPFB = h'132
PIPOPER = h'80 (start display PIP)

PIP controller settings to stop PIP display:

For the VPC_{main}:
PIPOPER = h'90 (stop display PIP)

5.2.3.3. Select Predefined Mode 6 for Tuner Scanning

Scaler settings for VPC_{pip}:

SCINC1 = h'600
FFLIM = h'168
NEWLIN = h'194
AVSTRT = h'86
AVSTOP = h'356
SC_PIP = h'11
SC_BRI = h'110
SC_CT = h'30
SC_MODE = h'00 (for S411=0)

PIP controller settings for tuner scanning:

For the VPC_{pip}:
VPCMODE = h'01
PIPMODE = h'06

PIPOPER = h'c0 (write the background of P1)
wait until NEWCMD = 0
PIPOPER = h'a0 (write the frame of P1)
wait until NEWCMD = 0

PIPOPER = h'c1 (write the background of P2)
wait until NEWCMD = 0
PIPOPER = h'a1 (write the frame of P2)
wait until NEWCMD = 0

PIPOPER = h'c4 (write the background of P3)
wait until NEWCMD = 0
PIPOPER = h'a4 (write the frame of P3)
wait until NEWCMD = 0

PIPOPER = h'c5 (write the background of P4)
wait until NEWCMD = 0
PIPOPER = h'a5 (write the frame of P4)
wait until NEWCMD = 0

For the VPC_{main}:
VPCMODE = h'05
PIPMODE = h'46
PIPOPER = h'80 (start display multi PIP)

For the VPC_{pip}:
tune a channel
PIPOPER = h'80 (start writing PIP of P1)
wait until NEWCMD = 0
PIPOPER = h'90 (stop writing PIP of P1)
wait until NEWCMD = 0

tune an other channel
PIPOPER = h'81 (start writing PIP of P2)
wait until NEWCMD = 0
PIPOPER = h'91 (stop writing PIP of P2)
wait until NEWCMD = 0

tune an other channel
PIPOPER = h'84 (start writing PIP of P3)
wait until NEWCMD = 0
PIPOPER = h'94 (stop writing PIP of P3)
wait until NEWCMD = 0

tune an other channel
PIPOPER = h'85 (start writing PIP of P4)
wait until NEWCMD = 0
PIPOPER = h'95 (stop writing PIP of P4)
wait until NEWCMD = 0

The tuning and writing of the four inset pictures are repeated.

PIP controller settings to stop tuner scanning:

For the VPC_{main}:
PIPOPER = h'90 (stop display PIP)

6. Data Sheet History

1. Preliminary data sheet: “VPC 323XD Comb Filter Video Processor”, July 26, 2001, 6251-472-1PD. First release of the preliminary data sheet.

Micronas GmbH
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-761-517-0
Fax +49-761-517-2174
E-mail: docservice@micronas.com
Internet: www.micronas.com

Printed in Germany
Order No. 6251-472-1PD