HOLTEK

HT70XX
Voltage Detector

Features

- Low power consumption
- Low temperature coefficient
- Built-in high-stability reference source
- Built-in hysteresis characteristic
- TO-92 & SOT-89 package

Applications

- Battery checkers
- Level selectors
- Power failure detectors
- Microcomputer reset
- Battery memory backup
- Non-volatile RAM signal storage protectors

General Description

The HT70XX series is a set of three-terminal low power voltage detectors implemented in CMOS technology. Each voltage detector in the series detects a particular fixed voltage ranging from 1.5V to 7V. The voltage detectors consist of a high-precision and low power consumption standard voltage source, a comparator, hysteresis circuit, and an output driver. CMOS technology ensures low power consumption.

Although designed primarily as fixed voltage detectors, these devices can be used with external components to detect user specified threshold voltages (NMOS open drain type only).

Selection Table

Part No.	Detectable Voltage	Hysteresis Width	Tolerance
HT7024A	2.4V	0.12V	±5%
HT7027A	2.7V	0.135V	±5%
HT7033A/B	3.3V	0.165V	±5%
HT7039A	3.9V	0.195V	±5%
HT7044A/B	4.4V	0.22V	±5%
HT7050A	5V	0.25V	±5%
HT7070A	7V	0.35V	±5%

Note: The output type selection codes are:

NMOS open drain normal open, active low

PMOS open drain normal open, active high

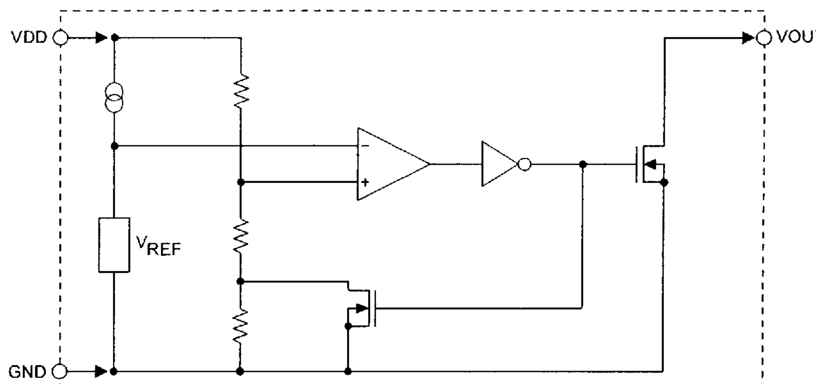
For example: The HT7070A is a 7V, NMOS open drain active low output

Output type selection table

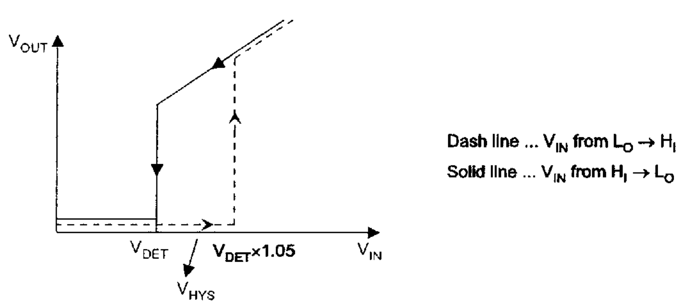
Type \ V_{OUT} \ V_{DD}	$V_{DD}>V_{DET}(+)$	$V_{DD}\le V_{DET}(-)$
A	Hi-Z	VSS
B	Hi-Z	VDD

Block Diagram

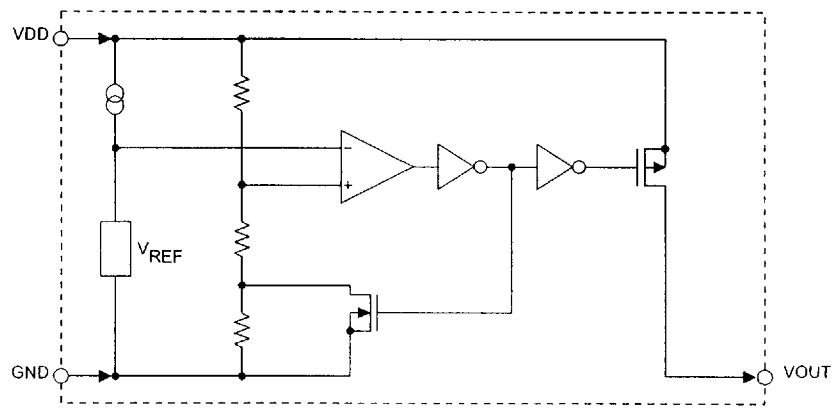
N channel open drain output (normal open; active low)



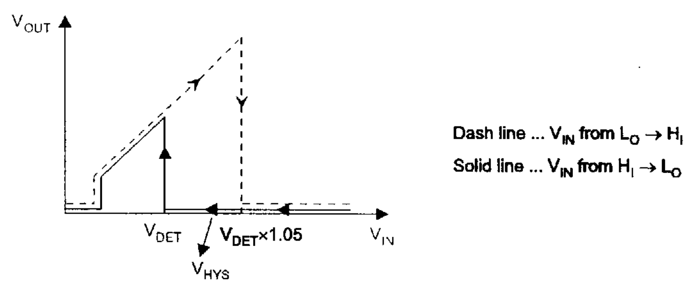
A type



P channel open drain output (normal open; active high)

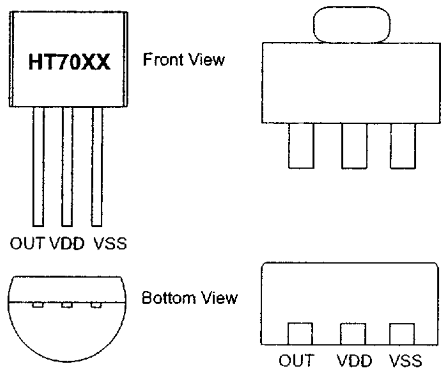


B type

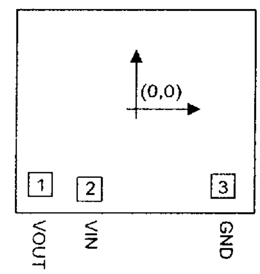


Pin Assignment

A. TO-92 **B. SOT-89**



Pad Assignment



Chip size: 1317 × 1158 $(\mu m)^2$

* The IC substrate should be connected to VDD in the PCB layout artwork.

Pad Coordinates

Unit: μm

Pad No.	X	Y
1	−483.30	−379.50
2	−234.60	−399.50
3	443.90	−386.00

Absolute Maximum Ratings

Supply Voltage .... −0.3V to 26V

Output Voltage .... V_{SS}−0.3V to V_{DD}+0.3V

Power Consumption 200mW

Output Current 50mA

Storage Temperature................. −50°C to 125°C

Operating Temperature .... 0°C to 70°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

HT7024A

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DET}	Hi→Lo Detectable Voltage	—	—	2.28	2.4	2.52	V
	Lo→Hi Detectable Voltage	—	—	2.325	2.52	2.772	V
V_{HYS}	Hysteresis Width	—	—	0.02 V_{DET}	0.05 V_{DET}	0.1 V_{DET}	V
I_{DD}	Operating Current	8	No load	—	4	7	μA
V_{DD}	Operating Voltage	—	—	1.5	—	24	V
I_{OL}	Output Sink Current	2	V_{OUT}=0.2V	0.5	1	—	mA
$\frac{\Delta V_{DET}}{\Delta T_A}$	Temperature Coefficient	—	0°C<Ta<70°C	—	±0.9	—	mV/°C

HT7027A

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DET}	Hi→Lo Detectable Voltage	—	—	2.565	2.7	2.835	V
	Lo→Hi Detectable Voltage	—	—	2.616	2.835	3.118	V
V_{HYS}	Hysteresis Width	—	—	0.02 V_{DET}	0.05 V_{DET}	0.1 V_{DET}	V
I_{DD}	Operating Current	8	No load	—	4	7	μA
V_{DD}	Operating Voltage	—	—	1.5	—	24	V
I_{OL}	Output Sink Current	2	V_{OUT}=0.2V	0.5	1	—	mA
$\frac{\Delta V_{DET}}{\Delta T_A}$	Temperature Coefficient	—	0°C<Ta<70°C	—	±0.9	—	mV/°C

HT7033A/B

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DET}	Hi→Lo Detectable Voltage	—	—	3.135	3.3	3.465	V
	Lo→Hi Detectable Voltage	—	—	3.197	3.465	3.811	V
V_{HYS}	Hysteresis Width	—	—	0.02 V_{DET}	0.05 V_{DET}	0.1 V_{DET}	V
I_{DD}	Operating Current	8	No load	—	4	7	μA
V_{DD}	Operating Voltage	—	—	1.5	—	24	V
I_{OL}	Output Sink Current	2.5	V_{OUT}=0.25V	1.2	2.5	—	mA
I_{OH}	Output Source Current	2.5	V_{OUT}=2.25V	–0.75	–1.5	—	mA
$\frac{\Delta V_{DET}}{\Delta T_A}$	Temperature Coefficient	—	0°C<Ta<70°C	—	±0.9	—	mV/°C

Note: HT7033A has no I_{OH}
HT7033B has no I_{OL}

HT7039A

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DET}	Hi→Lo Detectable Voltage	—	—	3.705	3.9	4.095	V
	Lo→Hi Detectable Voltage	—	—	3.779	4.095	4.504	V
V_{HYS}	Hysteresis Width	—	—	0.02 V_{DET}	0.05 V_{DET}	0.1 V_{DET}	V
I_{DD}	Operating Current	8	No load	—	4	7	μA
V_{DD}	Operating Voltage	—	—	1.5	—	24	V
I_{OL}	Output Sink Current	2.5	V_{OUT}=0.25V	1.2	2.5	—	mA
$\frac{\Delta V_{DET}}{\Delta T_A}$	Temperature Coefficient	—	0°C<Ta<70°C	—	0.9	—	mV/°C

HT7044A/B

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DET}	Hi→Lo Detectable Voltage	—	—	4.18	4.4	4.62	V
	Lo→Hi Detectable Voltage	—	—	4.263	4.62	5.082	V
V_{HYS}	Hysteresis Width	—	—	0.02 V_{DET}	0.05 V_{DET}	0.1 V_{DET}	V
I_{DD}	Operating Current	8	No load	—	4	7	μA
V_{DD}	Operating Voltage	—	—	1.5	—	24	V
I_{OL}	Output Sink Current	3.6	V_{OUT}=0.36V	3	6	—	mA
I_{OH}	Output Source Current	3.6	V_{OUT}=3.2V	-1	-2	—	mA
$\frac{\Delta V_{DET}}{\Delta T_A}$	Temperature Coefficient	—	0°C<Ta<70°C	—	±0.9	—	mV/°C

Note: HT7044A has no I_{OH}

HT7044B has no I_{OL}

HT7050A

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DET}	Hi→Lo Detectable Voltage	—	—	4.75	5	5.25	V
	Lo→Hi Detectable Voltage	—	—	4.845	5.25	5.775	V
V_{HYS}	Hysteresis Width	—	—	0.02 V_{DET}	0.05 V_{DET}	0.1 V_{DET}	V
I_{DD}	Operating Current	8	No load	—	4	7	μA
V_{DD}	Operating Voltage	—	—	2.1	—	24	V
I_{OL}	Output Sink Current	3.6	V_{OUT}=0.36V	3	6	—	mA
$\frac{\Delta V_{DET}}{\Delta T_A}$	Temperature Coefficient	—	0°C<Ta<70°C	—	±0.9	—	mV/°C

HT7070A

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DET}	Hi→Lo Detectable Voltage	—	—	6.65	7	7.35	V
	Lo→Hi Detectable Voltage	—	—	6.783	7.35	8.085	V
V_{HYS}	Hysteresis Width	—	—	0.02 V_{DET}	0.05 V_{DET}	0.1 V_{DET}	V
I_{DD}	Operating Current	8	No load	—	4	7	μA
V_{DD}	Operating Voltage	—	—	2.1	—	24	V
I_{OL}	Output Sink Current	5	V_{OUT}=0.5V	5	10	—	mA
$\frac{\Delta V_{DET}}{\Delta T_A}$	Temperature Coefficient	—	0°C<Ta<70°C	—	±0.9	—	mV/°C

Functional Description

The HT70XX series is a set of voltage detectors equipped with a high stability voltage reference which is connected to the negative input of a comparator— denoted as V_{REF} in the following figure for NMOS output voltage detector.

When the voltage drop to the positive input of the comparator (i,e,V_B) is higher than V_{REF}, VOUT goes high, M1 turns off, and V_B is expressed as V_{BH}=VDD×(RB+RC)/(RA+RB+RC). If VDD is decreased so that V_B falls to a value less than V_{REF}, the comparator output inverts from high to low, VOUT goes low, V_C is high, M1 turns on, RC is bypassed, and V_B becomes: V_{BL}=VDD×RB/(RA+RB), which is less than V_{BH}. By so doing, the comparator output will stay low to prevent the circuit from oscillating when $V_B \approx V_{REF}$.

If VDD falls below the minimum operating voltage, the output becomes undefined. When VDD goes from low to VDD×RB/(RA+RB) > V_{REF}, the comparator output and VOUT goes high.

The detectable voltage is defined as:

$$V_{DET}(-) = \frac{RA + RB + RC}{RB + RC} \times V_{REF}$$

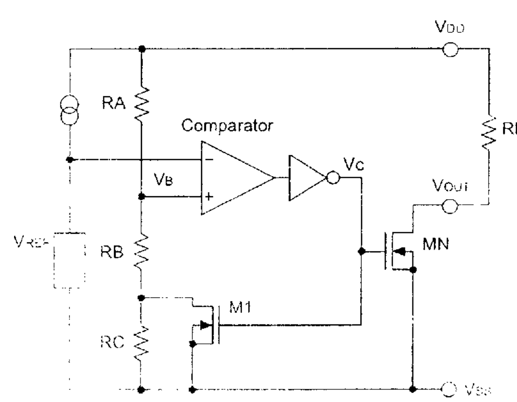
The release voltage is defined as:

$$V_{DET}(+) = \frac{RA + RB}{RB} \times V_{REF}$$

The hysteresis width is:

$$V_{HYS} = V_{DET}(+) - V_{DET}(-)$$

The figure demonstrates the NMOS output type with positive output polarity (VOUT is normally open, active low). The HT70XX series also supplies options for other output types with active high outputs. Application circuits shown are examples of positive output polarity (normally open, active low) unless otherwise specified.



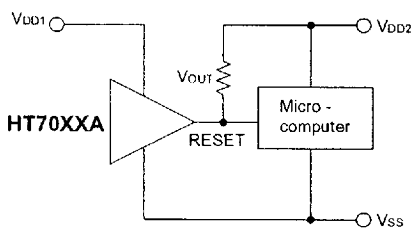
NMOS output voltage detector (HT70XXA)

Application Circuits

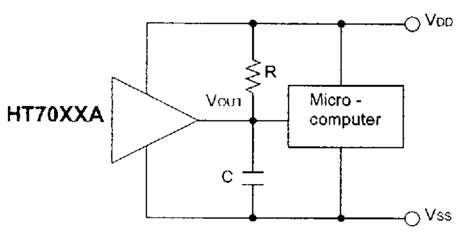
Microcomputer reset circuit

Normally a reset circuit is required to protect the microcomputer system from malfunctions due to power line interruptions. The following examples show how different output configurations perform a reset function in various systems.

- NMOS open drain output application for separate power supply

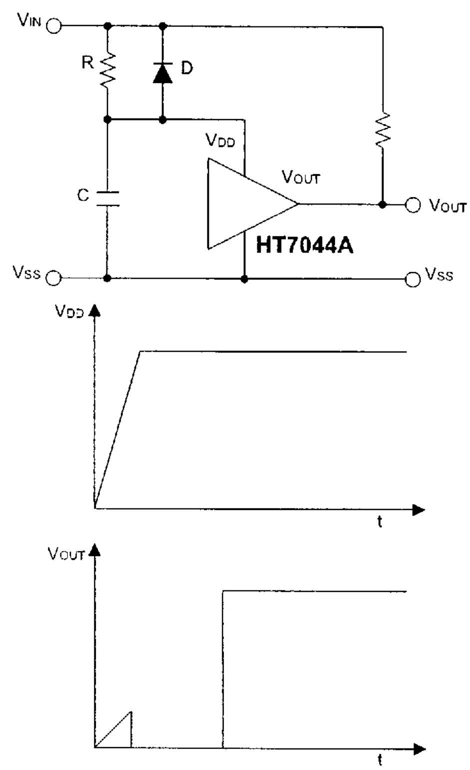


- NMOS open drain output application with R-C delay



Power-on reset circuit

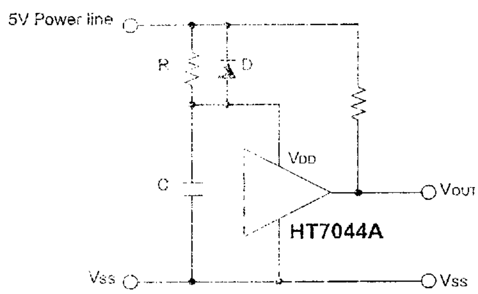
With several external components, the NMOS open drain type of the HT70XX series can be used to perform a power-on reset function as shown:



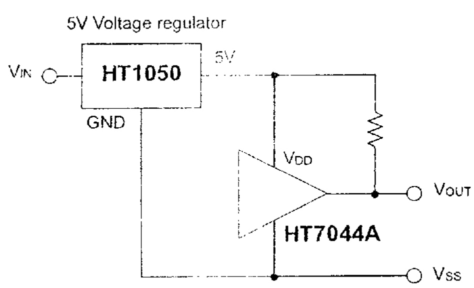
5V power line monitoring circuit

Generally, a minimum operating voltage of 4.5V is guaranteed in a 5V power line system. The HT7044A is recommended for use as 5V power line monitoring circuit.

• 5V power line monitor with power-on reset



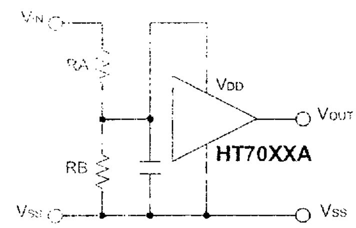
• with 5V voltage regulator



Change of detectable voltage

If the required voltage is not found in the standard product selection table, it is possible to change it by using external resistance dividers or diodes.

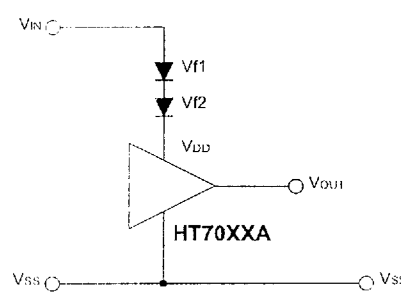
• Varying the detectable voltage with a resistance divider



$$\text{Detectable voltage} = \frac{RA + RB}{RB} \times V_{DET}$$

$$\text{Hysteresis width} = \frac{RA + RB}{RB} \times V_{HYS}$$

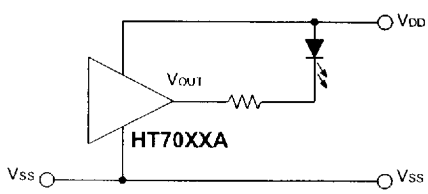
• Varying the detectable voltage with a diode



$$\text{Detectable Voltage} = V_{f1} + V_{f2} + V_{DET}$$

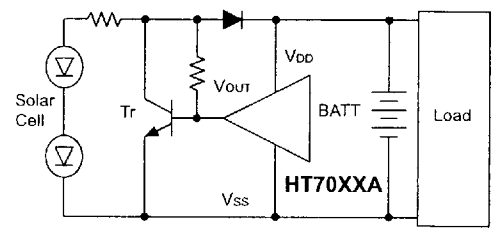
Malfunction analysis

The following circuit demonstrates the way a circuit analyzes malfunctions by monitoring the variation or spike noise of power supply voltage.



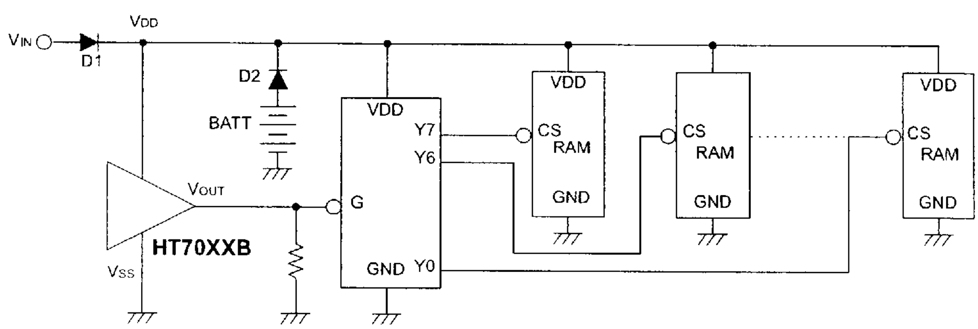
Charge monitoring circuit

The following circuit shows a charged monitor for protection against battery deterioration by overcharging. When the voltage of the battery is higher than the set detectable voltage, the transistor turns on to bypass the charge current, protecting the battery from overcharging.



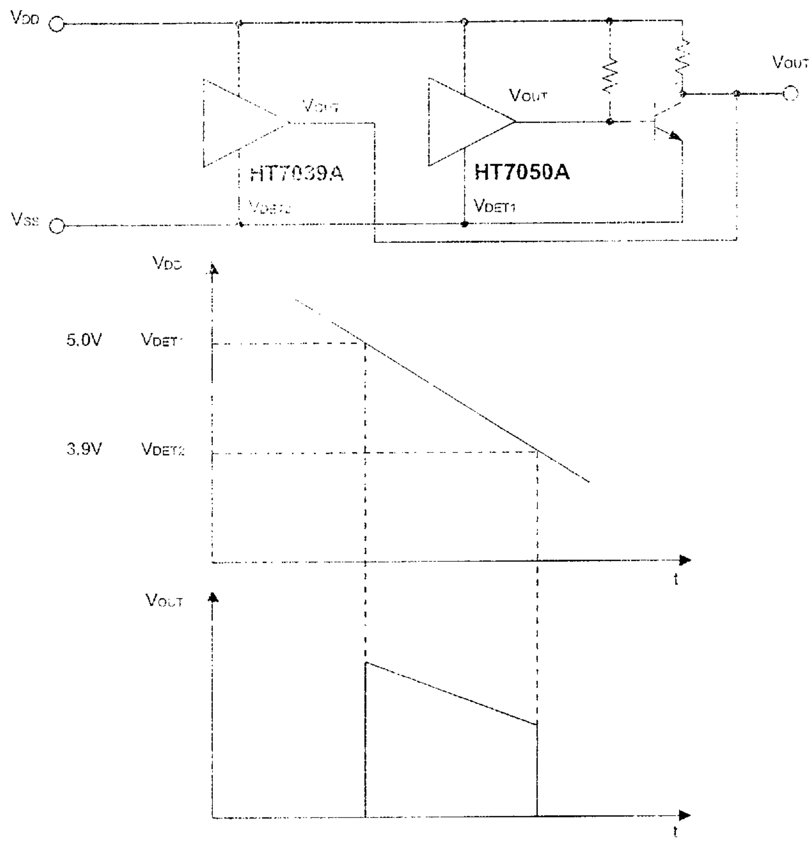
Battery backup for memories

An application example of battery backup for memory data retention is shown below. During battery backup (VDD below detectable voltage), the HT70XXB output goes high to disable the chip select decoder and to force the memory chips into a non-access state so as to retain the data.



Level selector

The following diagram illustrates a logic level selector.



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