INITIAL RELEASE

Final Electrical Specifications

LTC2846

# 3.3V Software-Selectable Multiprotocol Transceiver with Termination

January 2002

## FEATURES

- **Software-Selectable Transceiver Supports: RS232, RS449, EIA530, EIA530-A, V.35, V.36, X.21**
- **Operates from Single 3.3V Supply**
- 1.2MHz Boost Switching Regulator for 3.3V to 5V Conversion
- On-Chip Cable Termination
- Complete DTE or DCE Port with LTC2844
- Small Footprint

## APPLICATIONS

- Data Networking
- CSU and DSU
- Data Routers

## DESCRIPTION

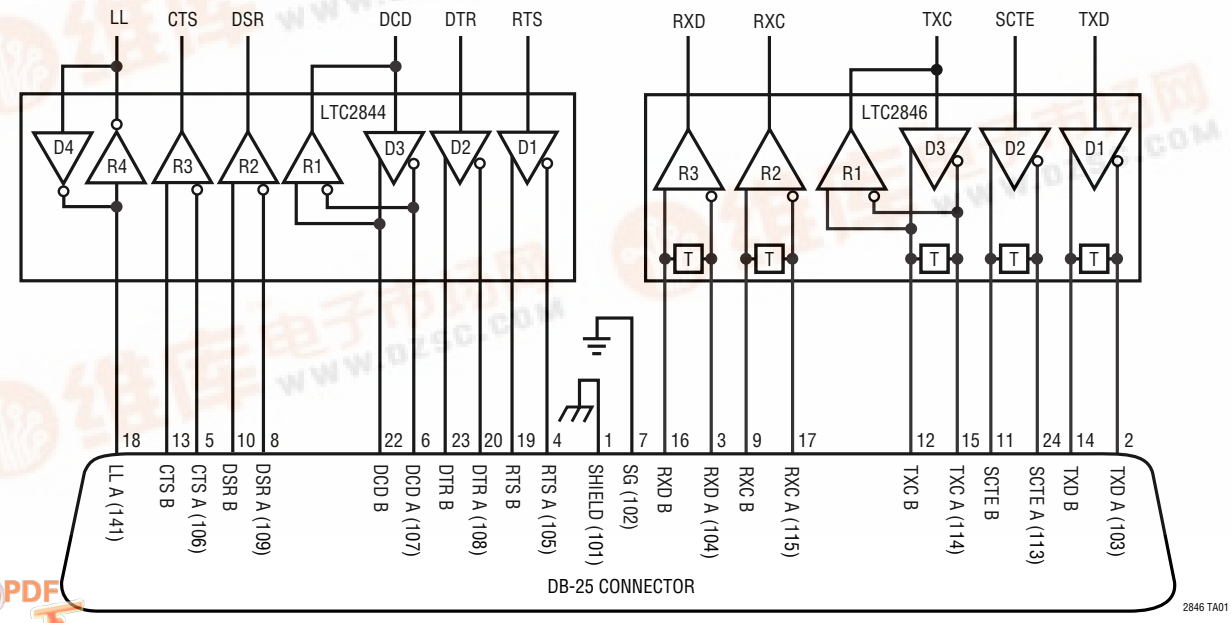
The LTC®2846 is a 3-driver/3-receiver multiprotocol transceiver with on-chip cable termination. When combined with the LTC2844, this chip set forms a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA530, EIA530-A, V.35, V.36 and X.21 protocols. All necessary cable termination is provided inside the LTC2846. The LTC2846 has a boost regulator that takes in a 3.3V input and switches at 1.2MHz, allowing the use of tiny, low cost capacitors and inductors 2mm or less in height.

The 5V output drives an internal charge pump that requires only five space-saving surface mounted capacitors. The LTC2846 is available in a 36-lead SSOP surface mount package.



## TYPICAL APPLICATION

**Complete DTE or DCE Multiprotocol Serial Interface with DB-25 Connector**

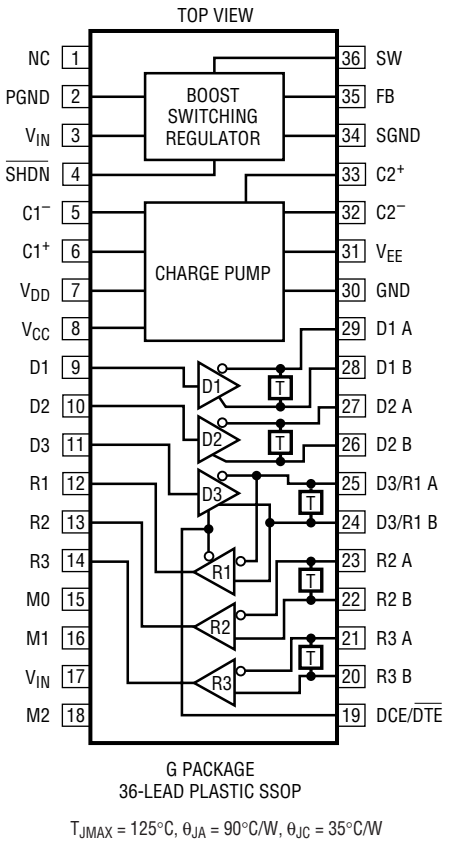


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{CC}$ Voltage ..... –0.3V to 6.5V
$V_{IN}$ Voltage ..... –0.3V to 6.5V
Input Voltage
  Transmitters ..... –0.3V to ($V_{CC}$ + 0.3V)
  Receivers ..... –18V to 18V
  Logic Pins ..... –0.3V to ($V_{CC}$ + 0.3V)
Output Voltage
  Transmitters ..... ($V_{EE}$ – 0.3V) to ($V_{DD}$ + 0.3V)
  Receivers ..... –0.3V to ($V_{IN}$ + 0.3V)
  $V_{EE}$ ..... –10V to 0.3V
  $V_{DD}$ ..... –0.3V to 10V
Short-Circuit Duration
  Transmitter Output ..... Indefinite
  Receiver Output ..... Indefinite
  $V_{EE}$ ..... 30 sec
SW Voltage ..... –0.4V to 36V
FB Voltage ..... –0.3V to 2.5V
Current into FB Pin ..... ±1mA
$\overline{SHDN}$ Voltage ..... –0.3V to 10V
Operating Temperature Range
  LTC2846C ..... 0°C to 70°C
  LTC2846I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION




G PACKAGE
36-LEAD PLASTIC SSOP

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 90°C/W, $\theta_{JC}$ = 35°C/W

| ORDER PART NUMBER |
|---|
| LTC2846CG |
| LTC2846IG |

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 5V, $V_{IN}$ = 3.3V, $V_{\overline{SHDN}}$ = $V_{IN}$, unless otherwise noted (Notes 2, 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Supplies** | | | | | | | |
| $I_{CC}$ | $V_{IN}$ Supply Current (DCE Mode, All Digital Pins = GND or $V_{IN}$) | RS530, RS530-A, X.21 Modes, No Load | | | 14 | | mA |
| | | RS530, RS530-A, X.21 Modes, Full Load | ● | | 100 | 130 | mA |
| | | V.35 Mode | ● | | 126 | 170 | mA |
| | | V.28 Mode, No Load | | | 20 | | mA |
| | | V.28 Mode, Full Load | ● | | 35 | 75 | mA |
| | | No-Cable Mode | ● | | 300 | 900 | µA |
| $P_D$ | Internal Power Dissipation (DCE Mode) | RS530, RS530-A, X.21 Modes, Full Load | | | 410 | | mW |
| | | V.35 Mode, Full Load | | | 625 | | mW |
| | | V.28 Mode, Full Load | | | 150 | | mW |
| $V^+$ | Positive Charge Pump Output Voltage | V.11 or V.28 Mode, No Load | ● | 8 | 9.3 | | V |
| | | V.35 Mode | ● | 7 | 8.0 | | V |
| | | V.28 Mode, with Load | ● | 8 | 8.7 | | V |
| | | V.28 Mode, with Load, $I_{DD}$ = 10mA | | | 6.5 | | V |

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 5V, $V_{IN}$ = 3.3V, $V_{\overline{SHDN}}$ = $V_{IN}$, unless otherwise noted (Notes 2, 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V^-$ | Negative Charge Pump Output Voltage | V.28 Mode, No Load | | | –9.6 | | V |
| | | V.28 Mode, Full Load | ● | –7.5 | –8.5 | | V |
| | | V.35 Mode | ● | –5.5 | –6.5 | | V |
| | | RS530, RS530-A, X.21 Modes, Full Load | ● | –4.5 | –6.0 | | V |
| $f_{OSC}$ | Charge Pump Oscillator Frequency | | | | 500 | | kHz |
| $t_r$ | Charge Pump Rise Time | No-Cable Mode/Power-Off to Normal Operation | | | 2 | | ms |
| **Logic Inputs and Outputs** | | | | | | | |
| $V_{IH}$ | Logic Input High Voltage | D1, D2, D3, M0, M1, M2, DCE/$\overline{DTE}$ | ● | 2.0 | | | V |
| | | $\overline{SHDN}$ | | 2.4 | | | V |
| $V_{IL}$ | Logic Input Low Voltage | D1, D2, D3, M0, M1, M2, DCE/$\overline{DTE}$ | ● | | | 0.8 | V |
| | | $\overline{SHDN}$ | | | | 0.5 | V |
| $I_{IN}$ | Logic Input Current | D1, D2, D3 | ● | | | ±10 | µA |
| | | M0, M1, M2, DCE/$\overline{DTE}$ = GND | ● | –30 | –75 | –120 | µA |
| | | M0, M1, M2, DCE/$\overline{DTE}$ = $V_{IN}$ | ● | | | ±10 | µA |
| | | $\overline{SHDN}$ = GND | | | | ±0.1 | µA |
| | | $\overline{SHDN}$ = 3V | | | 16 | 32 | µA |
| $V_{OH}$ | Output High Voltage | $I_O$ = –3mA | ● | 2.7 | 3 | | V |
| $V_{OL}$ | Output Low Voltage | $I_O$ = 1.6mA | ● | | 0.2 | 0.4 | V |
| $I_{OSR}$ | Output Short-Circuit Current | 0V ≤ $V_O$ ≤ $V_{IN}$ | ● | | | ±50 | mA |
| $I_{OZR}$ | Three-State Output Current | M0 = M1 = M2 = $V_{IN}$, $V_O$ = GND | ● | –30 | –85 | –160 | µA |
| | | M0 = M1 = M2 = $V_{IN}$, $V_O$ = $V_{IN}$ | ● | | | ±10 | µA |
| **V.11 Driver** | | | | | | | |
| $V_{ODO}$ | Open Circuit Differential Output Voltage | $R_L$ = 1.95k (Figure 1) | ● | | | ±5 | V |
| $V_{ODL}$ | Loaded Differential Output Voltage | $R_L$ = 50Ω (Figure 1) | | 0.5$V_{ODO}$ | | 0.67$V_{ODO}$ | V |
| | | $R_L$ = 50Ω (Figure 1) | ● | ±2 | | | V |
| $\Delta V_{OD}$ | Change in Magnitude of Differential Output Voltage | $R_L$ = 50Ω (Figure 1) | ● | | | 0.2 | V |
| $V_{OC}$ | Common Mode Output Voltage | $R_L$ = 50Ω (Figure 1) | ● | | | 3 | V |
| $\Delta V_{OC}$ | Change in Magnitude of Common Mode Output Voltage | $R_L$ = 50Ω (Figure 1) | ● | | | 0.2 | V |
| $I_{SS}$ | Short-Circuit Current | $V_{OUT}$ = GND | | | | ±150 | mA |
| $I_{OZ}$ | Output Leakage Current | $\lvert V_A \rvert$ and $\lvert V_B \rvert$ ≤ 0.25V, Power Off or No-Cable Mode or Driver Disabled | ● | | ±1 | ±100 | µA |
| $t_r$, $t_f$ | Rise or Fall Time | (Figures 2, 13) | ● | 2 | 15 | 25 | ns |
| $t_{PLH}$ | Input to Output Rising | (Figures 2, 13) | ● | 15 | 40 | 65 | ns |
| $t_{PHL}$ | Input to Output Falling | (Figures 2, 13) | ● | 15 | 40 | 65 | ns |
| $\Delta t$ | Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$ | (Figures 2, 13) | ● | 0 | 3 | 12 | ns |
| $t_{SKEW}$ | Output to Output Skew | (Figures 2, 13) | | | 3 | | ns |

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 5V, $V_{IN}$ = 3.3V, $V_{\overline{SHDN}}$ = $V_{IN}$, unless otherwise noted (Notes 2, 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **V.11 Receiver** | | | | | | | |
| $V_{TH}$ | Input Threshold Voltage | $-7V \le V_{CM} \le 7V$ | ● | –0.2 | | 0.2 | V |
| $\Delta V_{TH}$ | Input Hysteresis | $-7V \le V_{CM} \le 7V$ | ● | | 15 | 40 | mV |
| $R_{IN}$ | Input Impedance | $-7V \le V_{CM} \le 7V$ (Figure 3) | ● | 100 | 103 | | Ω |
| $t_r$, $t_f$ | Rise or Fall Time | $C_L$ = 50pF (Figures 4, 14) | | | 15 | | ns |
| $t_{PLH}$ | Input to Output Rising | $C_L$ = 50pF (Figures 4, 14) | ● | | 50 | 90 | ns |
| $t_{PHL}$ | Input to Output Falling | $C_L$ = 50pF (Figures 4, 14) | ● | | 50 | 90 | ns |
| $\Delta t$ | Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$ | $C_L$ = 50pF (Figures 4, 14) | ● | 0 | 4 | 25 | ns |
| **V.35 Driver** | | | | | | | |
| $V_{OD}$ | Differential Output Voltage | Open Circuit, $R_L$ = 1.95k (Figure 5)<br>With Load, $-4V \le V_{CM} \le 4V$ (Figure 6) | ● | <br>±0.44 | <br>±0.55 | ±1.2<br>±0.66 | V<br>V |
| $V_{OA}$, $V_{OB}$ | Single-Ended Output Voltage | Open Circuit, $R_L$ = 1.95k (Figure 5) | ● | | | ±1.2 | V |
| $V_{OC}$ | Transmitter Output Offset | $R_L$ = 50Ω (Figure 5) | ● | | | ±0.6 | V |
| $I_{OH}$ | Transmitter Output High Current | $V_A$, $V_B$ = 0V | ● | –9 | –11 | –13 | mA |
| $I_{OL}$ | Transmitter Output Low Current | $V_A$, $V_B$ = 0V | ● | 9 | 11 | 13 | mA |
| $I_{OZ}$ | Transmitter Output Leakage Current | $\lvert V_A \rvert$ and $\lvert V_B \rvert \le 0.25V$ | ● | | ±1 | ±100 | µA |
| $R_{OD}$ | Transmitter Differential Mode Impedance | | ● | 50 | 100 | 150 | Ω |
| $R_{OC}$ | Transmitter Common Mode Impedance | $-2V \le V_{CM} \le 2V$ (Figure 7) | | 135 | 150 | 165 | Ω |
| $t_r$, $t_f$ | Rise or Fall Time | (Figures 8, 13) | | | 5 | | ns |
| $t_{PLH}$ | Input to Output | (Figures 8, 13) | ● | 15 | 35 | 65 | ns |
| $t_{PHL}$ | Input to Output | (Figures 8, 13) | ● | 15 | 35 | 65 | ns |
| $\Delta t$ | Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$ | (Figures 8, 13) | ● | | 0 | 16 | ns |
| $t_{SKEW}$ | Output to Output Skew | (Figures 8, 13) | | | 4 | | ns |
| **V.35 Receiver** | | | | | | | |
| $V_{TH}$ | Differential Receiver Input Threshold Voltage | $-2V \le V_{CM} \le 2V$ (Figure 9) | ● | –0.2 | | 0.2 | V |
| $\Delta V_{TH}$ | Receiver Input Hysteresis | $-2V \le V_{CM} \le 2V$ (Figure 9) | ● | | 15 | 40 | mV |
| $R_{ID}$ | Receiver Differential Mode Impedance | $-2V \le V_{CM} \le 2V$ | ● | 90 | 103 | 110 | Ω |
| $R_{IC}$ | Receiver Common Mode Impedance | $-2V \le V_{CM} \le 2V$ (Figure 10) | | 135 | 150 | 165 | Ω |
| $t_r$, $t_f$ | Rise or Fall Time | $C_L$ = 50pF (Figures 4, 14) | | | 15 | | ns |
| $t_{PLH}$ | Input to Output | $C_L$ = 50pF (Figures 4, 14) | ● | | 50 | 90 | ns |
| $t_{PHL}$ | Input to Output | $C_L$ = 50pF (Figures 4, 14) | ● | | 50 | 90 | ns |
| $\Delta t$ | Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$ | $C_L$ = 50pF (Figures 4, 14) | ● | 0 | 4 | 25 | ns |
| **V.28 Driver** | | | | | | | |
| $V_O$ | Output Voltage | Open Circuit<br>$R_L$ = 3k (Figure 11) | ●<br>● | <br>±5 | <br>±8.5 | ±10 | V<br>V |
| $I_{SS}$ | Short-Circuit Current | $V_{OUT}$ = GND | ● | | | ±150 | mA |
| $R_{OZ}$ | Power-Off Resistance | $-2V < V_O < 2V$, Power Off or No-Cable Mode | ● | 300 | | | Ω |
| SR | Slew Rate | $R_L$ = 7k, $C_L$ = 0 (Figures 11, 15) | ● | 4 | | 30 | V/µs |
| $t_{PLH}$ | Input to Output | $R_L$ = 3k, $C_L$ = 2500pF (Figures 11, 15) | ● | | 1.5 | 2.5 | µs |
| $t_{PHL}$ | Input to Output | $R_L$ = 3k, $C_L$ = 2500pF (Figures 11, 15) | ● | | 1.5 | 2.5 | µs |

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 5V, $V_{IN}$ = 3.3V, $V_{\overline{SHDN}}$ = $V_{IN}$, unless otherwise noted (Notes 2, 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **V.28 Receiver** | | | | | | | |
| $V_{THL}$ | Input Low Threshold Voltage | (Figure 12) | ● | 0.8 | 1.2 | | V |
| $V_{TLH}$ | Input High Threshold Voltage | (Figure 12) | ● | | 1.2 | 2 | V |
| $\Delta V_{TH}$ | Receiver Input Hysteresis | (Figure 12) | ● | 0 | 0.05 | 0.3 | V |
| $R_{IN}$ | Receiver Input Impedance | $-15V \le V_A \le 15V$ | ● | 3 | 5 | 7 | kΩ |
| $t_r$, $t_f$ | Rise or Fall Time | $C_L$ = 50pF (Figures 12, 16) | | | 15 | | ns |
| $t_{PLH}$ | Input to Output | $C_L$ = 50pF (Figures 12, 16) | ● | | 60 | 300 | ns |
| $t_{PHL}$ | Input to Output | $C_L$ = 50pF (Figures 12, 16) | ● | | 160 | 300 | ns |
| **Boost Switching Regulator (Notes 4)** | | | | | | | |
| $V_{IN}$ | Operating Voltage | | | 3 | 3.3 | 3.6 | V |
| $V_{FB}$ | Feedback Voltage | | ● | 1.230 | 1.255 | 1.280 | V |
| $I_{FB}$ | FB Pin Bias Current | $V_{FB}$ = 1.255V | ● | | 120 | 360 | nA |
| $I_Q$ | Quiescent Current<br>Quiescent Current in Shutdown | $V_{\overline{SHDN}}$ = 2.4V, Not Switching<br>$V_{\overline{SHDN}}$ = 0V, $V_{IN}$ = 3V | | | 4.2<br>0.01 | 6<br>1 | mA<br>µA |
| $\Delta V_{FB(LR)}$ | Reference Line Regulation | $3V \le V_{IN} \le 3.6V$ | | | 0.01 | 0.05 | %/V |
| f | Switching Frequency | | ● | 0.85 | 1.2 | 1.6 | MHz |
| $DC_{MAX}$ | Maximum Duty Cycle | | ● | 82 | 90 | | % |
| $I_{LIM}$ | Switch Current Limit | (Note 5) | | 1 | 1.2 | 2 | A |
| $V_{SAT}$ | Switch $V_{CESAT}$ | $I_{SW}$ = 900mA | | | 350 | | mV |
| $I_{LEAK}$ | Switch Leakage Current | $V_{SW}$ = 5V | | | 0.01 | 1 | µA |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

**Note 2:** All currents into device pins are positive; all currents out of device are negative. All voltages are referenced to device ground unless otherwise specified.

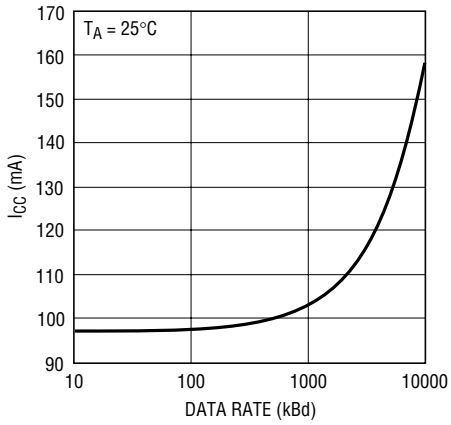
**Note 3:** All typicals are given for $V_{CC}$ = 5V, $V_{IN}$ = 3.3V, $C_{VCC}$ = $C_{VIN}$ = 10µF, $C_{VDD}$ = 1µF, $C_{VEE}$ = 3.3µF and $T_A$ = 25°C.

**Note 4:** The Boost Regulator is specified for $V_{IN}$ = 3V unless otherwise noted.

**Note 5:** Current limit guaranteed by design and/or correlation to static test.

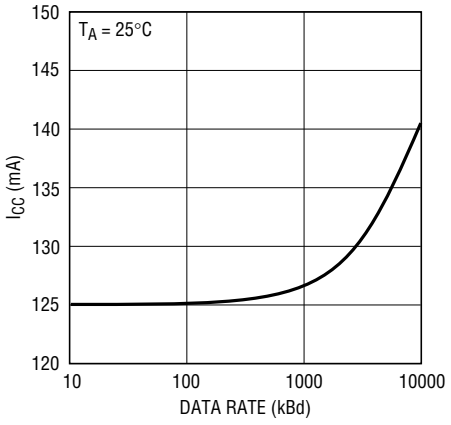
# TYPICAL PERFORMANCE CHARACTERISTICS

### V.11 Mode $I_{CC}$ vs Data Rate



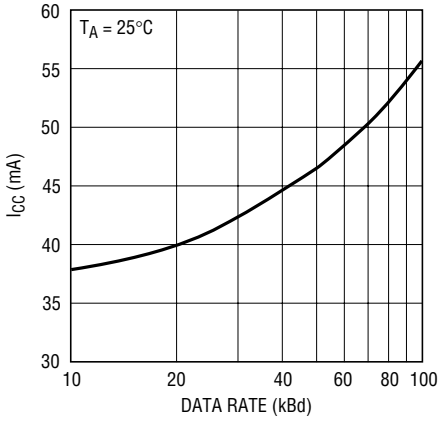

2846 G04

### V.35 Mode $I_{CC}$ vs Data Rate



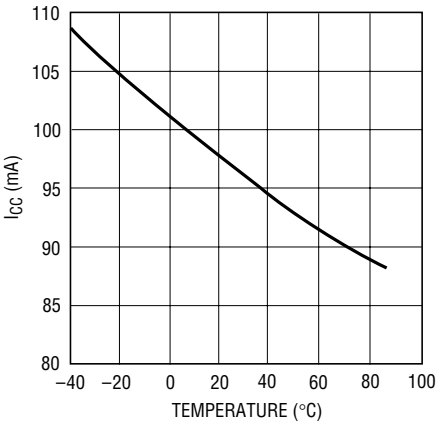

2846 G05

### V.28 Mode $I_{CC}$ vs Data Rate



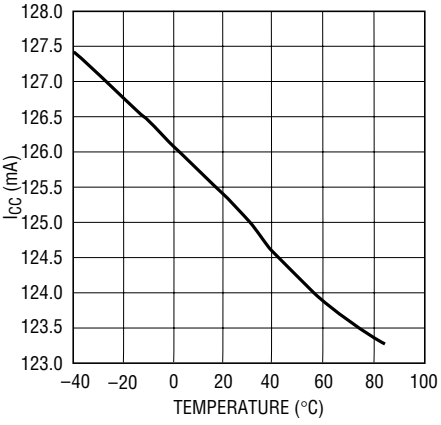

2846 G06

### V.11 Mode $I_{CC}$ vs Temperature



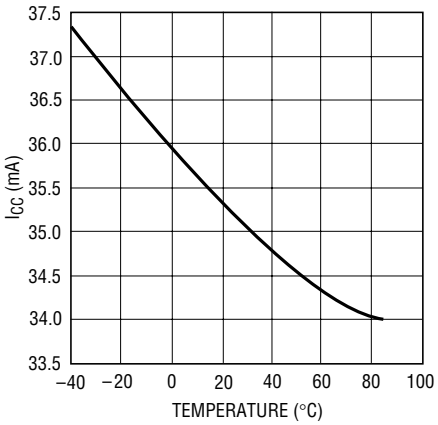

2846 G07

### V.35 Mode $I_{CC}$ vs Temperature



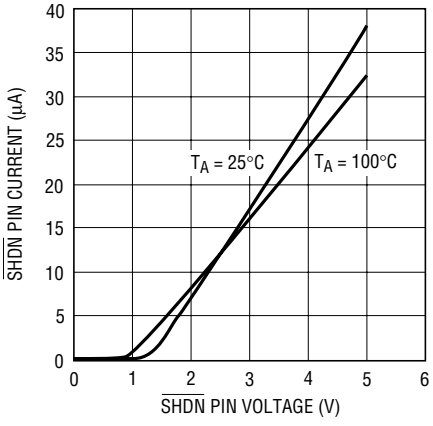

2846 G08

### V.28 Mode $I_{CC}$ vs Temperature



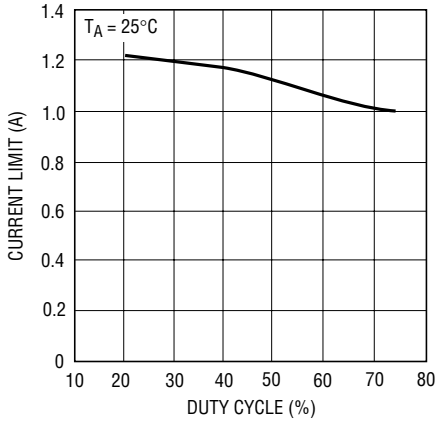

3846 G09

### Boost Switching Regulator $\overline{SHDN}$ Pin Current vs Voltage



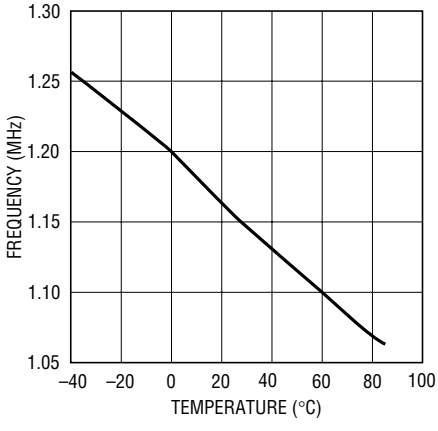

2846 G10

### Boost Switching Regulator Current Limit vs Duty Cycle




2846 G11

### Boost Switching Regulator Oscillator Frequency vs Temperature




2846 G12

## PIN FUNCTIONS

**NC (Pin 1):** No Connect.

**PGND (Pin 2):** Boost Switching Regulator Power Ground. Tie PGND to SGND.

**$V_{IN}$ (Pin 3):** Input Supply Pin. Input supply to boost switching regulator. $3V \leq V_{IN} \leq 3.6V$. Bypass with a 10µF capacitor to ground.

**$\overline{SHDN}$ (Pin 4):** Boost Switching Regulator Shutdown Pin. Tie to 2.4V or more to enable regulator. Ground to shut down.

**$C1^-$ (Pin 5):** Capacitor C1 Negative Terminal. Connect a 1µF capacitor between $C1^+$ and $C1^-$.

**$C1^+$ (Pin 6):** Capacitor C1 Positive Terminal. Connect a 1µF capacitor between $C1^+$ and $C1^-$.

**$V_{DD}$ (Pin 7):** Generated Positive Supply Voltage for V.28. Connect a 1µF capacitor to ground.

**$V_{CC}$ (Pin 8):** Input Supply Pin. Input supply to transceiver. $4.75V \leq V_{CC} \leq 5.25V$. Connect to output of switching regulator.

**D1 (Pin 9):** TTL Level Driver 1 Input.

**D2 (Pin 10):** TTL Level Driver 2 Input.

**D3 (Pin 11):** TTL Level Driver 3 Input.

**R1 (Pin 12):** CMOS Level Receiver 1 Output with Pull-Up to $V_{IN}$ when Three-Stated.

**R2 (Pin 13):** CMOS Level Receiver 2 Output with Pull-Up to $V_{IN}$ when Three-Stated.

**R3 (Pin 14):** CMOS Level Receiver 3 Output with Pull-Up to $V_{IN}$ when Three-Stated.

**M0 (Pin 15):** TTL Level Mode Select Input 0 with Pull-Up to $V_{IN}$. See Table 1.

**M1 (Pin 16):** TTL Level Mode Select Input 1 with Pull-Up to $V_{IN}$. See Table 1.

**$V_{IN}$ (Pin 17):** Input Supply Pin. Input supply to transceiver. $3V \leq V_{IN} \leq 3.6V$. Connect to Pin 3.

**M2 (Pin 18):** TTL Level Mode Select Input 2 with Pull-Up to $V_{IN}$. See Table 1.

**DCE/$\overline{DTE}$ (Pin 19):** TTL Level Mode Select Input with Pull-Up to $V_{IN}$. See Table 1.

**R3 B (Pin 20):** Receiver 3 Noninverting Input.

**R3 A (Pin 21):** Receiver 3 Inverting Input.

**R2 B (Pin 22):** Receiver 2 Noninverting Input.

**R2 A (Pin 23):** Receiver 2 Inverting Input.

**D3/R1 B (Pin 24):** Receiver 1 Noninverting Input and Driver 3 Noninverting Output.

**D3/R1 A (Pin 25):** Receiver 1 Inverting Input and Driver 3 Inverting Output.

**D2 B (Pin 26):** Driver 2 Noninverting Output.

**D2 A (Pin 27):** Driver 2 Inverting Output.

**D1 B (Pin 28):** Driver 1 Noninverting Output.

**D1 A (Pin 29):** Driver 1 Inverting Output.

**GND (Pin 30):** Transceiver Ground.

**$V_{EE}$ (Pin 31):** Generated Negative Supply Voltage. Connect a 3.3µF capacitor to GND.

**$C2^-$ (Pin 32):** Capacitor C2 Negative Terminal. Connect a 1µF capacitor between $C2^+$ and $C2^-$.

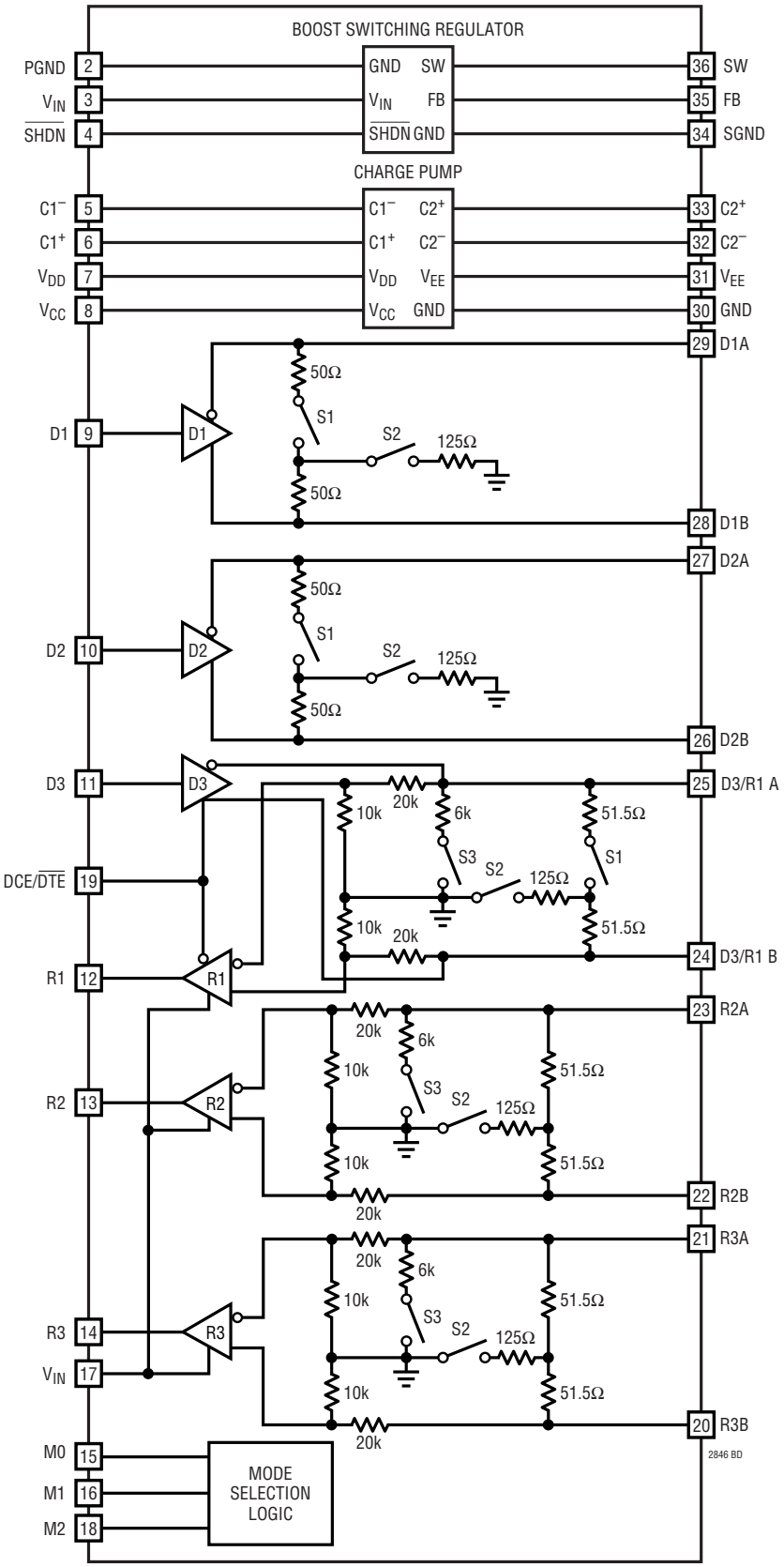
**$C2^+$ (Pin 33):** Capacitor C2 Positive Terminal. Connect a 1µF capacitor between $C2^+$ and $C2^-$.

**SGND (Pin 34):** Boost Switching Regulator Signal Ground. Tie PGND to SGND.

**FB (Pin 35):** Boost Switching Regulator Feedback Pin. Reference voltage is 1.255V. Connect resistive divider tap here. Minimize trace area at FB.

**SW (Pin 36):** Boost Switching Regulator Switch Pin. Connect inductor/diode here. Minimize trace area at this pin to reduce EMI.

## BLOCK DIAGRAM



# TEST CIRCUITS

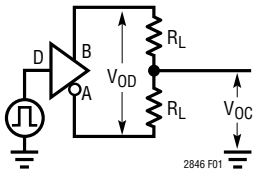



Figure 1. V.11 Driver DC Test Circuit

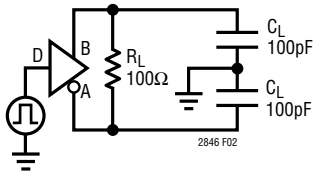



Figure 2. V.11 Driver AC Test Circuit

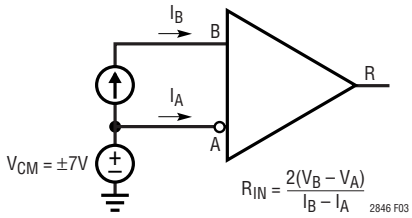



Figure 3. Input Impedance Test Circuit

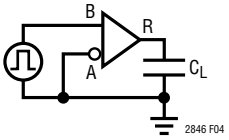



Figure 4. V.11, V.35 Receiver AC Test Circuit

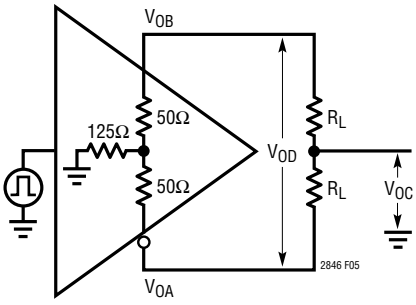



Figure 5. V.35 Driver Open-Circuit Test

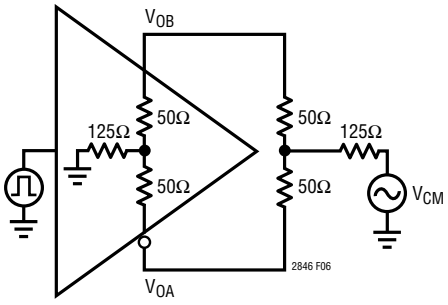



Figure 6. V.35 Driver Test Circuit

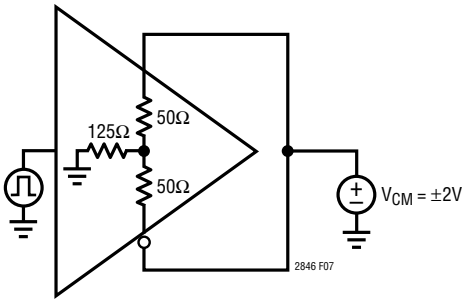



Figure 7. V.35 Driver Common Mode Impedance Test Circuit

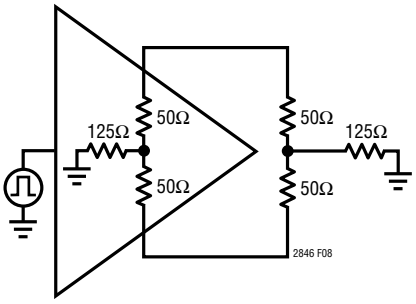



Figure 8. V.35 Driver AC Test Circuit

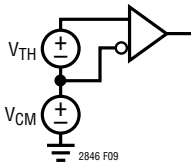



Figure 9. V.35 Receiver DC Test Circuit

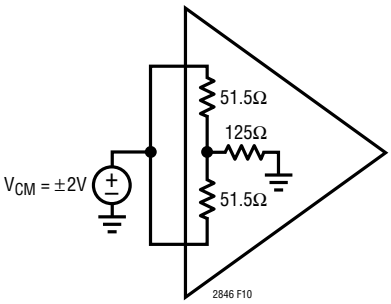



Figure 10. Receiver Common Mode Impedance Test Circuit

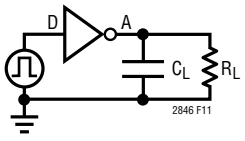



Figure 11. V.28 Driver Test Circuit

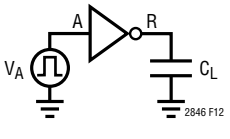



Figure 12. V.28 Receiver Test Circuit

## MODE SELECTION

**Table 1**

| LTC2846 MODE NAME | M2 | M1 | M0 | DCE/$\overline{\text{DTE}}$ | D1 | D2 | D3 | R1 | R2 | R3 |
|---|---|---|---|---|---|---|---|---|---|---|
| Not Used (Default V.11) | 0 | 0 | 0 | 0 | V.11 | V.11 | Z | V.11 | V.11 | V.11 |
| RS530A | 0 | 0 | 1 | 0 | V.11 | V.11 | Z | V.11 | V.11 | V.11 |
| RS530 | 0 | 1 | 0 | 0 | V.11 | V.11 | Z | V.11 | V.11 | V.11 |
| X.21 | 0 | 1 | 1 | 0 | V.11 | V.11 | Z | V.11 | V.11 | V.11 |
| V.35 | 1 | 0 | 0 | 0 | V.35 | V.35 | Z | V.35 | V.35 | V.35 |
| RS449/V.36 | 1 | 0 | 1 | 0 | V.11 | V.11 | Z | V.11 | V.11 | V.11 |
| V.28/RS232 | 1 | 1 | 0 | 0 | V.28 | V.28 | Z | V.28 | V.28 | V.28 |
| No Cable | 1 | 1 | 1 | 0 | Z | Z | Z | Z | Z | Z |
| Not Used (Default V.11) | 0 | 0 | 0 | 1 | V.11 | V.11 | V.11 | Z | V.11 | V.11 |
| RS530A | 0 | 0 | 1 | 1 | V.11 | V.11 | V.11 | Z | V.11 | V.11 |
| RS530 | 0 | 1 | 0 | 1 | V.11 | V.11 | V.11 | Z | V.11 | V.11 |
| X.21 | 0 | 1 | 1 | 1 | V.11 | V.11 | V.11 | Z | V.11 | V.11 |
| V.35 | 1 | 0 | 0 | 1 | V.35 | V.35 | V.35 | Z | V.35 | V.35 |
| RS449/V.36 | 1 | 0 | 1 | 1 | V.11 | V.11 | V.11 | Z | V.11 | V.11 |
| V.28/RS232 | 1 | 1 | 0 | 1 | V.28 | V.28 | V.28 | Z | V.28 | V.28 |
| No Cable | 1 | 1 | 1 | 1 | Z | Z | Z | Z | Z | Z |

## SWITCHING TIME WAVEFORMS

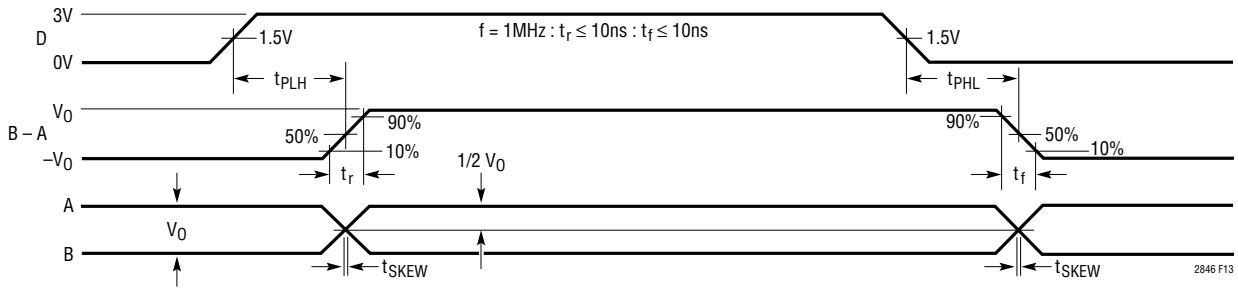



**Figure 13. V.11, V.35 Driver Propagation Delays**

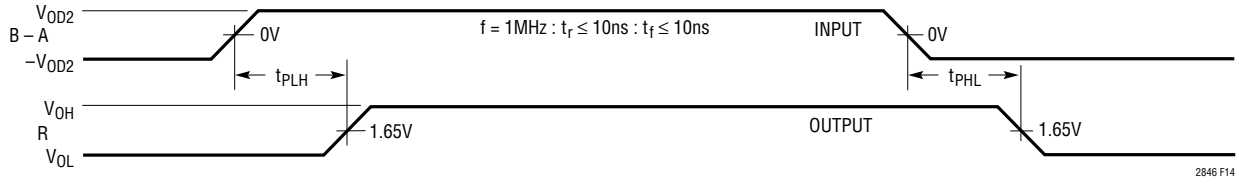



**Figure 14. V.11, V.35 Receiver Propagation Delays**

# SWITCHING TIME WAVEFORMS

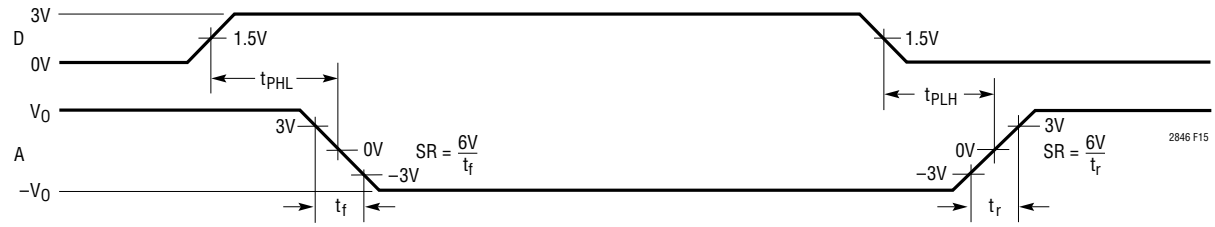



**Figure 15. V.28 Driver Propagation Delays**

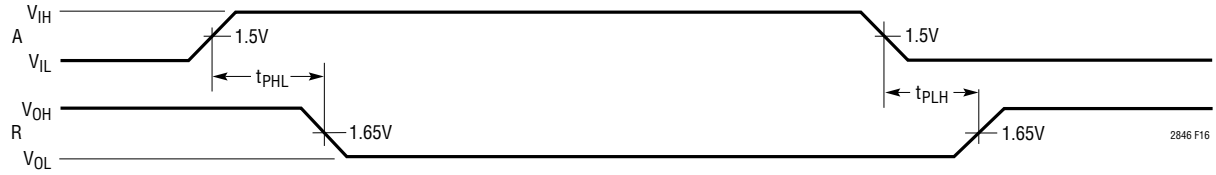



**Figure 16. V.28 Receiver Propagation Delays**

# APPLICATIONS INFORMATION

## Overview

The LTC2846 consists of a boost switching regulator, a charge pump and a 3-driver/3-receiver transceiver. The boost switching regulator generates a 5V $V_{CC}$ from the 3.3V input at $V_{IN}$ to power the charge pump and transceiver. The charge pump generates the $V_{DD}$ and $V_{EE}$ supplies. The LTC2846's $V_{CC}$, $V_{DD}$ and $V_{EE}$ supplies can be used to power a companion chip like the LTC2844 or LTC2845. The receiver outputs are driven between 0V and $V_{IN}$ to interface with 3.3V logic.

The LTC2846 and LTC2844 form a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA530, EIA530-A, V.35, V.36 and X.21 protocols. Cable termination is provided on-chip, eliminating the need for discrete termination designs.

A complete DCE-to-DTE interface operating in EIA530 mode is shown in Figure 17. The LTC2846 half of each port is used to generate and appropriately terminate the clock and data signals. The LTC2844 is used to generate the control signals along with LL (Local Loopback).

## Mode Selection

The interface protocol is selected using the mode select pins M0, M1 and M2 (see Table 1).

For example, if the port is configured as a V.35 interface, the mode selection pins should be M2 = 1, M1 = 0, M0 = 0. For the control signals, the drivers and receivers will operate in V.28 (RS232) electrical mode. For the clock and data signals, the drivers and receivers will operate in V.35 electrical mode. The DCE/$\overline{\text{DTE}}$ pin will configure the port for DCE mode when high, and DTE when low.

The interface protocol may be selected simply by plugging the appropriate interface cable into the connector. The mode pins are routed to the connector and are left unconnected (1) or wired to ground (0) in the cable as shown in Figure 18. The internal pull-up current sources will ensure a binary 1 when a pin is left unconnected.

The mode selection may also be accomplished by using jumpers to connect the mode pins to ground or $V_{IN}$.

## APPLICATIONS INFORMATION

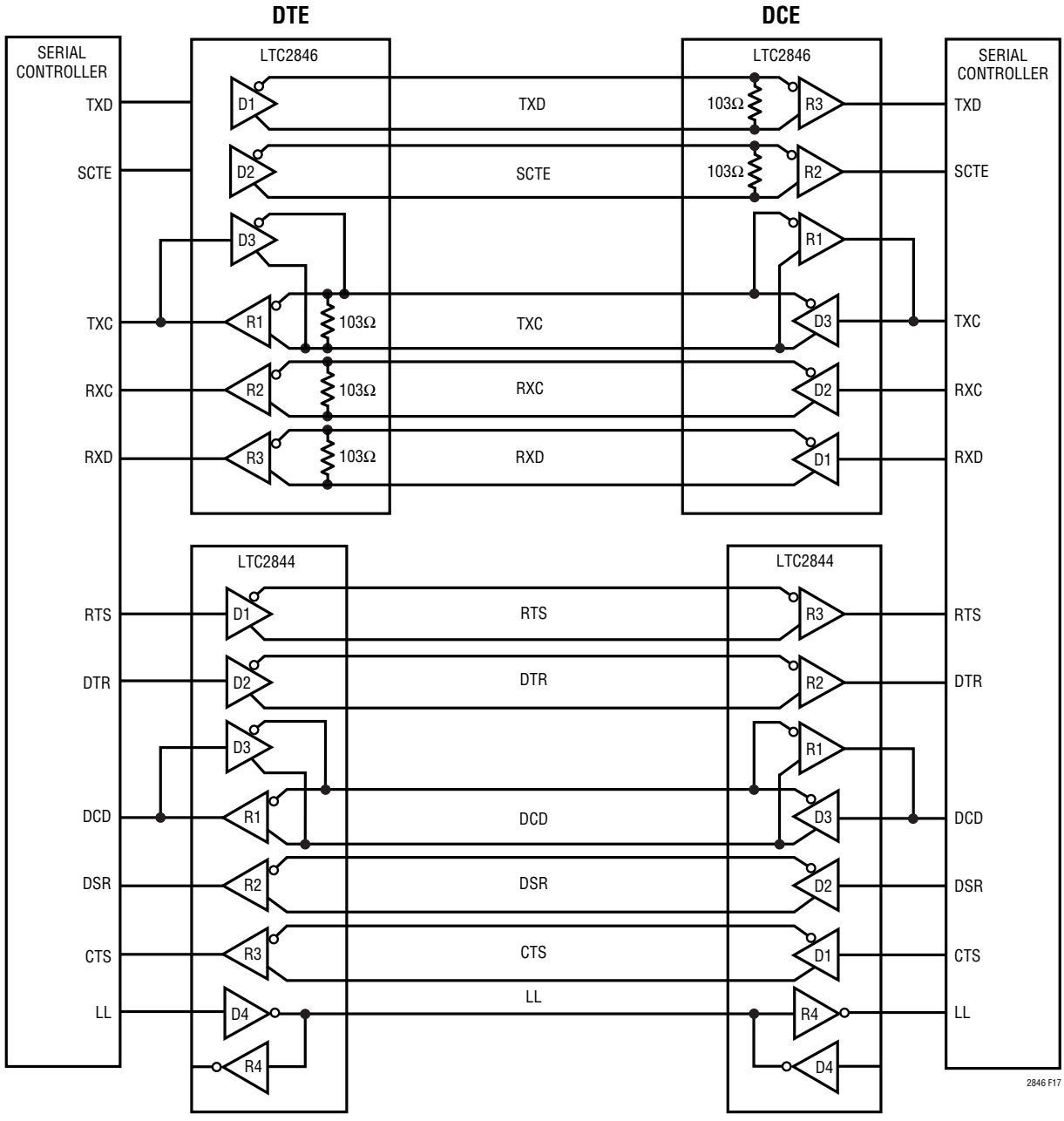



**Figure 17. Complete Multiprotocol Interface in EIA530 Mode**

When the cable is removed, leaving all mode pins unconnected, the LTC2846/LTC2844 will enter no-cable mode. In this mode the LTC2846/LTC2844 supply current drops to less than 900μA and the LTC2846/LTC2844 driver outputs are forced into a high impedance state. At the same time, the R2 and R3 receivers of the LTC2846 are differentially terminated with 103Ω and the other receivers on the LTC2846 and LTC2844 are terminated with 30kΩ to ground.

### Cable Termination

Traditional implementations used expensive relays to switch resistors or required the user to change termination modules every time a new interface standard was

# APPLICATIONS INFORMATION

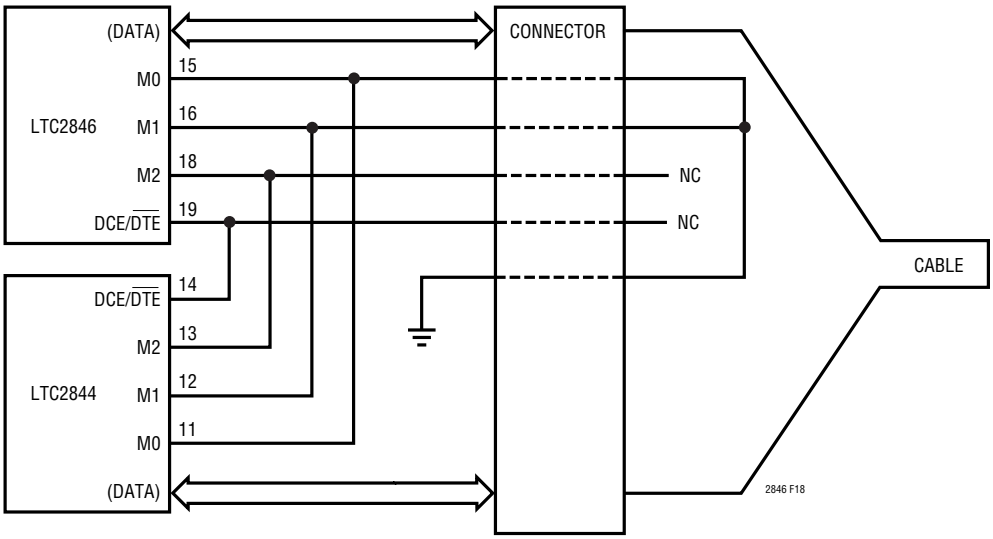



**Figure 18: Single Port DCE V.35 Mode Selection in the Cable**

selected. Switching the terminations with FETs is difficult because the FETs must remain off when the signal voltage is beyond the supply voltage. Alternatively, custom cables may contain termination in the cable head or route signals to various terminations on the board.

The LTC2846/LTC2844 chip set solves the cable termination switching problem by automatically providing the appropriate termination and switching on-chip for the V.10 (RS423), V.11 (RS422), V.28 (RS232) and V.35 electrical protocols.

### V.10 (RS423) Interface

All V.10 drivers and receivers necessary for the RS449, EIA530, EIA530-A, V.36 and X.21 protocols are implemented on the LTC2844.

A typical V.10 unbalanced interface is shown in Figure 19. A V.10 single-ended generator with output A and ground C is connected to a differential receiver with input A' connected to A, and ground C' connected via the signal return to ground C. Usually, no cable termination is required for V.10 interfaces, but the receiver inputs must be compliant with the impedance curve shown in Figure 20.

The V.10 receiver configuration in the LTC2844 is shown in Figure 21. In V.10 mode, switch S3 inside the LTC2844 is turned off. The noninverting input is disconnected

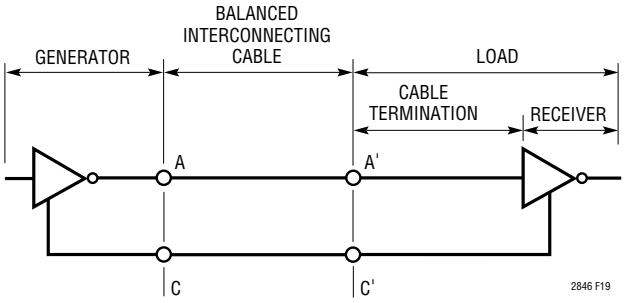



**Figure 19. Typical V.10 Interface**

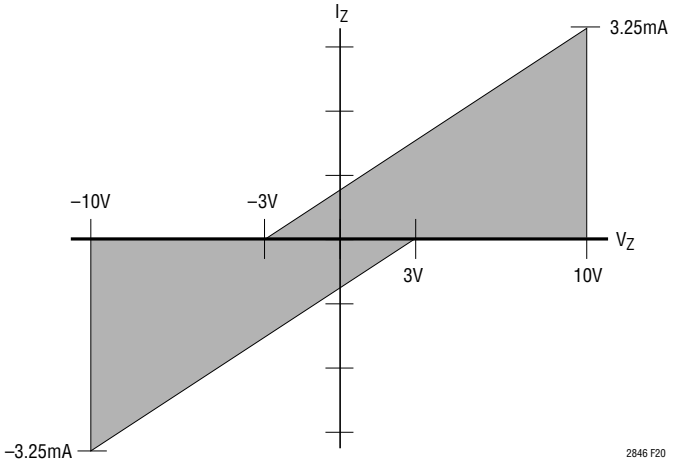



**Figure 20. V.10 Receiver Input Impedance**

## APPLICATIONS INFORMATION

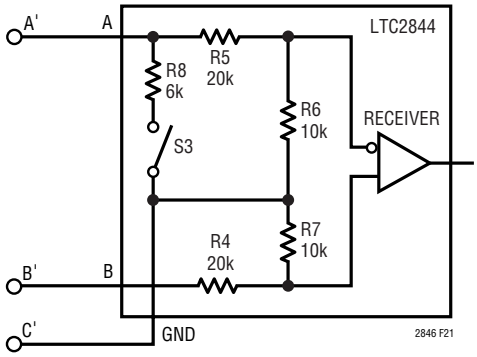



**Figure 21. V.10 Receiver Configuration**

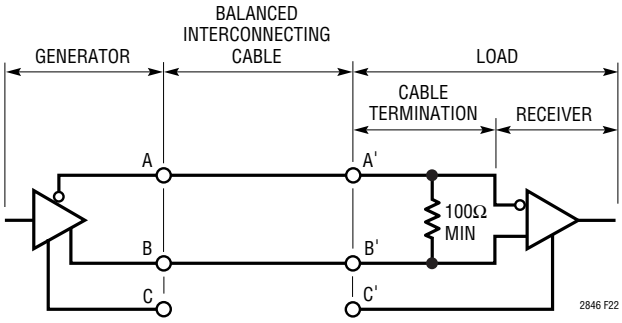



**Figure 22. Typical V.11 Interface**

inside the LTC2844 receiver and connected to ground. The cable termination is then the 30k input impedance to ground of the LTC2844 V.10 receiver.

### V.11 (RS422) Interface

A typical V.11 balanced interface is shown in Figure 22. A V.11 differential generator with outputs A and B and ground C is connected to a differential receiver with input A' connected to A, input B' connected to B, and ground C' connected via the signal return to ground C. The V.11 interface has a differential termination at the receiver end that has a minimum value of 100Ω. The termination resistor is optional in the V.11 specification, but for the high speed clock and data lines, the termination is essential to prevent reflections from corrupting the data. The receiver inputs must also be compliant with the impedance curve shown in Figure 20.

In V.11 mode, all switches are off except S1 of the LTC2846's receivers which connects a 103Ω differential

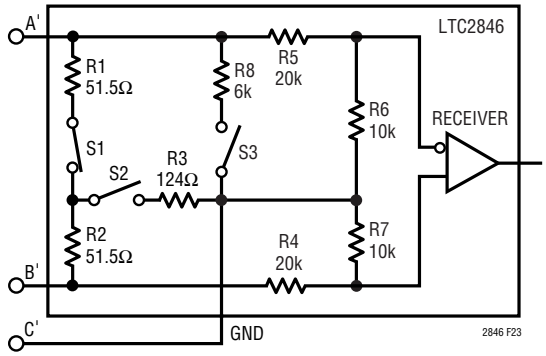



**Figure 23. V.11 Receiver Configuration**

termination impedance to the cable as shown in Figure 23[1]. The LTC2844 only handles control signals, so no termination other than its V.11 receivers' 30k input impedance is necessary.

### V.28 (RS232) Interface

A typical V.28 unbalanced interface is shown in Figure 24. A V.28 single-ended generator with output A and ground C is connected to a single-ended receiver with input A' connected to A and ground C' connected via the signal return to ground C.

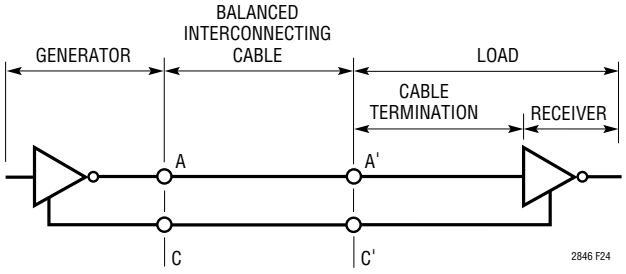



**Figure 24. Typical V.28 Interface**

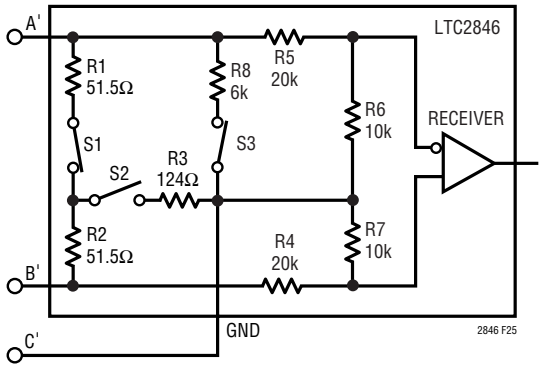



**Figure 25. V.28 Receiver Configuration**

[1]Actually, there is no switch S1 in receivers R2 and R3. However, for simplicity, all termination networks on the LTC2846 can be treated identically if it is assumed that an S1 switch exists and is always closed on the R2 and R3 receivers.

# APPLICATIONS INFORMATION

In V.28 mode, S3 is closed inside the LTC2846/LTC2844 which connects a 6k (R8) impedance to ground in parallel with 20k (R5) plus 10k (R6) for a combined impedance of 5k as shown in Figure 25. Proper termination is only provided when the B input of the receivers is floating, since S1 of the LTC2846's R2 and R3 receivers remains on in V.28 mode[1]. The noninverting input is disconnected inside the LTC2846/LTC2844 receiver and connected to a TTL level reference voltage to give a 1.4V receiver trip point.

### V.35 Interface

A typical V.35 balanced interface is shown in Figure 26. A V.35 differential generator with outputs A and B and ground C is connected to a differential receiver with input A' connected to A, input B' connected to B, and ground C' connected via the signal return to ground C. The V.35 interface requires a T or delta network termination at the receiver end and the generator end. The receiver differential impedance measured at the connector must be 100Ω ±10Ω, and the impedance between shorted terminals (A' and B') and ground (C') must be 150Ω ±15Ω.

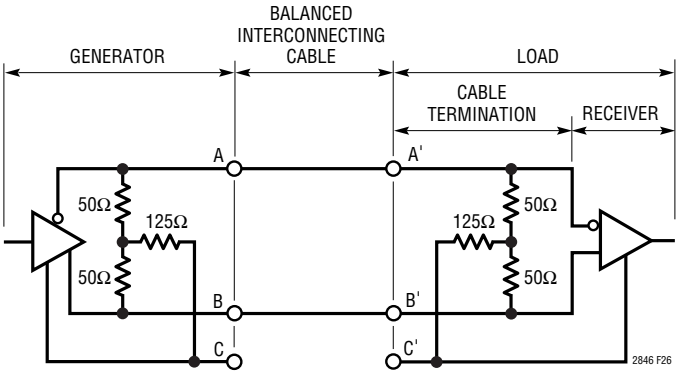



**Figure 26. Typical V.35 Interface**

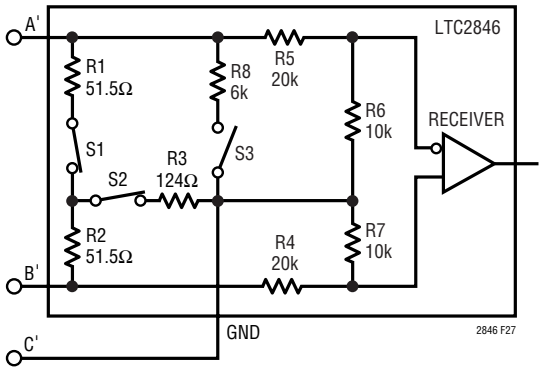



**Figure 27. V.35 Receiver Configuration**

In V.35 mode, both switches S1 and S2 inside the LTC2846 are on, connecting a T network impedance as shown in Figure 27. The 30k input impedance of the receiver is placed in parallel with the T network termination, but does not affect the overall input impedance significantly.

The generator differential impedance must be 50Ω to 150Ω and the impedance between shorted terminals (A and B) and ground (C) must be 150Ω ±15Ω.

### No-Cable Mode

The no-cable mode (M0 = M1 = M2 = 1) is intended for the case when the cable is disconnected from the connector. The charge pump, bias circuitry, drivers and receivers are turned off, the driver outputs are forced into a high impedance state, and the $V_{CC}$ supply current to the transceiver drops to less than 900μA while its $V_{IN}$ supply current drops to less than 10μA. Note that the LTC2846's R2 and R3 receivers continue to be terminated by a 103Ω differential impedance.

### Charge Pump

The LTC2846 uses an internal capacitive charge pump to generate $V_{DD}$ and $V_{EE}$ as shown in Figure 28. A voltage doubler generates about 8V on $V_{DD}$ and a voltage inverter generates about –7.5V on $V_{EE}$. Three 1μF surface mounted tantalum or ceramic capacitors are required for C1, C2 and C3. The $V_{EE}$ capacitor C4 should be a minimum of 3.3μF. All capacitors are 16V and should be placed as close as possible to the LTC2846 to reduce EMI.

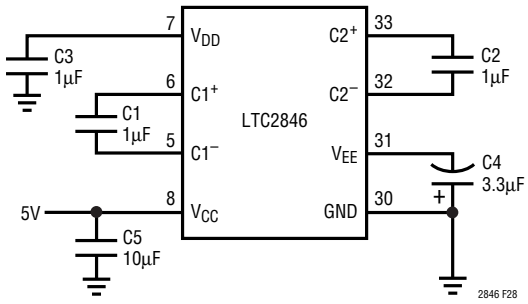



**Figure 28. Charge Pump**

## APPLICATIONS INFORMATION

### Switching Regulator

The circuit as shown in Figure 29 can provide up to 480mA at 5V to drive the LTC2846's transceiver as well as its companion chip in the DTE-DCE interface. In its shut down mode with the $\overline{SHDN}$ pin at 0V, the boost switching regulator draws less than 10µA.

Ferrite core inductors should be used to obtain the best efficiency, as core losses at 1.2MHz are much lower for ferrite cores than for cheaper powdered-iron types. Choose an inductor that can handle at least 1A without saturating, and ensure that the inductor has a low DCR (copper wire resistance) to minimize $I^2R$ power losses.

Use low ESR capacitors for the output to minimize output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they have extremely low ESR and are available in very small packages. Ceramic capacitors also make a good choice for the input decoupling capacitor, and should be placed as close as possible to the switching regulator. Solid tantalum or OS-CON capacitors can be used but they will occupy more board area than a ceramic and will have a higher ESR.

A Schottky diode is recommended for use with the switching regulator. The ON Semiconductor MBR0520 is a very good choice.

To set the output voltage, select the values of R1 and R2 according to the following equation.

$$R1 = R2[(5V/1.255V) - 1]$$

A good value for R2 is 4.3k which sets the current in the resistor divider chain to 1.255V/4.3k = 292µA.

The switching regulator has a switch current limit of 1A. This current limit protects the switch as well as the external components connected to the switching regulator.

The high speed operation of the boost switching regulator demands careful attention to board layout. Figure 30 shows the recommended component placement.

### Receiver Fail-Safe

All LTC2846/LTC2844 receivers feature fail-safe operation in all modes. If the receiver inputs are left floating or are shorted together by a termination resistor, the receiver output will always be forced to a logic high.

### DTE vs DCE Operation

The DCE/$\overline{DTE}$ pin acts as an enable for Driver 3/Receiver 1 in the LTC2846, and Driver 3/Receiver 1 and Receiver 4/Driver 4 in the LTC2844.

The LTC2846/LTC2844 can be configured for either DTE or DCE operation in one of two ways: a dedicated DTE or DCE port with a connector of appropriate gender or a port with one connector that can be configured for DTE or DCE operation by rerouting the signals to the LTC2846/LTC2844 using a dedicated DTE cable or dedicated DCE cable.

A dedicated DTE port using a DB-25 male connector is shown in Figure 31. The interface mode is selected by logic outputs from the controller or from jumpers to either $V_{IN}$ or GND on the mode select pins. A dedicated DCE port using a DB-25 female connector is shown in Figure 32.

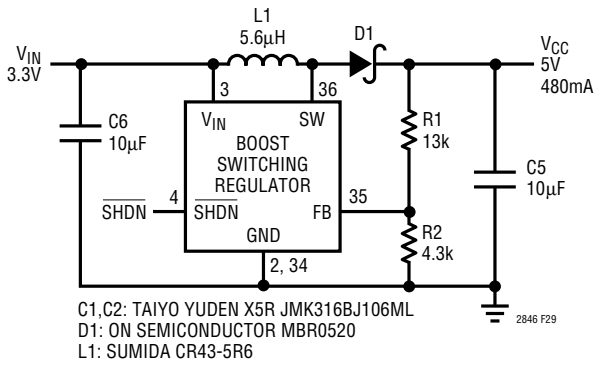



Figure 29. Boost Switching Regulator

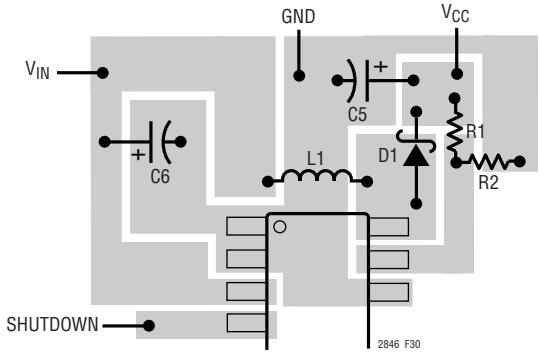



Figure 30. Suggested Layout

# TYPICAL APPLICATIONS

A port with one DB-25 connector, that can be configured for either DTE or DCE operation is shown in Figure 33. The configuration requires separate cables for proper signal routing in DTE or DCE operation. For example, in DTE mode, the TXD signal is routed to Pins 2 and 14 via the LTC2846's Driver 1. In DCE mode, Driver 1 now routes the RXD signal to Pins 2 and 14.

### Multiprotocol Interface with RL, LL, TM and a DB-25 Connector

If the RL, LL and TM signals are implemented, there are not enough drivers and receivers available in the LTC2846/LTC2844. In Figure 34, the required control signals are handled by the LTC2845. The LTC2845 has an additional single-ended driver/receiver pair that can handle two more optional control signals such as TM and RL.

### Cable-Selectable Multiprotocol Interface

A cable-selectable multiprotocol DTE/DCE interface is shown in Figure 35. The select lines M0, M1 and DCE/$\overline{\text{DTE}}$ are brought out to the connector. The mode is selected by the cable by wiring M0 (connector Pin 18) and M1 (connector Pin 21) and DCE/$\overline{\text{DTE}}$ (connector Pin 25) to ground (connector Pin 7) or letting them float. If M0, M1 or DCE/$\overline{\text{DTE}}$ is floating, internal pull-up current sources will pull the signals to $V_{IN}$. The select bit M2 is floating, and therefore, internally pulled high. When the cable is pulled out, the interface will go into the no-cable mode.

## TYPICAL APPLICATIONS

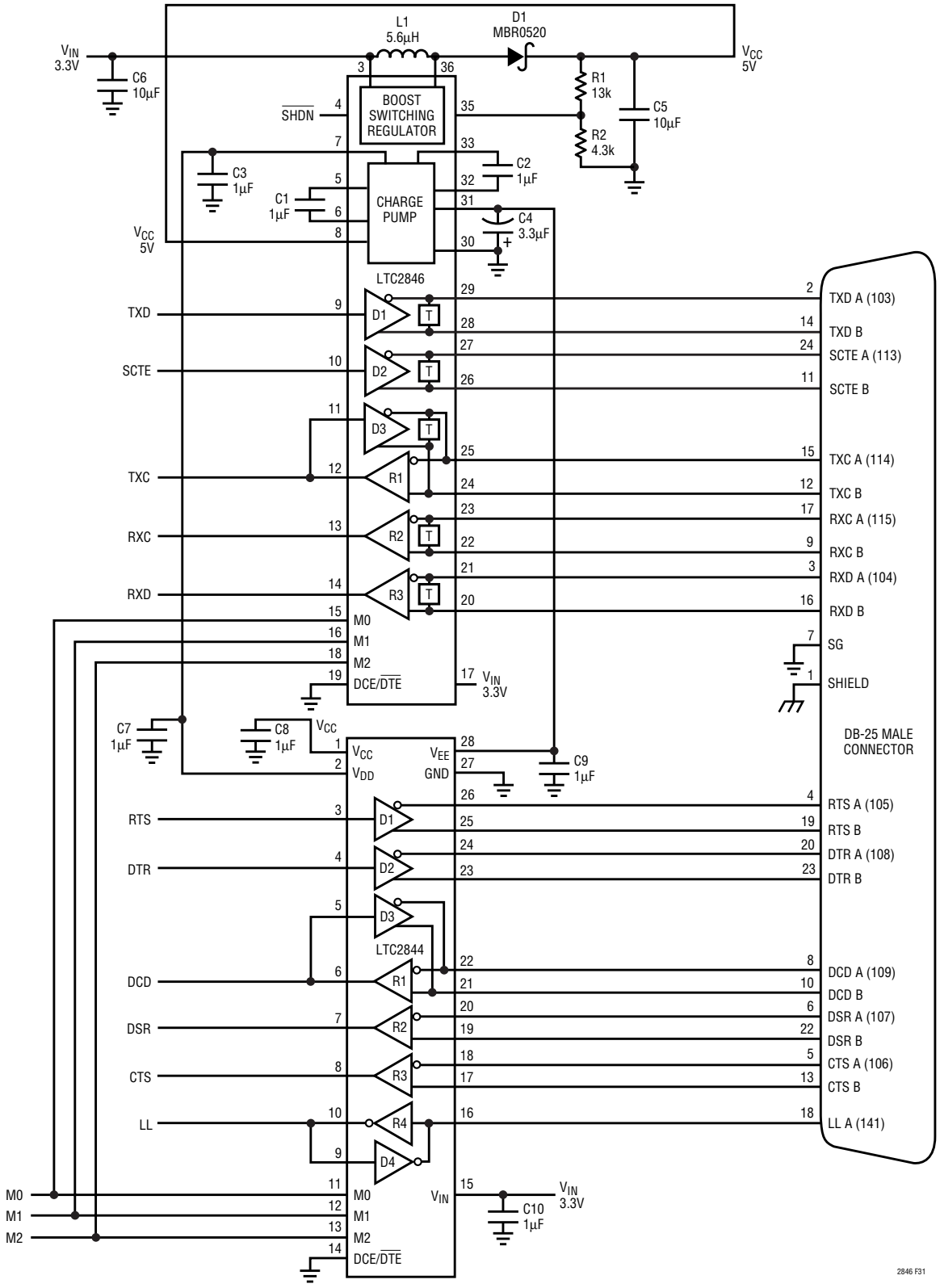



**Figure 31. Controller-Selectable Multiprotocol DTE Port with DB-25 Connector**

# TYPICAL APPLICATIONS

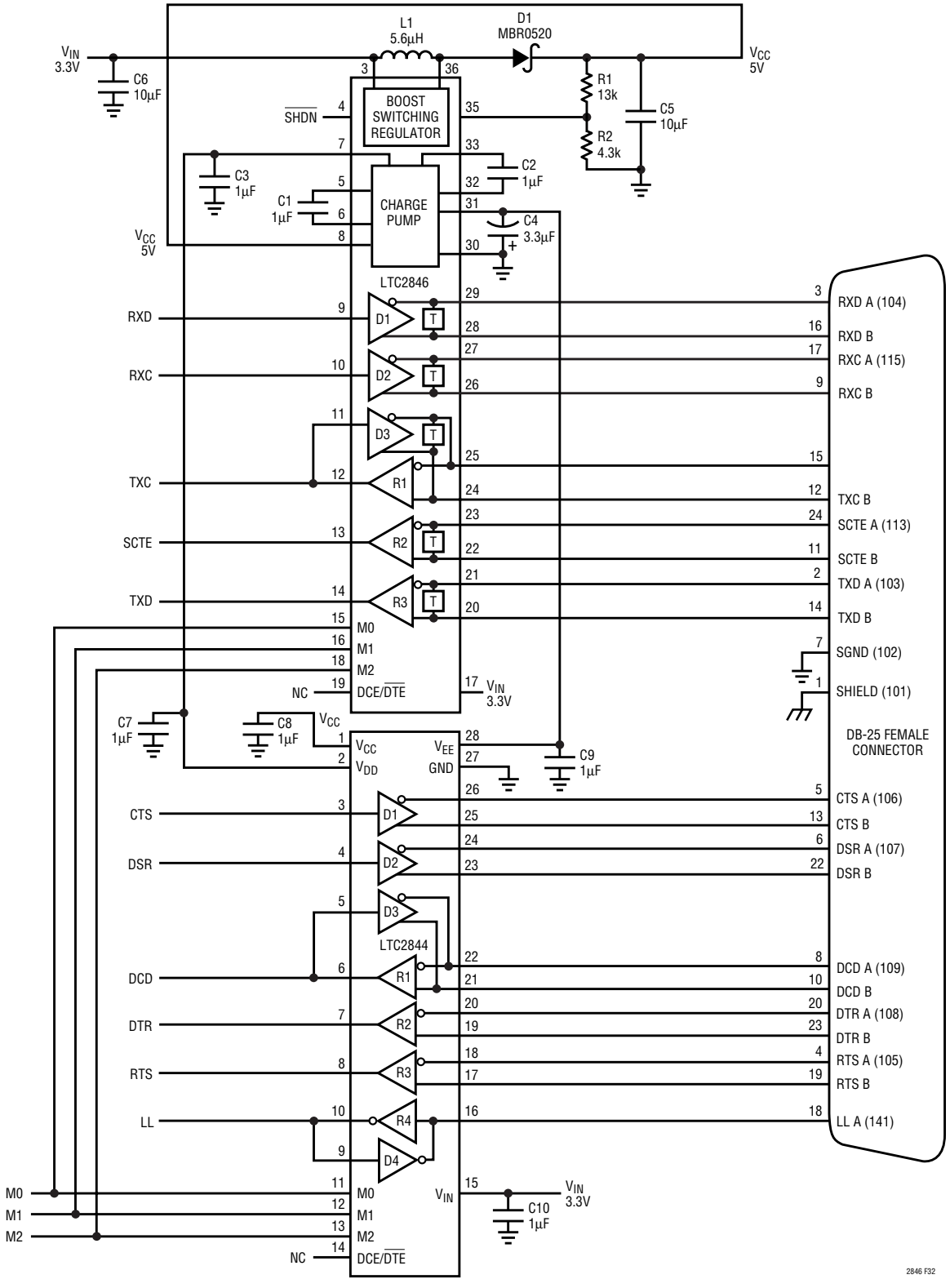



**Figure 32. Controller-Selectable DCE Port with DB-25 Connector**

## TYPICAL APPLICATIONS

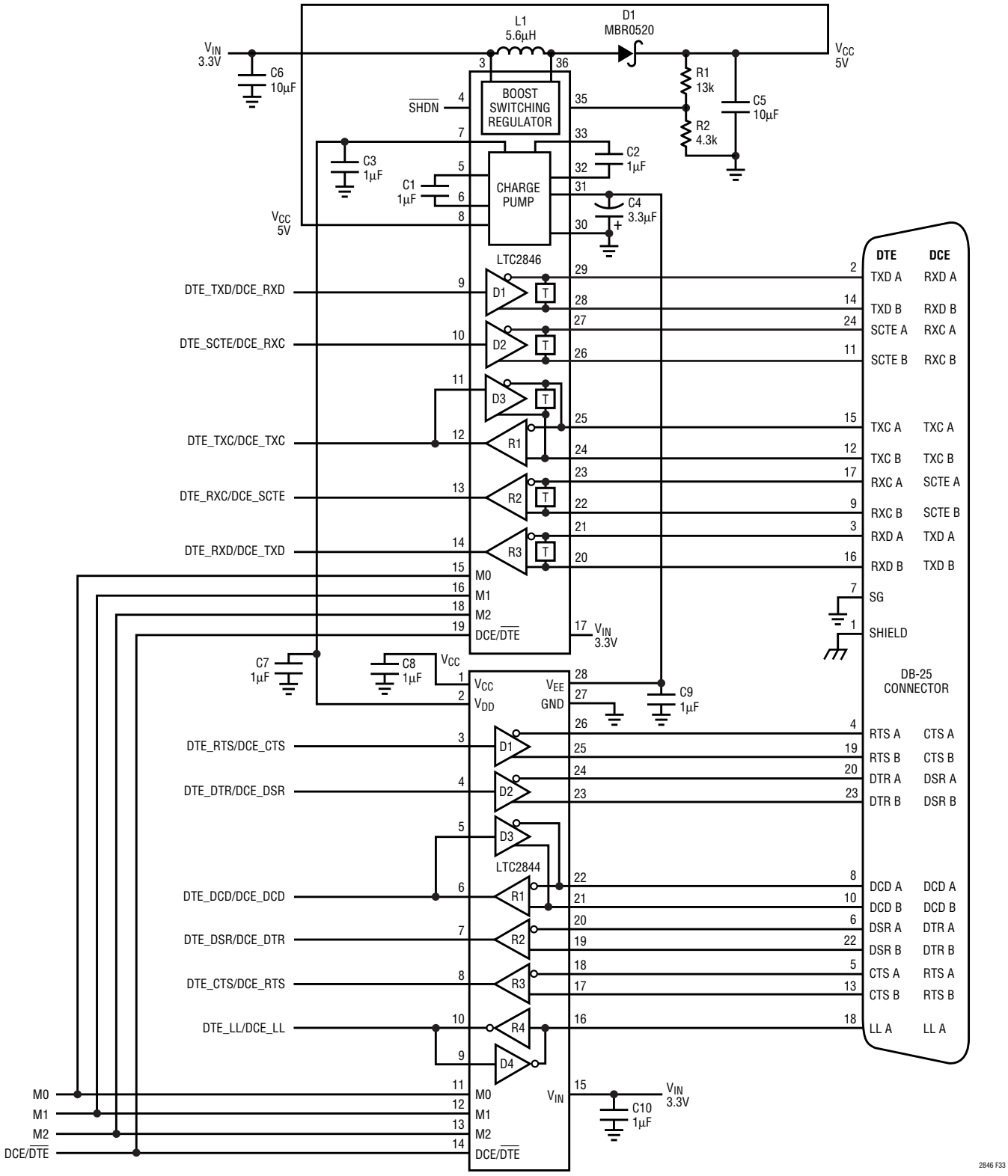



**Figure 33. Controller-Selectable Multiprotocol DTE/DCE Port with DB-25 Connector**

# TYPICAL APPLICATIONS

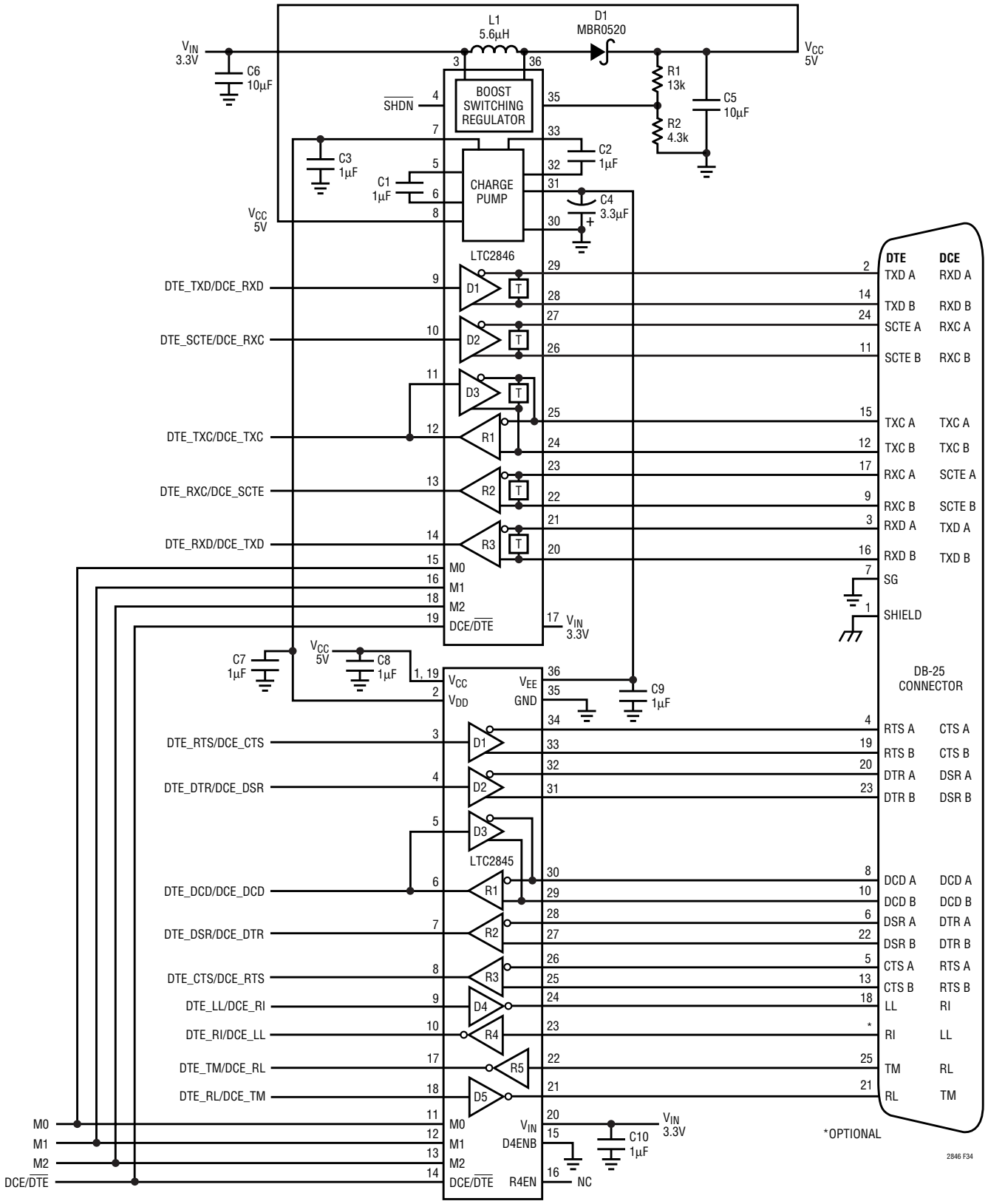
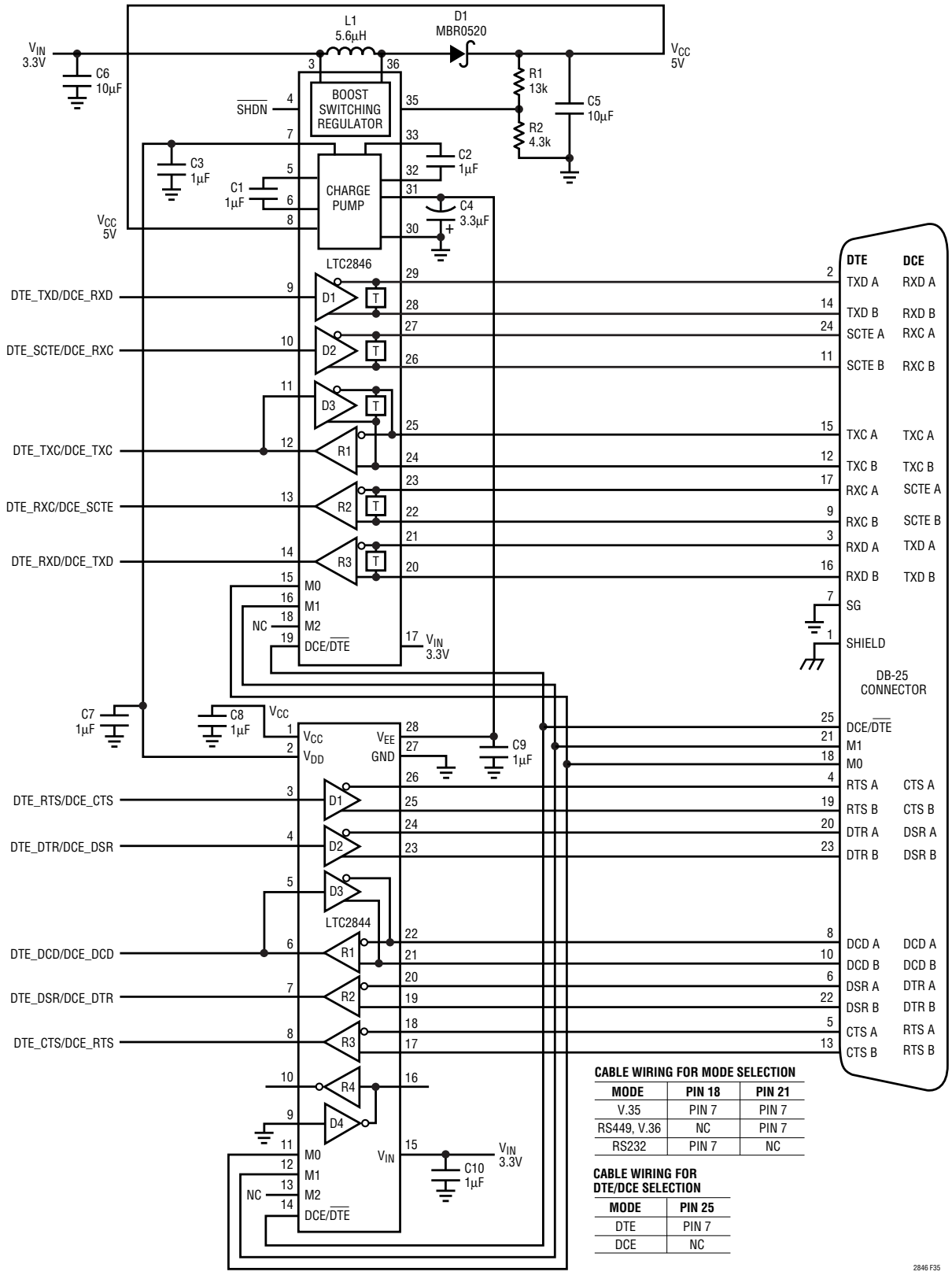



**Figure 34. Controller-Selectable Multiprotocol DTE/DCE Port with RL, LL, TM and DB-25 Connector**

## TYPICAL APPLICATIONS




**CABLE WIRING FOR MODE SELECTION**

| MODE | PIN 18 | PIN 21 |
|---|---|---|
| V.35 | PIN 7 | PIN 7 |
| RS449, V.36 | NC | PIN 7 |
| RS232 | PIN 7 | NC |

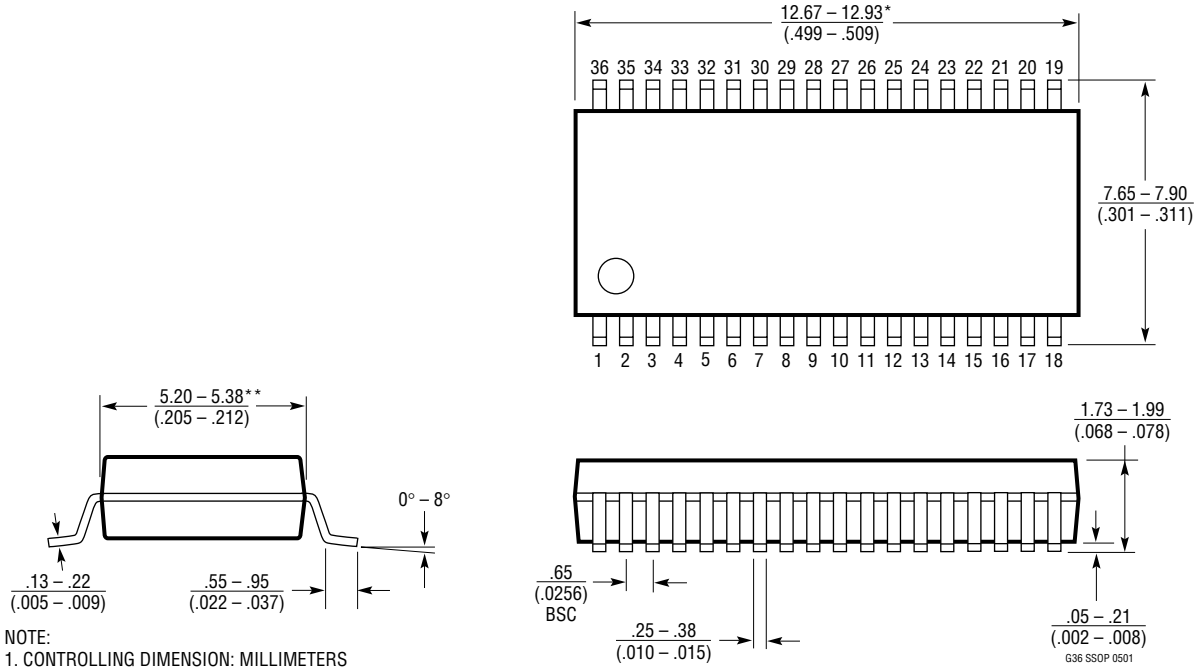
**CABLE WIRING FOR DTE/DCE SELECTION**

| MODE | PIN 25 |
|---|---|
| DTE | PIN 7 |
| DCE | NC |

**Figure 35. Cable-Selectable Multiprotocol DTE/DCE Port with DB-25 Connector**

# PACKAGE DESCRIPTION

**G Package**
**36-Lead Plastic SSOP (0.209)**
(LTC DWG # 05-08-1640)




NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1321 | Dual RS232/RS485 Transceiver | Two RS232 Driver/Receiver Pairs or Two RS485 Driver/Receiver Pairs |
| LTC1334 | Single 5V RS232/RS485 Multiprotocol Transceiver | Two RS232 Driver/Receiver or Four RS232 Driver/Receiver Pairs |
| LTC1343 | Software-Selectable Multiprotocol Transceiver | 4-Driver/4-Receiver for Data and Clock Signals |
| LTC1344A | Software-Selectable Cable Terminator | Perfect for Terminating the LTC1543 (Not Needed with LTC1546) |
| LTC1345 | Single Supply V.35 Transceiver | 3-Driver/3-Receiver for Data and Clock Signals |
| LTC1346A | Dual Supply V.35 Transceiver | 3-Driver/3-Receiver for Data and Clock Signals |
| LTC1543 | Software-Selectable Multiprotocol Transceiver | Terminated with LTC1344A for Data and Clock Signals, Companion to LTC1544 or LTC1545 for Control Signals |
| LTC1544 | Software-Selectable Multiprotocol Transceiver | Companion to LTC1546 or LTC1543 for Control Signals Including LL |
| LTC1545 | Software-Selectable Multiprotocol Transceiver | 5-Driver/5-Receiver Companion to LTC1546 or LTC1543 for Control Signals Including LL, TM and RL |
| LTC1546 | Software-Selectable Multiprotocol Transceiver | 3-Driver/3-Receiver with Termination for Data and Clock Signals |
| LTC2844 | 3.3V Software-Selectable Multiprotocol Transceiver | Companion to LTC2846 for Control Signals Including LL |
| LTC2845 | 3.3V Software-Selectable Multiprotocol Transceiver | 5-Driver/5-Receiver Companion to LTC2846 for Control Signals Including LL, TM and R |



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