INITIAL RELEASE

Final Electrical Specifications

LTC2845

# 3.3V Software-Selectable Multiprotocol Transceiver

April 2002

## FEATURES

- **Software-Selectable Transceiver Supports: RS232, RS449, EIA530, EIA530-A, V.35, V.36, X.21**
- **Operates from Single 3.3V Supply with LTC2846**
- Complete DTE or DCE Port with LTC2846

## APPLICATIONS

- Data Networking
- CSU and DSU
- Data Routers

## DESCRIPTION

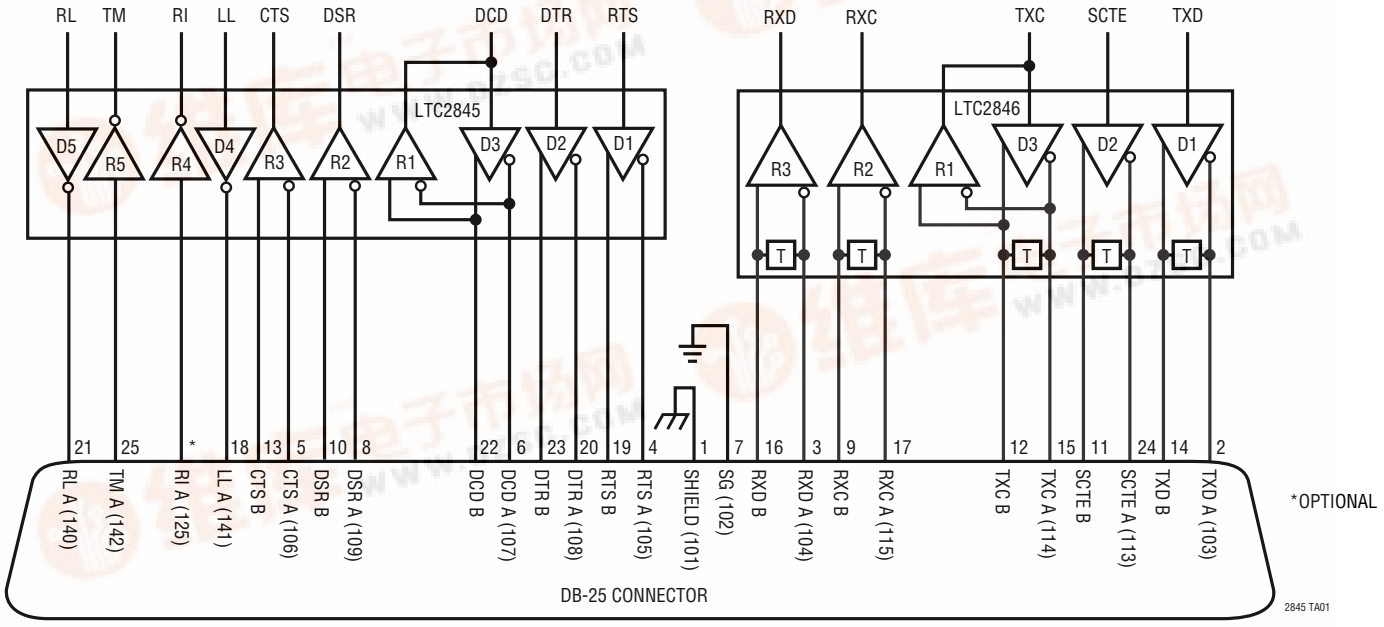
The LTC®2845 is a 5-driver/5-receiver multiprotocol transceiver. The LTC2845 and LTC2846 form the core of a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA530, EIA530-A, V.35, V.36 or X.21 protocols.

The LTC2845 operates from a 3.3V supply and supplies provided by the LTC2846. This part is available in a 36-lead SSOP surface mount package.



## TYPICAL APPLICATION

**DTE or DCE Multiprotocol Serial Interface with DB-25 Connector**



## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Supply Voltage
- $V_{CC}$ ..... –0.3V to 6.5V
- $V_{IN}$ ..... –0.3V to 6.5V
- $V_{EE}$ ..... –10V to 0.3V
- $V_{DD}$ ..... –0.3V to 10V

Input Voltage
- Transmitters ..... –0.3V to ($V_{CC}$ + 0.3V)
- Receivers ..... –18V to 18V
- Logic Pins ..... –0.3V to ($V_{CC}$ + 0.3V)

Output Voltage
- Transmitters ..... ($V_{EE}$ – 0.3V) to ($V_{DD}$ + 0.3V)
- Receivers ..... –0.3V to ($V_{IN}$ + 0.3V)

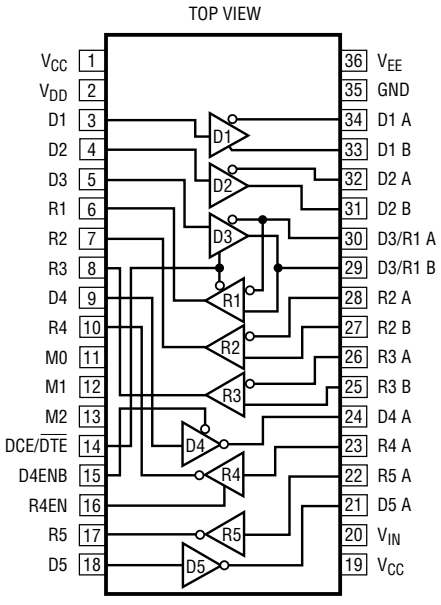
Short-Circuit Duration
- Transmitter Output ..... Indefinite
- Receiver Output ..... Indefinite
- $V_{EE}$ ..... 30 sec

Operating Temperature Range
- LTC2845CG ..... 0°C to 70°C
- LTC2845IG ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION




G PACKAGE
36-LEAD PLASTIC SSOP

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 90°C/W, $\theta_{JC}$ = 35°C/W

| ORDER PART NUMBER |
|---|
| LTC2845CG<br>LTC2845IG |

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 5V, $V_{IN}$ = 3.3V, $V_{DD}$ = 8V, $V_{EE}$ = – 7V for V.28, – 5.5V for V.10, V.11 (Notes 2, 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Supplies** | | | | | | | |
| $I_{CC}$ | $V_{CC}$ Supply Current (DCE Mode, All Digital Pins = GND or $V_{IN}$) | RS530, RS530-A, X.21 Modes, No Load | | | 2.7 | | mA |
| | | RS530, RS530-A, X.21 Modes, Full Load | ● | | 110 | 150 | mA |
| | | V.28 Mode, No Load | ● | | 1 | 3 | mA |
| | | V.28 Mode, Full Load | ● | | 1 | 3 | mA |
| | | No-Cable Mode | ● | | 700 | 1400 | µA |
| $I_{EE}$ | $V_{EE}$ Supply Current (DCE Mode, All Digital Pins = GND or $V_{IN}$) | RS530, RS530-A, X.21 Modes, No Load | | | 2 | | mA |
| | | RS530, X.21 Modes, Full Load | | | 23 | | mA |
| | | RS530-A, Full Load | | | 34 | | mA |
| | | V.28 Mode, No Load | | | 1 | | mA |
| | | V.28 Mode, Full Load | | | 12 | | mA |
| | | No-Cable Mode | | | 10 | | µA |
| $I_{DD}$ | $V_{DD}$ Supply Current (DCE Mode, All Digital Pins = GND or $V_{IN}$) | RS530, RS530-A, X.21 Modes, No Load | | | 0.3 | | mA |
| | | RS530, RS530-A, X.21 Modes, Full Load | | | 0.3 | | mA |
| | | V.28 Mode, No Load | | | 1 | | mA |
| | | V.28 Mode, Full Load | | | 13.5 | | mA |
| | | No-Cable Mode | | | 10 | | µA |
| $I_{VIN}$ | $V_{IN}$ Supply Current (DCE Mode, All Digital Pins = GND or $V_{IN}$) | All Modes Except No-Cable Mode | | | 650 | | µA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 5V, $V_{IN}$ = 3.3V, $V_{DD}$ = 8V, $V_{EE}$ = – 7V for V.28, – 5.5V for V.10, V.11 (Notes 2, 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $P_D$ | Internal Power Dissipation (DCE Mode, All Digital Pins = GND or $V_{IN}$) | RS530, RS530-A, X.21 Modes, Full Load<br>V.28 Mode, Full Load | | | 340<br>64 | | mW<br>mW |
| **Logic Inputs and Outputs** | | | | | | | |
| $V_{IH}$ | Logic Input High Voltage | | ● | 2 | | | V |
| $V_{IL}$ | Logic Input Low Voltage | $V_{CC}$ = 5V<br>R4EN when $V_{CC}$ = 3.3V | ●<br>● | | | 0.8<br>0.5 | V<br>V |
| $I_{IN}$ | Logic Input Current | D1, D2, D3, D4, D5<br>M0, M1, M2, DCE, D4ENB, R4EN = GND<br>M0, M1, M2, DCE, D4ENB, R4EN = $V_{IN}$ | ●<br>●<br>● | <br>–30<br> | <br>–75<br> | ±10<br>–120<br>±10 | µA<br>µA<br>µA |
| $V_{OH}$ | Output High Voltage | $I_O$ = –3mA | ● | 2.7 | 3 | | V |
| $V_{OL}$ | Output Low Voltage | $I_O$ = 1.6mA | ● | | 0.2 | 0.4 | V |
| $I_{OSR}$ | Output Short-Circuit Current | 0V ≤ $V_O$ ≤ $V_{IN}$ | ● | | | ±50 | mA |
| $I_{OZR}$ | Three-State Output Current | M0 = M1 = M2 = $V_{IN}$, $V_O$ = GND<br>M0 = M1 = M2 = $V_{IN}$, $V_O$ = $V_{IN}$ | ●<br>● | –30<br> | –85<br> | –160<br>±10 | µA<br>µA |
| **V.11 Driver** | | | | | | | |
| $V_{ODO}$ | Open Circuit Differential Output Voltage | $R_L$ = 1.95k (Figure 1) | ● | | | ±5 | V |
| $V_{ODL}$ | Loaded Differential Output Voltage | $R_L$ = 50Ω (Figure 1) | <br>● | 0.5$V_{ODO}$<br>±2 | | 0.67$V_{ODO}$ | V<br>V |
| $\Delta V_{OD}$ | Change in Magnitude of Differential Output Voltage | $R_L$ = 50Ω (Figure 1) | ● | | | 0.2 | V |
| $V_{OC}$ | Common Mode Output Voltage | $R_L$ = 50Ω (Figure 1) | ● | | | 3 | V |
| $\Delta V_{OC}$ | Change in Magnitude of Common Mode Output Voltage | $R_L$ = 50Ω (Figure 1) | ● | | | 0.2 | V |
| $I_{SS}$ | Short-Circuit Current | $V_{OUT}$ = GND | | | | ±150 | mA |
| $I_{OZ}$ | Output Leakage Current | –0.25V ≤ $V_O$ ≤ 0.25V, Power Off or No-Cable Mode or Driver Disabled | ● | | ±1 | ±100 | µA |
| $t_r$, $t_f$ | Rise or Fall Time | LTC2845C (Figures 2, 5)<br>LTC2845I (Figures 2, 5) | ●<br>● | 2<br>2 | 15<br>15 | 25<br>35 | ns<br>ns |
| $t_{PLH}$ | Input to Output | LTC2845C (Figures 2, 5)<br>LTC28451 (Figures 2, 5) | ●<br>● | 20<br>20 | 40<br>40 | 65<br>75 | ns<br>ns |
| $t_{PHL}$ | Input to Output | LTC2845C (Figures 2, 5)<br>LTC2845I (Figures 2, 5) | ●<br>● | 20<br>20 | 40<br>40 | 65<br>75 | ns<br>ns |
| $\Delta t$ | Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$ | LTC2845C (Figures 2, 5)<br>LTC2845I (Figures 2, 5) | ●<br>● | 0<br>0 | 3<br>3 | 12<br>17 | ns<br>ns |
| $t_{SKEW}$ | Output to Output Skew | (Figures 2, 5) | | | 3 | | ns |
| **V.11 Receiver** | | | | | | | |
| $V_{TH}$ | Input Threshold Voltage | –7V ≤ $V_{CM}$ ≤ 7V | ● | –0.2 | | 0.2 | V |
| $\Delta V_{TH}$ | Input Hysteresis | –7V ≤ $V_{CM}$ ≤ 7V | ● | | 15 | 40 | mV |
| $I_{IN}$ | Input Current (A, B) | –10V ≤ $V_{A,B}$ ≤ 10V | ● | | | ±0.66 | mA |
| $R_{IN}$ | Input Impedance | –10V ≤ $V_{A,B}$ ≤ 10V | ● | 15 | 30 | | kΩ |
| $t_r$, $t_f$ | Rise or Fall Time | (Figures 2, 6) | | | 15 | | ns |

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 5V, $V_{IN}$ = 3.3V, $V_{DD}$ = 8V, $V_{EE}$ = – 7V for V.28, – 5.5V for V.10, V.11 (Notes 2, 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Input to Output | LTC2845C $C_L$ = 50pF (Figures 2, 6)<br>LTC2845I $C_L$ = 50pF (Figures 2, 6) | ●<br>● | | 50<br>50 | 80<br>90 | ns<br>ns |
| $t_{PHL}$ | Input to Output | LTC2845C $C_L$ = 50pF (Figures 2, 6)<br>LTC2845I $C_L$ = 50pF (Figures 2, 6) | ●<br>● | | 50<br>50 | 80<br>90 | ns<br>ns |
| $\Delta t$ | Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$ | LTC2845C $C_L$ = 50pF (Figures 2, 6)<br>LTC2845I $C_L$ = 50pF (Figures 2, 6) | ●<br>● | 0<br>0 | 4<br>4 | 16<br>21 | ns<br>ns |
| **V.10 Driver** | | | | | | | |
| $V_O$ | Output Voltage | Open Circuit, $R_L$ = 3.9k | ● | ±4 | | ±6 | V |
| $V_T$ | Output Voltage | $R_L$ = 450Ω (Figure 3)<br>$R_L$ = 450Ω (Figure 3) | ● | ±3.6<br>0.9$V_O$ | | | V |
| $I_{SS}$ | Short-Circuit Current | $V_O$ = GND | | | | ±150 | mA |
| $I_{OZ}$ | Output Leakage Current | –0.25V ≤ $V_O$ ≤ 0.25V, Power Off or No-Cable Mode or Driver Disabled | ● | | ±0.1 | ±100 | µA |
| $t_r$, $t_f$ | Rise or Fall Time | $R_L$ = 450Ω, $C_L$ = 100pF (Figures 3, 7) | | | 2 | | µs |
| $t_{PLH}$ | Input to Output | $R_L$ = 450Ω, $C_L$ = 100pF (Figures 3, 7) | | | 1 | | µs |
| $t_{PHL}$ | Input to Output | $R_L$ = 450Ω, $C_L$ = 100pF (Figures 3, 7) | | | 1 | | µs |
| **V.10 Receiver** | | | | | | | |
| $V_{TH}$ | Receiver Input Threshold Voltage | | ● | –0.25 | | 0.25 | V |
| $\Delta V_{TH}$ | Receiver Input Hysteresis | | ● | | 25 | 50 | mV |
| $I_{IN}$ | Receiver Input Current | –10V ≤ $V_A$ ≤ 10V | ● | | | ±0.66 | mA |
| $R_{IN}$ | Receiver Input Impedance | –10V ≤ $V_A$ ≤ 10V | ● | 15 | 30 | | kΩ |
| $t_r$, $t_f$ | Rise or Fall Time | $C_L$ = 50pF (Figures 4, 8) | | | 15 | | ns |
| $t_{PLH}$ | Input to Output | $C_L$ = 50pF (Figures 4, 8) | | | 55 | | ns |
| $t_{PHL}$ | Input to Output | $C_L$ = 50pF (Figures 4, 8) | | | 109 | | ns |
| $\Delta t$ | Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$ | $C_L$ = 50pF (Figures 4, 8) | | | 60 | | ns |
| **V.28 Driver** | | | | | | | |
| $V_O$ | Output Voltage | Open Circuit<br>$R_L$ = 3k (Figure 3) | ●<br>● | <br>±5 | <br>±8.5 | ±10 | V<br>V |
| $I_{SS}$ | Short-Circuit Current | $V_O$ = GND | ● | | | ±150 | mA |
| $I_{OZ}$ | Output Leakage Current | –0.25V ≤ $V_O$ ≤ 0.25V, Power Off or No-Cable Mode or Driver Disabled | ● | | ±1 | ±100 | µA |
| SR | Slew Rate | $R_L$ = 3k, $C_L$ = 2500pF (Figures 3, 7) | ● | 4 | | 30 | V/µs |
| $t_{PLH}$ | Input to Output | $R_L$ = 3k, $C_L$ = 2500pF (Figures 3, 7) | ● | | 1.3 | 2.5 | µs |
| $t_{PHL}$ | Input to Output | $R_L$ = 3k, $C_L$ = 2500pF (Figures 3, 7) | ● | | 1.3 | 2.5 | µs |
| **V.28 Receiver** | | | | | | | |
| $V_{THL}$ | Input Low Threshold Voltage | | ● | | | 0.8 | V |
| $V_{TLH}$ | Input High Threshold Voltage | | ● | 2 | | | V |
| $\Delta V_{TH}$ | Receiver Input Hysterisis | | ● | | 0.1 | 0.3 | V |
| $R_{IN}$ | Receiver Input Impedance | –15V ≤ $V_A$ ≤ 15V | ● | 3 | 5 | 7 | kΩ |
| $t_r$, $t_f$ | Rise or Fall Time | $C_L$ = 50pF (Figures 4, 8) | | | 15 | | ns |
| $t_{PLH}$ | Input to Output | $C_L$ = 50pF (Figures 4, 8) | ● | | 60 | 100 | ns |
| $t_{PHL}$ | Input to Output | $C_L$ = 50pF (Figures 4, 8) | ● | | 150 | 500 | ns |

## ELECTRICAL CHARACTERISTICS

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All currents into device pins are positive; all currents out of device are negative. All voltages are referenced to device ground unless otherwise specified.

**Note 3:** All typicals are given for $V_{CC}$ = 5V, $V_{IN}$ = 3.3V, $V_{DD}$ = 8V, $V_{EE}$ = –7V for V.28, –5.5V for V.10, V.11 and $T_A$ = 25°C.

## PIN FUNCTIONS

**$V_{CC}$ (Pins 1, 19):** Positive Supply for the Transceivers. Connect to $V_{CC}$ Pin 8 on LTC2846 or to 5V supply. Connect a 1µF capacitor to ground.

**$V_{DD}$ (Pin 2):** Positive Supply Voltage for V.28. Connect to $V_{DD}$ Pin 7 on LTC2846 or 8V supply. Connect a 1µF capacitor to ground.

**D1 (Pin 3):** TTL Level Driver 1 Input.

**D2 (Pin 4):** TTL Level Driver 2 Input.

**D3 (Pin 5):** TTL Level Driver 3 Input.

**R1 (Pin 6):** CMOS Level Receiver 1 Output. Receiver outputs have a weak pull up to $V_{IN}$ when high impedance.

**R2 (Pin 7):** CMOS Level Receiver 2 Output.

**R3 (Pin 8):** CMOS Level Receiver 3 Output.

**D4 (Pin 9):** TTL Level Driver 4 Input.

**R4 (Pin 10):** CMOS Level Receiver 4 Output.

**M0 (Pin 11):** TTL Level Mode Select Input 0. Mode select inputs pull up to $V_{IN}$.

**M1 (Pin 12):** TTL Level Mode Select Input 1.

**M2 (Pin 13):** TTL Level Mode Select Input 2.

**DCE/$\overline{\text{DTE}}$ (Pin 14):** TTL Level Mode Select Input. Logic high enables Driver 3. Logic low enables Receiver 1.

**D4ENB (Pin 15):** TTL Level Enable Input. Logic low enables Driver 4. Pulls up to $V_{IN}$.

**R4EN (Pin 16):** TTL Level Enable Input. Logic high enables Receiver 4. Pulls up to $V_{IN}$.

**R5 (Pin 17):** CMOS Level Receiver 5 Output.

**D5 (Pin 18):** TTL Level Driver 5 Input.

**$V_{IN}$ (Pin 20):** Positive Supply for the Receiver Outputs. 3V ≤ $V_{IN}$ ≤ 3.6V. Connect a 1µF capacitor to ground.

**D5 A (Pin 21):** Driver 5 Output.

**R5 A (Pin 22):** Receiver 5 Input.

**R4 A (Pin 23):** Receiver 4 Input.

**D4 A (Pin 24):** Driver 4 Input.

**R3 B (Pin 25):** Receiver 3 Noninverting Input.

**R3 A (Pin 26):** Receiver 3 Inverting Input.

**R2 B (Pin 27):** Receiver 2 Noninverting Input.

**R2 A (Pin 28):** Receiver 2 Inverting Input.

**D3/R1 B (Pin 29):** Receiver 1 Noninverting Input and Driver 3 Noninverting Output.

**D3/R1 A (Pin 30):** Receiver 1 Inverting Input and Driver 3 Inverting Output.

**D2 B (Pin 31):** Driver 2 Noninverting Output.

**D2 A (Pin 32):** Driver 2 Inverting Output.

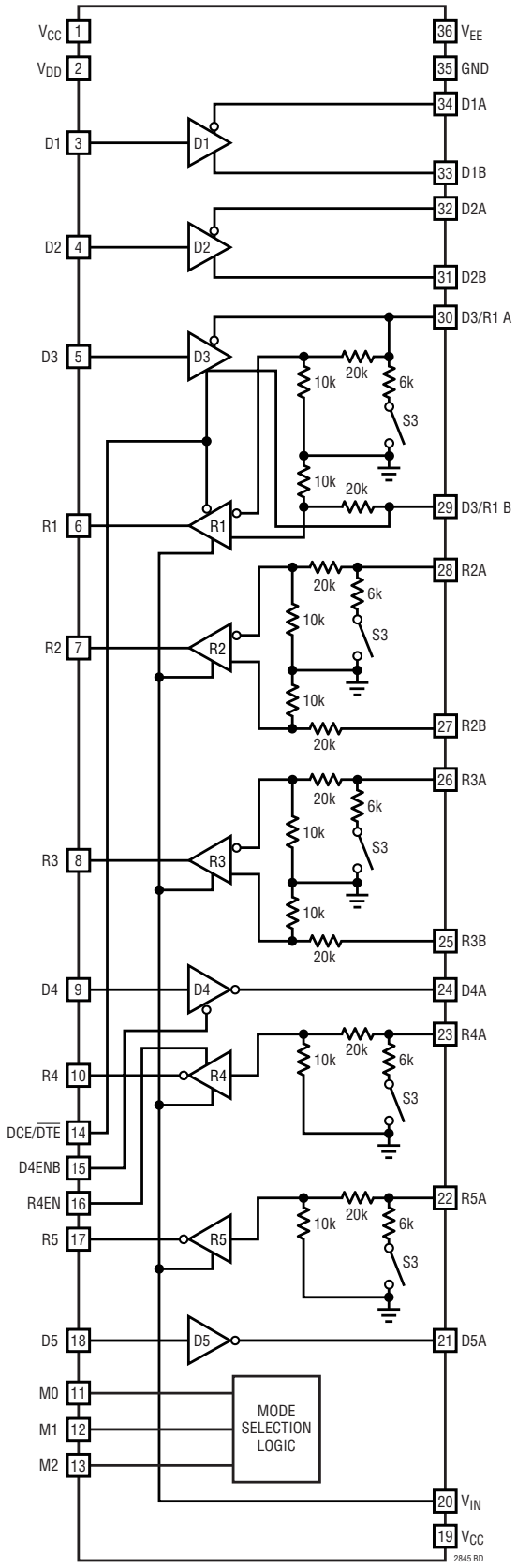
**D1 B (Pin 33):** Driver 1 Noninverting Output.

**D1 A (Pin 34):** Driver 1 Inverting Output.

**GND (Pin 35):** Ground.

**$V_{EE}$ (Pin 36):** Negative Supply Voltage. Connect to $V_{EE}$ Pin 31 on LTC2846 or to –7V supply. Connect a 1µF capacitor to ground.

## BLOCK DIAGRAM



## TEST CIRCUITS

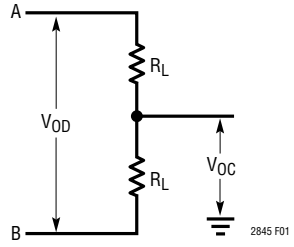



**Figure 1. V.11 Driver Test Circuit**

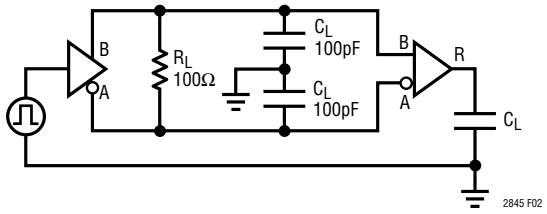



**Figure 2. V.11 Driver/Receiver AC Test Circuit**

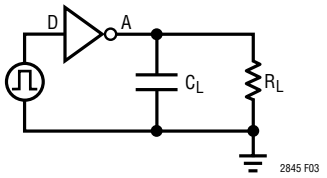



**Figure 3. V.10/V.28 Driver Test Circuit**

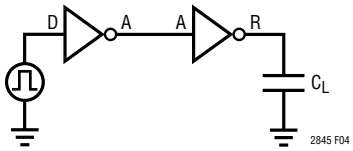



**Figure 4. V.10/V.28 Receiver Test Circuit**

## MODE SELECTION

| LTC2845 MODE NAME | M2 | M1 | M0 | D1 | D2 | (Note 1) D3 | (Note 2) D4 | D5 | (Note 1) R1 | R2 | R3 | (Note 3) R4 | R5 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Not Used (Default V.11) | 0 | 0 | 0 | V.11 | V.11 | V.11 | V.10 | V.10 | V.11 | V.11 | V.11 | V.10 | V.10 |
| RS530A | 0 | 0 | 1 | V.11 | V.10 | V.11 | V.10 | V.10 | V.11 | V.10 | V.11 | V.10 | V.10 |
| RS530 | 0 | 1 | 0 | V.11 | V.11 | V.11 | V.10 | V.10 | V.11 | V.11 | V.11 | V.10 | V.10 |
| X.21 | 0 | 1 | 1 | V.11 | V.11 | V.11 | V.10 | V.10 | V.11 | V.11 | V.11 | V.10 | V.10 |
| V.35 | 1 | 0 | 0 | V.28 | V.28 | V.28 | V.28 | V.28 | V.28 | V.28 | V.28 | V.28 | V.28 |
| RS449/V.36 | 1 | 0 | 1 | V.11 | V.11 | V.11 | V.10 | V.10 | V.11 | V.11 | V.11 | V.10 | V.10 |
| V.28/RS232 | 1 | 1 | 0 | V.28 | V.28 | V.28 | V.28 | V.28 | V.28 | V.28 | V.28 | V.28 | V.28 |
| D4ENB = 1, R4EN = 0 M0 = M1 = M2 = 1 | 1 | 1 | 1 | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z |

**Note 1:** Driver 3 and Receiver 1 are enabled (and disabled) by DCE/$\overline{\text{DTE}}$ (Pin 14). Logic high enables Driver 3. Logic low enables Receiver 1.

**Note 2:** Driver 4 is enabled by D4ENB = 0 (Pin 15).

**Note 3:** Receiver 4 is enabled by R4EN = 1 (Pin 16).

## SWITCHING TIME WAVEFORMS

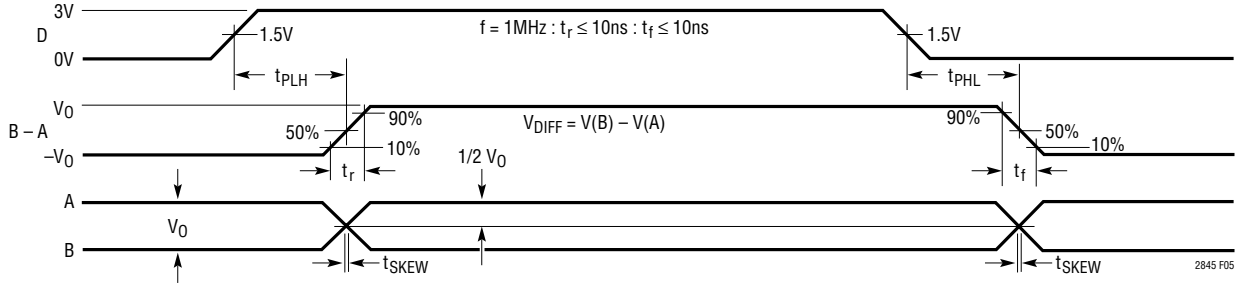



**Figure 5. V.11 Driver Propagation Delays**

## SWITCHING TIME WAVEFORMS

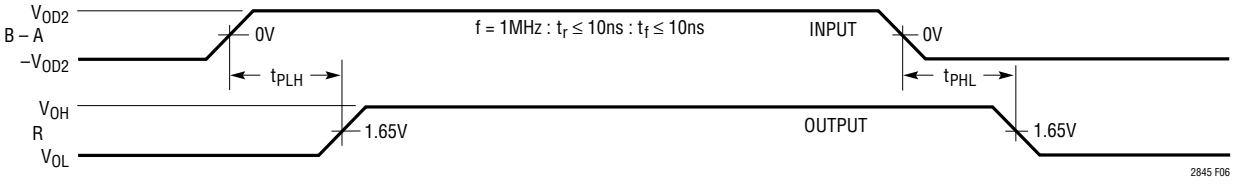



**Figure 6. V.11 Receiver Propagation Delays**

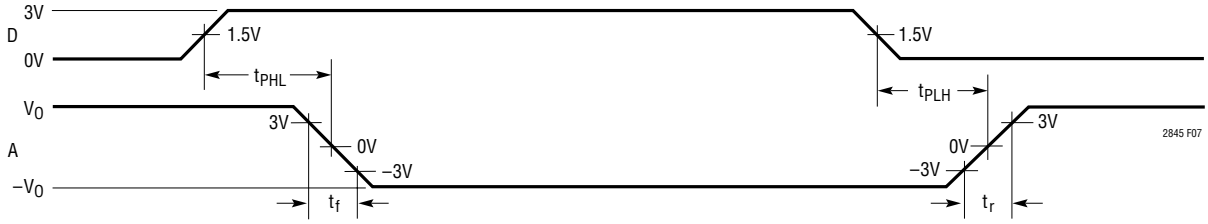



**Figure 7. V.10, V.28 Driver Propagation Delays**

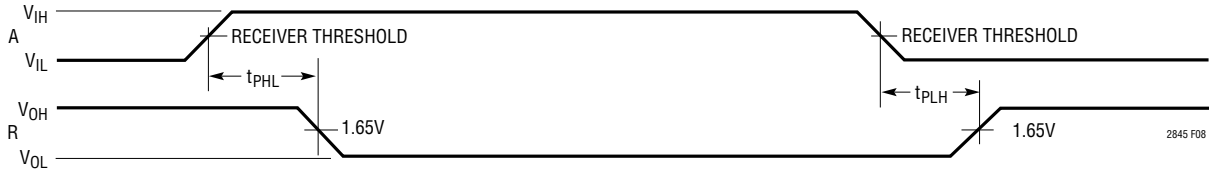



**Figure 8. V.10, V.28 Receiver Propagation Delays**

## APPLICATIONS INFORMATION

### Overview

The LTC2846/LTC2845 form the core of a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA530, EIA530-A, V.35, V.36 or X.21 protocols. Cable termination is provided on-chip, eliminating the need for discrete designs.

A complete DCE-to-DTE interface operating in EIA530 mode is shown in Figure 9. The LTC2846 of each port is used to generate the clock and data signals. The LTC2845 is used to generate the control signals along with LL (Local Loop-Back), RL (Remote Loop-Back), TM (Test Mode) and RI (Ring Indicate). Cable termination is used only for the clock and data signals because they must support V.11 cable termination. The control signals do not need any external resistors.

### Mode Selection

The interface protocol is selected using the mode select pins M0, M1 and M2 (see the Mode Selection table).

For example, if the port is configured as a V.35 interface, the mode selection pins should be M2 = 1, M1 = 0, M0 = 0. For the control signals, the drivers and receivers will operate in V.28 (RS232) electrical mode. For the clock and data signals, the drivers and receivers will operate in V.35 electrical mode. The DCE/$\overline{\text{DTE}}$ pin will configure the port for DCE mode when high, and DTE when low.

The interface protocol may be selected simply by plugging the appropriate interface cable into the connector. The mode pins are routed to the connector and are left unconnected (1) or wired to ground (0) in the cable as shown in Figure 10.

## APPLICATIONS INFORMATION

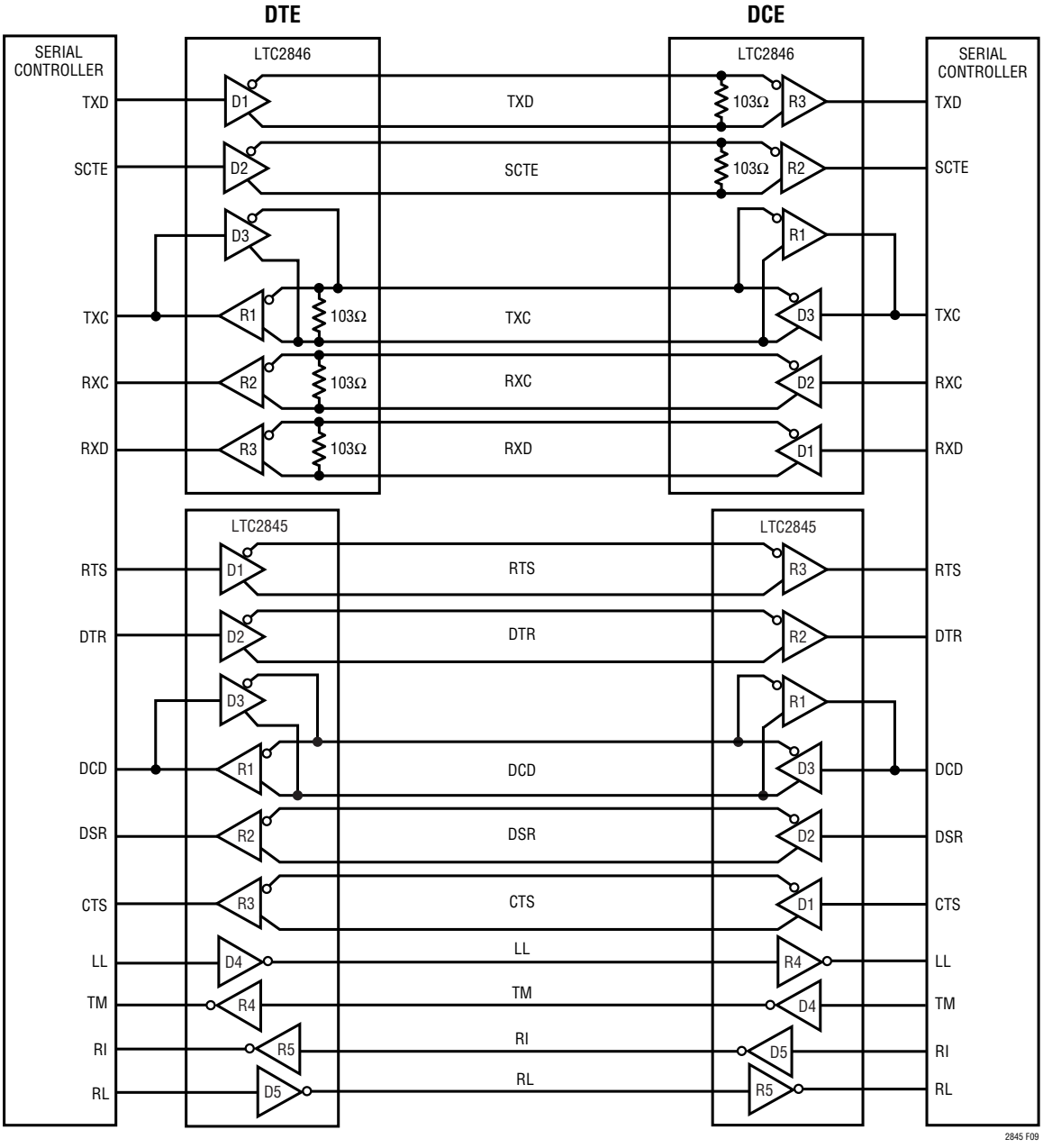



**Figure 9. Complete Multiprotocol Interface in EIA530 Mode**

The internal pull-up current sources will ensure a binary 1 when a pin is left unconnected and that the LTC2846/LTC2845 enters the no-cable mode when the cable is removed. In the no-cable mode the LTC2846/LTC2845 supply current drops to less than 1400µA and all driver outputs are forced into a high impedance state.

The mode selection may also be accomplished by using jumpers to connect the mode pins to ground or $V_{IN}$.

### Cable Termination

Traditional implementations have included switching resistors with expensive relays, or required the user to change termination modules every time the interface

## APPLICATIONS INFORMATION

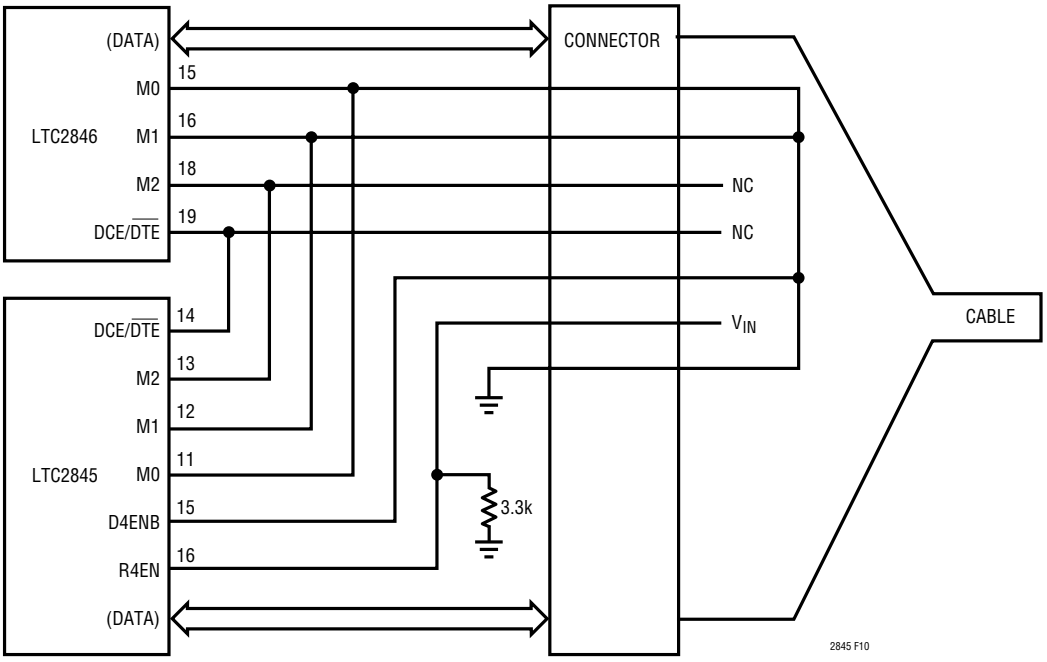



**Figure 10: Single Port DCE V.35 Mode Selection in the Cable**

standard has changed. Custom cables have been used with the termination in the cable head or separate terminations are built on the board and a custom cable routes the signals to the appropriate termination. Switching the termination with FETs is difficult because the FETs must remain off even though the signal voltage is beyond the supply voltage for the FET drivers or the power is off.

Using the LTC2846/LTC2845 solves the cable termination switching problem. Via software control, appropriate termination for the V.10 (RS423), V.11 (RS422), V.28 (RS232) and V.35 electrical protocols is chosen.

### V.10 (RS423) Interface

A typical V.10 unbalanced interface is shown in Figure 11. A V.10 single-ended generator output A with ground C is connected to a differential receiver with inputs A' connected to A, and input C' connected to the signal return ground C. Usually, no cable termination is required for V.10 interfaces, but the receiver inputs must be compliant with the impedance curve shown in Figure 12.

The V.10 receiver configuration in the LTC2845 is shown in Figure 13. In V.10 mode switch S3 inside the LTC2845 is turned off. The noninverting input is disconnected inside the LTC2845 receiver and connected to ground.The cable termination is then the 30k input impedance to ground of the LTC2845 V.10 receiver.

### V.11 (RS422) Interface

A typical V.11 balanced interface is shown in Figure 14. A V.11 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.11 interface has a differential termination at the receiver end that has a minimum value of 100Ω. The termination resistor is optional in the V.11 specification, but for the high speed clock and data lines, the termination is required to prevent reflections from corrupting the data. The receiver inputs must also be compliant with the impedance curve shown in Figure 12.

## APPLICATIONS INFORMATION

In V.11 mode, all switches are off except S1 of the LTC2846's receivers which connects a 103Ω differential termination impedance to the cable as shown in Figure 15[1]. The LTC2845 only handles control signals, so no termination other than its V.11 receivers' 30k input impedance is necessary.

[1]Actually, there is no switch S1 in receivers R2 and R3. However, for simplicity, all termination networks on the LTC2846 can be treated identically if it is assumed that an S1 switch exists and is always closed on the R2 and R3 receivers.

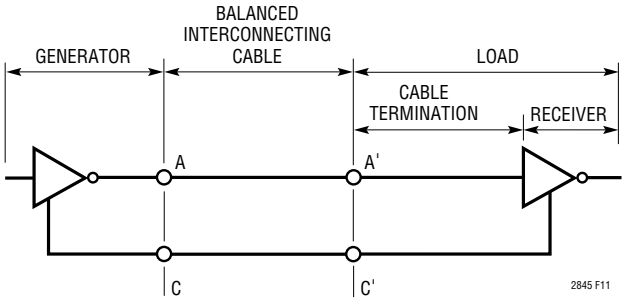



**Figure 11. Typical V.10 Interface**

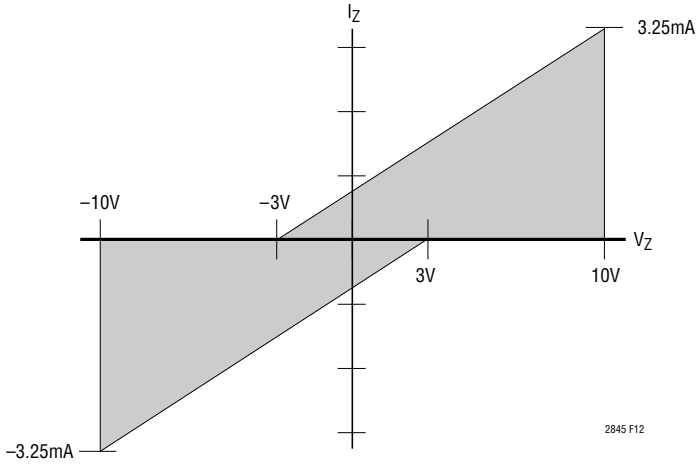



**Figure 12. V.10 Receiver Input Impedance**

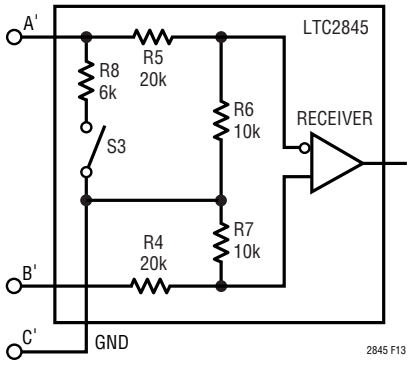



**Figure 13. V.10 Receiver Configuration**

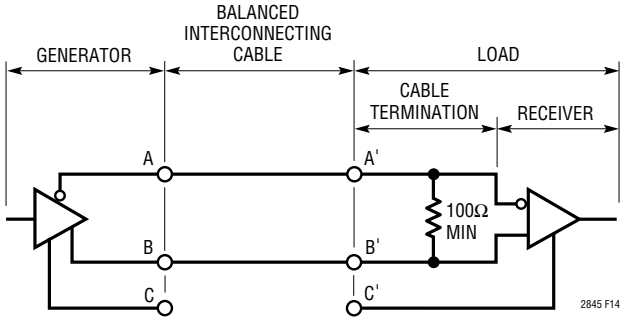



**Figure 14. Typical V.11 Interface**

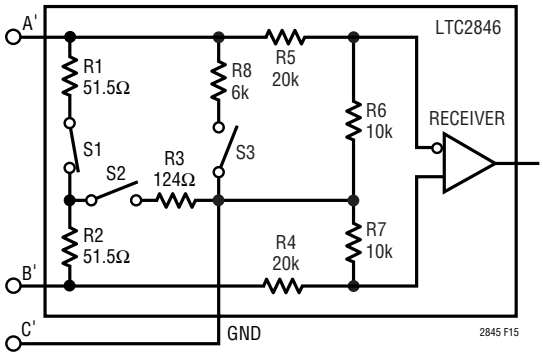



**Figure 15. V.11 Receiver Configuration**

## APPLICATIONS INFORMATION

### V.28 (RS232) Interface

A typical V.28 unbalanced interface is shown in Figure 16. A V.28 single-ended generator output A with ground C is connected to a single-ended receiver with input A' connected to A, ground C' connected via the signal return ground C.

In V.28 mode, all switches are off except S3 inside the LTC2846/LTC2845 which connects a 6k (R8) impedance to ground in parallel with 20k (R5) plus 10k (R6) for a combined impedance of 5k as shown in Figure 17. The noninverting input is disconnected inside the LTC2846/LTC2845 receiver and connected to a TTL level reference voltage for a 1.4V receiver trip point.

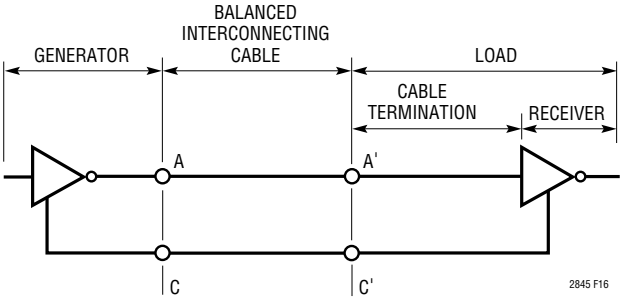



**Figure 16. Typical V.28 Interface**

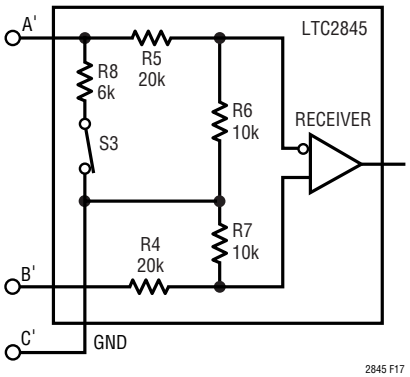



**Figure 17. V.28 Receiver Configuration**

# APPLICATIONS INFORMATION

### V.35 Interface

A typical V.35 balanced interface is shown in Figure 18. A V.35 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.35 interface requires a T or delta network termination at the receiver end and the generator end. The receiver differential impedance measured at the connector must be 100Ω ±10Ω, and the impedance between shorted terminals (A' and B') and ground C' must be 150Ω ±15Ω.

In V.35 mode, both switches S1 and S2 inside the LTC2846 are on, connecting the T network impedance as shown in Figure 19. The 30k input impedance of the receiver is placed in parallel with the T network termination, but does not affect the overall input impedance significantly.

The generator differential impedance must be 50Ω to 150Ω and the impedance between shorted terminals (A and B) and ground C must be 150Ω ±15Ω. For the generator termination, switches S1 and S2 are both on as shown in Figure 20.

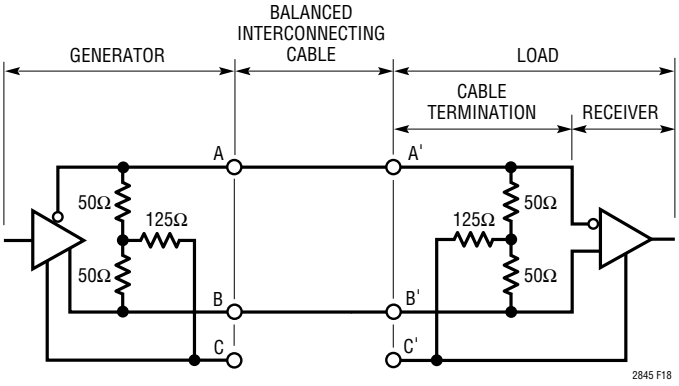



Figure 18. Typical V.35 Interface

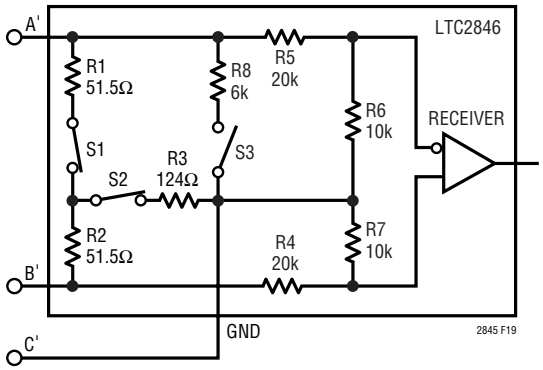



Figure 19. V.35 Receiver Configuration

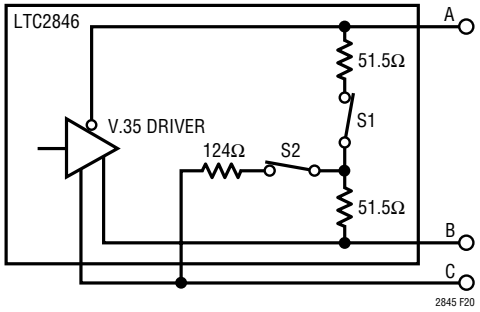



Figure 20. V.35 Driver

## APPLICATIONS INFORMATION

### No-Cable Mode

The no-cable mode (M0 = M1 = M2 = D4ENB = 1, R4EN = 0) is intended for the case when the cable is disconnected from the connector. The bias circuitry, drivers and receivers are turned off, the driver outputs are forced into a high impedance state, and the supply current drops to less than 1400µA.

### LTC2846 Supplies

The LTC2846 uses an internal capacitive charge pump to generate $V_{DD}$ and $V_{EE}$ as shown in Figure 21. A voltage doubler generates about 8V on $V_{DD}$ and a voltage inverter generates about –7.5V for $V_{EE}$. Three 1µF surface mounted tantalum or ceramic capacitors are required for C1, C2 and C3. The $V_{EE}$ capacitor C4 should be a minimum of 3.3µF. All capacitors are 16V and should be placed as close as possible to the LTC2846 to reduce EMI.

The LTC2846 has an internal boost switching regulator which generates a 5V output from the 3.3V supply as shown in Figure 22. The 5V $V_{CC}$ supplies its internal charge pump and transceivers as well as its companion chip.

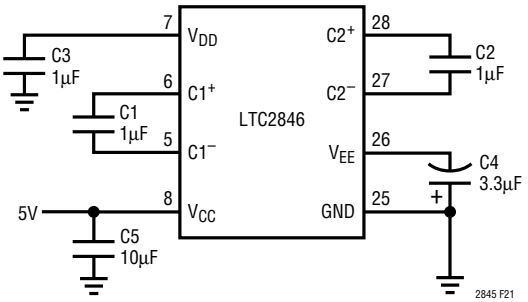



**Figure 21. Charge Pump**

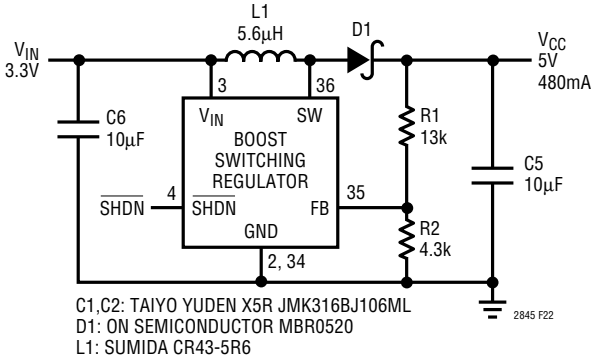



**Figure 22. Boost Switching Regulator**

## APPLICATIONS INFORMATION

### Receiver Fail-Safe

All LTC2846/LTC2845 receivers feature fail-safe operation in all modes. If the receiver inputs are left floating or shorted together by a termination resistor, the receiver output will always be forced to a logic high.

### DTE vs DCE Operation

The DCE/$\overline{DTE}$ pin acts as an enable for Driver 3/Receiver 1 in the LTC2846, and Driver 3/Receiver 1 in the LTC2845.

The LTC2846/LTC2845 can be configured for either DTE or DCE operation in one of two ways: a dedicated DTE or DCE port with a connector of appropriate gender, or a port with one connector that can be configured for DTE or DCE operation by rerouting the signals to the LTC2846/LTC2845 using a dedicated DTE cable or dedicated DCE cable.

A dedicated DTE port using a DB-25 male connector is shown in Figure 23. The interface mode is selected by logic outputs from the controller or from jumpers to either $V_{IN}$ or GND on the mode select pins. A dedicated DCE port using a DB-25 female connector is shown in Figure 24.

A port with one DB-25 connector, can be configured for either DTE or DCE operation is shown in Figure 25. The configuration requires separate cables for proper signal routing in DTE or DCE operation. For example, in DTE mode, the TXD signal is routed to Pins 2 and 14 via Driver 1 in the LTC2846. In DCE mode, Driver 1 now routes the RXD signal to Pins 2 and 14.

# TYPICAL APPLICATIONS

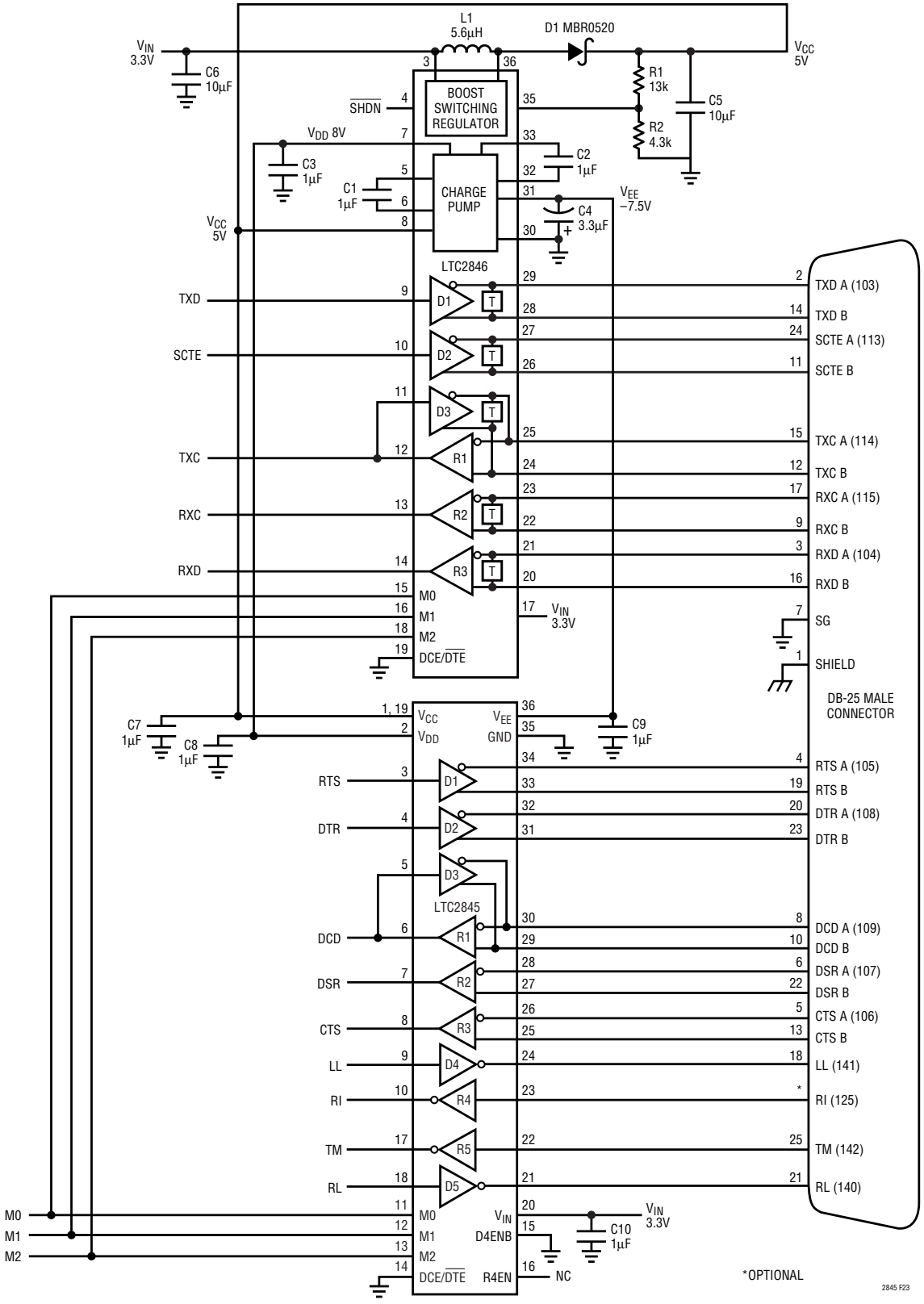



**Figure 23. Controller-Selectable Multiprotocol DTE Port with DB-25 Connector**

# TYPICAL APPLICATIONS

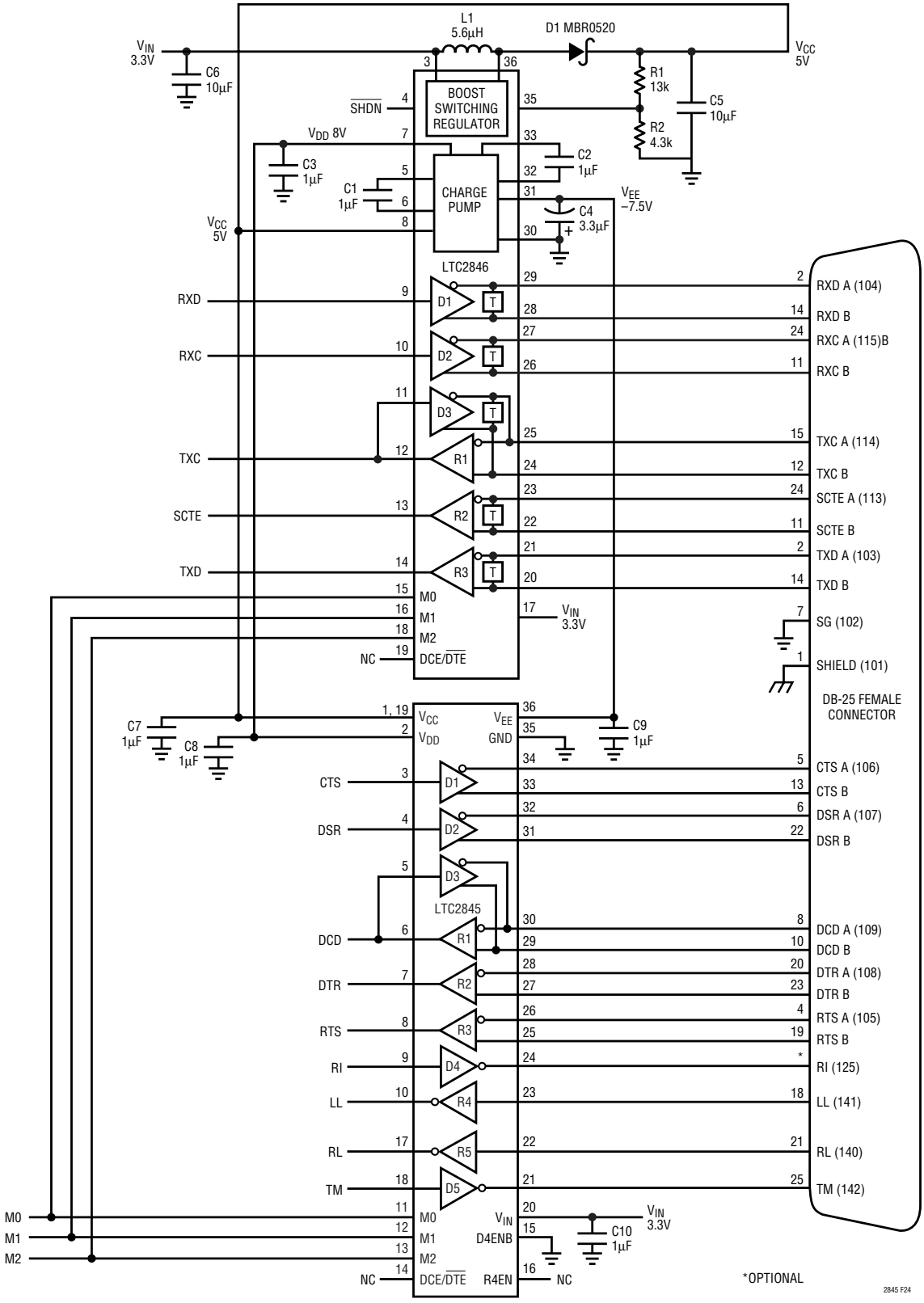



**Figure 24. Controller-Selectable DCE Port with DB-25 Connector**

# TYPICAL APPLICATIONS

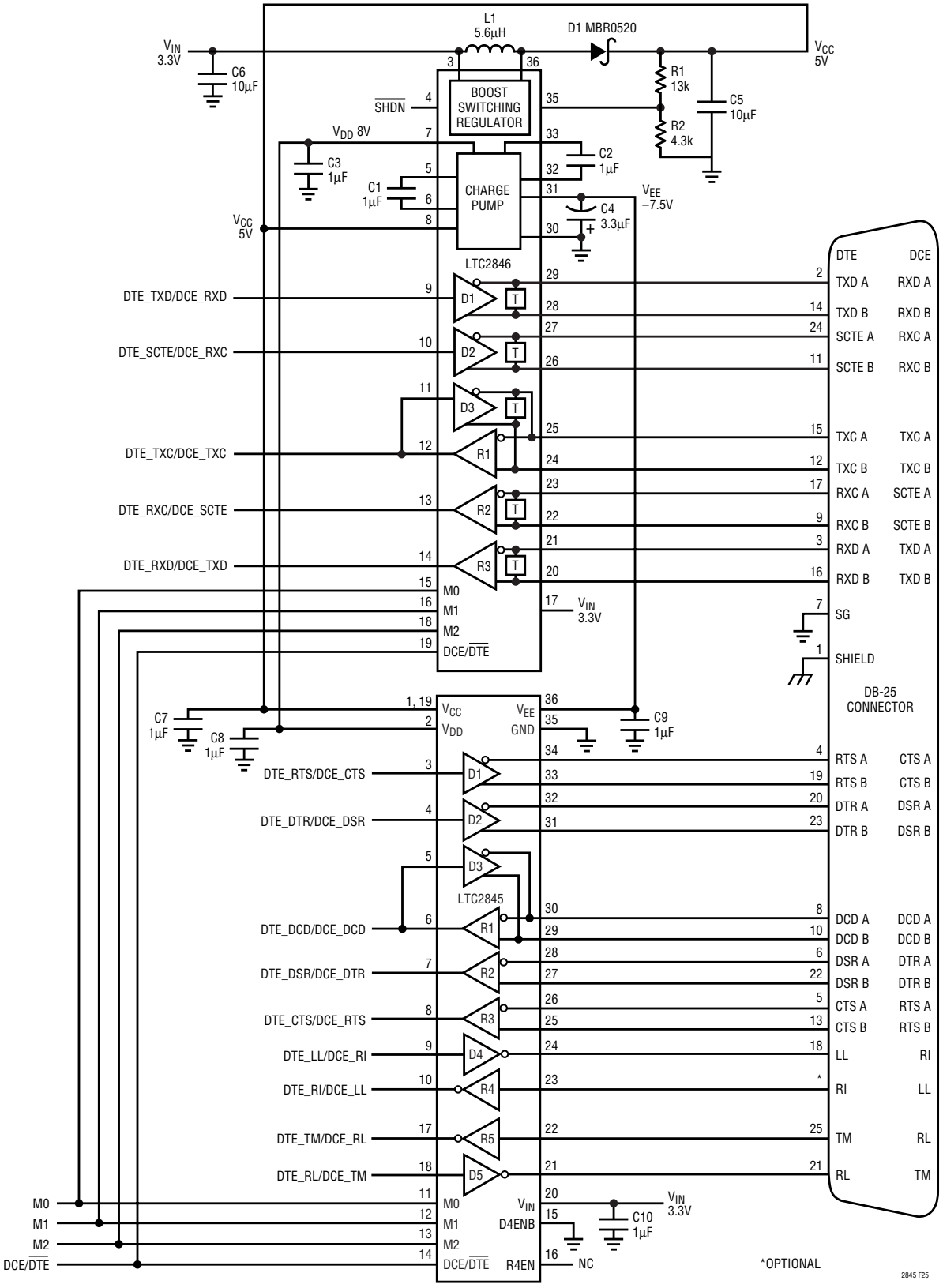
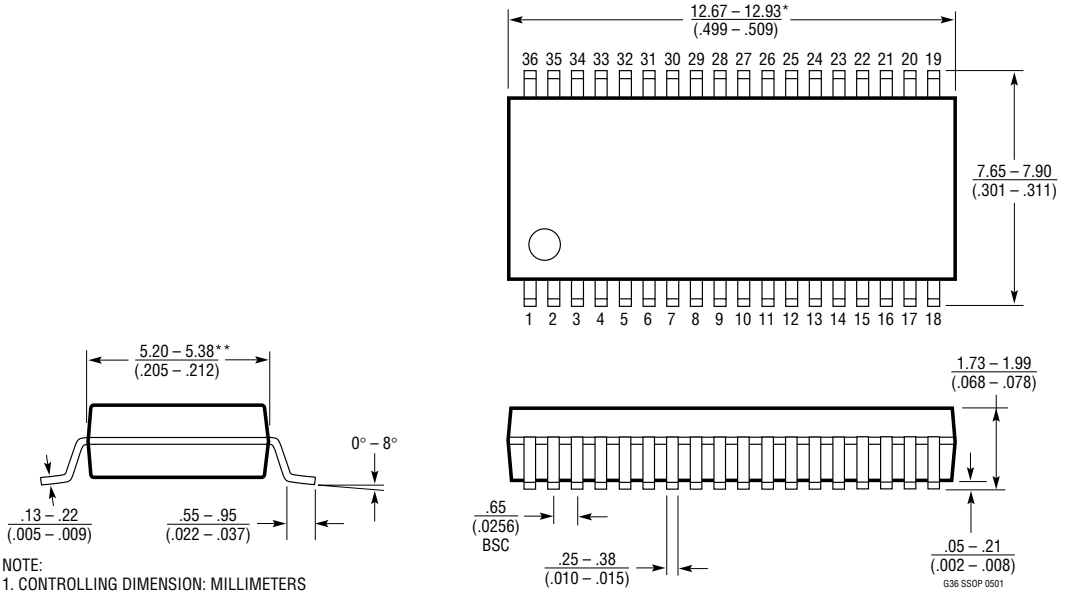



**Figure 25. Controller-Selectable Multiprotocol DTE/DCE Port with DB-25 Connector**

# PACKAGE DESCRIPTION

**G Package**
**36-Lead Plastic SSOP (5.3mm)**
(Reference LTC DWG # 05-08-1640)




NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
   *DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
   **DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1321 | Dual RS232/RS485 Transceiver | Two RS232 Driver/Receiver Pairs or Two RS485 Driver/Receiver Pairs |
| LTC1334 | Single 5V RS232/RS485 Multiprotocol Transceiver | Two RS232 Driver/Receiver or Four RS232 Driver/Receiver Pairs |
| LTC1343 | Software-Selectable Multiprotocol Transceiver | 4-Driver/4-Receiver for Data and Clock Signals |
| LTC1344A | Software-Selectable Cable Terminator | Perfect for Terminating the LTC1543 (Not Needed with LTC1546) |
| LTC1345 | Single Supply V.35 Transceiver | 3-Driver/3-Receiver for Data and Clock Signals |
| LTC1346A | Dual Supply V.35 Transceiver | 3-Driver/3-Receiver for Data and Clock Signals |
| LTC1543 | Software-Selectable Multiprotocol Transceiver | Terminated with LTC1344A for Data and Clock Signals, Companion to LTC1544 or LTC1545 for Control Signals |
| LTC1544 | Software-Selectable Multiprotocol Transceiver | Companion to LTC1546 or LTC1543 for Control Signals Including LL |
| LTC1545 | Software-Selectable Multiprotocol Transceiver | 5-Driver/5-Receiver Companion to LTC1546 or LTC1543 for Control Signals Including LL, TM and RL |
| LTC1546 | Software-Selectable Multiprotocol Transceiver | 3-Driver/3-Receiver with Termination for Data and Clock Signals |
| LTC2844 | 3.3V Software-Selectable Multiprotocol Transceiver | 3.3V Supply, 4-Driver/4-Receiver Companion to LTC2846 for Control Signals Including LL |
| LTC2846 | 3.3V Software-Selectable Multiprotocol Transceiver | 3.3V Supply, 3-Driver/3-Receiver with Termination for Data and Clock Signals, Generates the Required 5V and ±8V Supplies for LTC2846 and Companion Parts |



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